

GE Energy

Mark* VI Control System Guide, Volume II

GEH-6421M



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Documentation Design, Rm. 293
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Safety Symbol Legend



Warning

Indicates a procedure, condition, or statement that, if not strictly observed, could result in personal injury or death.



Caution

Indicates a procedure, condition, or statement that, if not strictly observed, could result in damage to or destruction of equipment.



Attention

Indicates a procedure, condition, or statement that should be strictly followed in order to optimize these applications.

Note Indicates an essential or important procedure, condition, or statement.



This equipment contains a potential hazard of electric shock or burn. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Isolation of test equipment from the equipment under test presents potential electrical hazards. If the test equipment cannot be grounded to the equipment under test, the test equipment's case must be shielded to prevent contact by personnel.

To minimize hazard of electrical shock or burn, approved grounding practices and procedures must be strictly followed.



To prevent personal injury or equipment damage caused by equipment malfunction, only adequately trained personnel should modify any programmable machine.

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I/O Overview

The following table lists all the I/O processor boards, the number of I/O per processor that they support, and their associated standard terminal boards. Some standard terminal boards have simplex and TMR versions (in addition to simplex DIN-rail mounted ones). Refer to the section, simplex DIN-rail mounted terminal board summary for simplex DIN-rail mounted terminal board information.

I/O Processor Boards and Standard Terminal Boards

I/O Processor Board	I/O Signal Type	Number of I/O per Processor	Associated Terminal Boards
VAIC	Analog inputs, 0-1 mA, 4-20 mA, voltage	20	TBAI
	Analog outputs, 4-20 mA, 0-200 mA	4	TBAI
VAOC	Analog outputs, 4-20 mA	16	TBAO
VCCC	Contact inputs	48	TBCI, TICI
	Solenoid outputs	12	TRLY
	Dry contact relay outputs	12	TRLY
VCRC	Contact inputs	48	TBCI
	Solenoid outputs	12	TRLY
	Dry contact relays outputs	12	TRLY
VGEN	Analog inputs, 4-20 mA	4	TGEN
	Potential transformers, gen (1) bus (1)	2	TGEN
	Current transformers on generator	3	TGEN
	Relay outputs (optional)	12	TRLY
VPRO	Pulse rate inputs	3	TPRO
	Potential transformers, gen (1), bus (1)	2	TPRO
	Thermocouple inputs	3	TPRO
	Analog inputs, 4-20 mA	3	TPRO
	Trip solenoid drivers	3	TREG (through J3)
	Trip interlock inputs	7	TREG (through J3)
	Emergency-stop input (hardwired)	1	TREG (through J3)
	Economizing relays	3	TREG (through J3)
	Trip solenoid drivers	3	TREG (2nd board through J4)
	Emergency-stop input (hardwired)	1	TREG (2nd board through J4)
	Economizing relays	3	TREG (2nd board through J4)
VPYR	Pyrometer temperature inputs (4/probe)	2	TPYR
	Keyphasor [®] shaft position inputs	2	TPYR
VRTD	Resistance temperature device (RTD)	16	TRTD
VSCA	Serial I/O communications	6	DSCB
VSVO	Servo outputs to hydraulic servo valve	4	TSVO
	LVDT inputs from valve position	12	TSVO
	LVDT excitation outputs	8	TSVO
	Pulse rate inputs for flow monitoring	2	TSVO
	Pulse rate probe excitation	2	TSVO
VTCC	Thermocouple inputs	24	TBTC
VAMA	Acoustic monitoring (Simplex only)	2	DDPT

I/O Processor Board	I/O Signal Type	Number of I/O per Processor	Associated Terminal Boards
VAMB	Acoustic monitoring (Simplex only)	18	TAMB
VTURH1B	Pulse rate magnetic speed pickups	4	TTUR
	Potential transformers, generator and bus	2	TTUR
	Shaft current and voltage monitor	2	TTUR
	Breaker Interface	1	TTUR
	Flame detectors (Geiger-Mueller)	8	TRPG (through J4)
	Trip solenoid drivers for ETDs	3	TRPG (through J4)
VTURH2B	Same as above, plus 3 trip solenoid drivers		TRPG (2nd board through J4A)
VVIB	Shaft Proximito [®] r/seismic probes (Vib/Displ/Accel)	16	TVIB
	Shaft proximity probes (displacement)	8	TVIB
	Shaft proximity reference (Keyphasor)	2	TVIB

Terminal Board Terminal Block Features

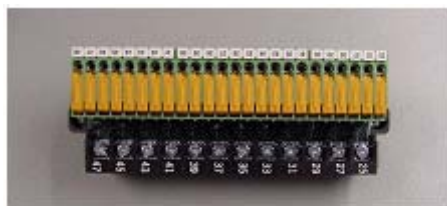
Many of the terminal boards in the Mark VI use a 24-position pluggable barrier terminal block (179C9123BB). These terminal blocks have the following features:

- Made from a polyester resin material with 130°C (266 °F) rating
- Terminal rating is 300 V, 10 A, UL class C general industry, 0.375 in creepage, 0.250 in strike
- UL and CSA code approved
- Screws finished in zinc clear chromate and contacts in tin
- Each block screw is number labeled 1 through 24 or 25 through 48 in white
- Recommended screw tightening torque is 8 in lbs

Terminal Board Disconnect Switch (TBSW)

The Mark VI Terminal Board Disconnect Switch (TBSW) provides an individual disconnect switch for each of the 48 customer I/O points on Mark VI terminal boards in the following figure. This facilitates such procedures as continuity checking, isolation for test, and others. Two TBSW assemblies are required for each terminal board, one numbered 1-24, the other numbered 25-48 (GE part numbers 336A4940CHG1 and 336A4940CHG2 respectively). The TBSW fits and connects into the terminal boards' 24-point pluggable barrier terminal block receptacles.

The TBSW is designed for continuous 5 A rms current at 300 V rms and complies with EN61010-1 clearance specifications. The NEMA power/voltage class rating (A, E, F, G) for the TBSW is dependant on the terminal board the TBSW is mounted upon see the following table.



Top View



Front View



Side View

TBSW Mounted to Terminal Block



The TBSW is not to be used for live circuit interruption. The circuit must be de-energized before the circuit is either closed or opened by the TBSW.

Caution

TBSW/Terminal Board Applications Summary

In the following table lists the TBSW/terminal board applications for the Mark VI. An OK indicated in the TBSW applications column indicates an approved application of the TBSW for terminal board specifications for voltage and current. Those board points that require limiting the terminal boards application are indicated with a note number (corresponding notes follow the table).

TBSW/Terminal Board Applications

Board	Type	TBSW Applications	
		CSA	NEMA
TBTC	Thermocouples	OK	OK
TRTD	RTDs	OK	OK
TBAI	Analog inputs	OK	OK
TBAO	Analog outputs	OK	OK
TBCI	Contact inputs	OK	OK
TICI	Contact inputs	Note 1	Note 2
TRLY	Contact outputs	Note 1	Note 2
TSVO	Servo I/O	OK	OK
TTUR	Turbine I/O	OK	OK
TRPG	Flame I/O	Note 3	Note 3
TREG		OK	OK
TRPL		OK	OK
TREL		OK	OK
TRPS		OK	OK
TRES		OK	OK
TPRO		OK	OK
TVIB		OK	OK
TGEN		OK	OK
TPYR		OK	OK

Table Notes:

1. The inputs on the TICI and TRLY boards are high voltage isolated inputs. The TBSW is classified by CSA for use up to 300 V rms. Circuits applied to the TICI or TRLY terminal board with the TBSW installed must be externally limited to 300 V rms. Care must also be taken to assure that no adjacent circuits, that when both are operating, do not exceed 300 V rms between them.

2. NEMA ratings are given according to the power and voltage limiting abilities of the circuit. The TICI and TRLY terminal boards carry no components that are designed to limit voltage or current. For this reason, the TBSW application limitations for these two terminal boards will depend on the customer's ability to install voltage and current limiting devices on the TBSW circuits according to NEMA guidelines. The following chart indicates the NEMA class and the voltage it must be limited too before it can be applied to the TBSW. Voltages are for circuit voltage, and circuit to adjacent circuit voltage.

Class	Voltage	Description
A	50 V peak	All circuits which cannot be otherwise classified. Use this rating when no external current and voltage limiting devices are present.
E	225 V peak	Known and controlled transient voltages without sufficient current limiting impedance.
F	300 V rms	Known and controlled voltages with short-circuit power 10 kVA or less.
G	300 V rms	Known and controlled voltages with short-circuit power 500VA or less.

3. The TRPG flame detectors require a 335 V dc circuit. The TBSW is classified by CSA and NEMA for use up to 300 V rms. Circuits applied to the TRPG terminal board flame detectors with the TBSW installed must be limited to 300 V rms, disallowing the use of the TBSW when the flame detectors are operational.

Relay Board Summary

Mark VI Relay Board Features

Feature	DRLYH1A DRLYH1B	TRLYH1B	TRLYH1C TRLYH2C	TRLYH1D	TRLYH1E TRLYH2E TRLYH3E	TRLYH1F TRLYH2F
Fused solenoid driver relays	0	6	6	6	0	12 (with WPDF)
# Dry circuit relays	12	5	5	0	12	12 (without WPDF)
Relay Type	Mechanical Form C	Mechanical Form C	Mechanical Form C	Mechanical Form C	Solid-State Form A	Mechanical H1F = Form A H2F = Form B
Control	Simplex	Simplex and TMR	Simplex and TMR	Simplex and TMR	Simplex and TMR	TMR Only
# Ignition transformer outputs	0	1	1	0	0	0
Relay suppression	No	MOV	MOV and R-C	MOV	No	No
Solenoid relay sensing type/quantity	No	Relay coil current/6	Relay NO contact voltage/6	Solenoid resistance /6	No	Relay coil current /12 (WPDF)
Other relay sensing type/quantity	No	Relay coil current/6	Relay NO contact voltage/6	N/A	Relay NO contact voltage/12	Relay coil current /12 (no WPDF)
Solenoid fuse sense	N/A	6	6	6	N/A	12 (WPDF)
Operating voltage V ac	120/240	120/240	H1=120/ 240 H2=No	No	H3= 120/240	120
Operating voltage V dc	28/125	24/125	H1=125 H2=24	24/ 110/ 125	H2=28 H3=125	28/125
Internal switching power supply	No	No	No	Yes	No	No
Daughterboards	None	None	18	None	None	WPDF
Terminal type	Euro-box	Barrier	Barrier	Barrier	Barrier	Barrier

Trip Terminal Board Summary

Mark VI Trip Terminal Board Features

Board	TMR	Simplex	Output Contacts, 125 V dc, 1 Amp	Output Contacts, 24 V dc, 3 Amp	ESTOP	Input Contacts, Dry, 125 V dc	Input Contacts, Dry, 24 V dc	Economy Resistor
TRPGH1A*	Yes	No	Yes	No	No	No	No	No
TRPGH1B	Yes	No	Yes	Yes	No	No	No	No
TRPGH2A*	No	Yes	Yes	No	No	No	No	No
TRPGH2B	No	Yes	Yes	Yes	No	No	No	No
TREGH1A*	Yes	No	Yes	No	Yes	Yes	No	Yes
TREGH1B	Yes	No	Yes	Yes	Yes	Yes	No	Yes
TREGH2B	Yes	No	Yes	Yes	Yes	No	Yes	Yes
TRPLH1A	Yes	No	Yes	Yes	Yes	No	No	No
TRELH1A	Yes	No	Yes	Yes	No	Yes	No	No
TRELH2A	Yes	No	Yes	Yes	No	No	Yes	No
TRPSH1A	Yes	Yes	Yes	Yes	Yes	No	No	No
TRESH1A	Yes	Yes	Yes	Yes	No	Yes	No	No
TRESH2A	Yes	Yes	Yes	Yes	No	No	Yes	No

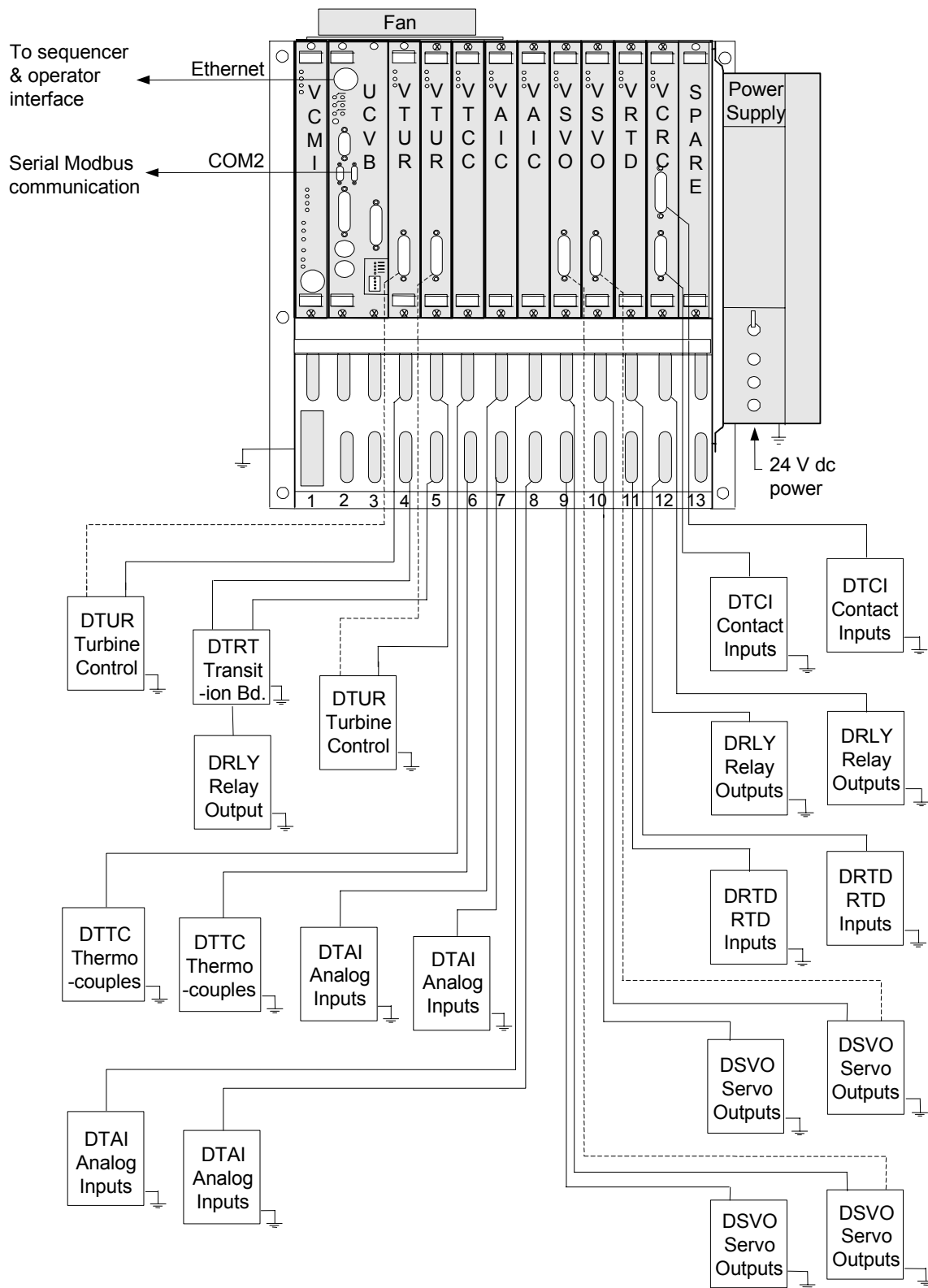
*These boards will become obsolete.

Simplex DIN-Rail Mounted Terminal Board Summary

Speed control systems for small turbines require a simplified system architecture. Simplex control is used to reduce cost and save space. Compact DIN-rail mounted terminal boards are available instead of the larger T-type terminal boards used on TMR systems. IONet is not used since the D-type terminal boards cable directly into the control chassis to interface with the I/O boards.

In the VME rack, a VCMi board provides two-way communication between the controller and the I/O processor boards. The controller Ethernet port is used to communicate with other system components, such as an operator interface or PLC. Additional PLC I/O can be tied into the system using the controller Genius port. A typical system is illustrated in the following figure. The system is powered by 24 V dc, and uses a low voltage version of the standard VME rack power supply.

The board designations and functions along with the corresponding I/O processor boards are listed in the following table. In all cases, the signal conditioning on the DIN-type terminal boards is the same as on the T-type boards, and the I/O specifications described apply. However, the number of inputs and outputs, and the grounding provisions differ, and the boards do not support TMR. Permanently mounted high-density Euro-Block terminal blocks are used to save space. The blocks have terminals accepting wire sizes up to one #12 wire, or two #14 wires. The typical wire size used is #18 AWG.



Small Simplex System Rack, Boards, and Cabling

DIN Euro Size Terminal board	Number of Points	Description of I/O	I/O Processor Board
DTTC	12	Thermocouple temperature inputs with one cold junction reference	VTCC
DRTD	8	RTD temperature inputs	VRTD
DTAI	10	Analog current or voltage inputs with on-board 24 V dc power supply	VAIC
	2	Analog current outputs, with choice of 20 mA or 200 mA	
DTAO	8	Analog current outputs, 0-20 mA	VAOC
DTCI	24	Contact Inputs with external 24 V dc excitation	VCRC (or VCCC)
DRLY	12	Form-C relay outputs, dry contacts, customer powered	VCRC (or VCCC)
DTRT	-----	Transition board between VTUR and DRLY for solenoid trip functions	VTUR
DTUR	4	Magnetic (passive) pulse rate pickups for speed and fuel flow measurement	VTUR
DSVO	2	Servo valve outputs with choice of coil currents from 10 mA to 120 mA	VSVO
	6	LVDT valve position sensors with on-board excitation	
	2	Active pulse rate probes for flow measurement, with 24 V dc excitation provided	
DVIB	8	Shaft Proximitors/seismic probes (Vib/Displ/Accel)	VVIB
	4	Shaft proximity probes (displacement)	
	1	Shaft proximity reference (Keyphasor)	

Grounding

During panel design, provisions for grounding the terminal board and wiring shields must be made. These connections should be as short as possible. A metal grounding strip can be firmly mounted to the panel on the right hand side of the terminal board. Shields and the SCOM connection can be conveniently made to this strip. Note that only the thermocouple board has screws for the shield wires.

The VME rack is grounded to the mounting panel by the metal-to-metal contact under the mounting screws. No wiring to the ground terminal is required. For more grounding information, refer to *Volume I, Chapter 5*.

Notes

UCV Controller

Controller Overview

The Mark* VI UCV_ controller is a 6U high, single or double slot, single board computer (SBC) that operates the turbine application code. The controller mounts in a VME rack called the control module and communicates with the turbine I/O boards through the VME bus. The controller operating system is QNX[®], a real time, multitasking OS designed for high-speed, high-reliability industrial applications. Three communication ports provide links to operator and engineering interfaces as follows:

- Ethernet connections to the UDH for communication with HMIs, and other control equipment
- RS-232C connection for setup using the COM1 port
- RS-232C connection for communication with distributed control systems (DCS) using the COM2 port (such as Modbus[®] slave)

Operation

The controller is loaded with software specific to its application to steam, gas, and land-marine aeroderivative (LM), or balance of plant (BOP) products. It can execute up to 100,000 rungs or blocks per second, assuming a typical collection of average size blocks. An external clock interrupt permits the controller to synchronize to the clock on the VCM1 communication board to within ± 100 microseconds.

External data is transferred to and from the control system database (CSDB) in the controller over the VME bus by the VCM1 communication board. In a simplex system, the data consists of the process inputs and outputs from the I/O boards. In a TMR system, the data consists of the voted inputs from the input boards, singular inputs from simplex boards, computed outputs to be voted by the output hardware, and the internal state values that must be exchanged between the controllers.

Note Application software can be modified online without requiring a restart.

Controller Versions

Five controller versions are in use:

- The single-slot UCVE is the current generation controller used in most new systems.
- The double-slot UCVF is the high-end current generation controller used in only the systems that require it.
- The single-slot UCVG features performance between the UCVE and the UCVF and may be used as a direct replacement for any previous controller version without necessitating a backplane upgrade.

Note The double-slot UCVB and UCVD are no longer shipped with new systems, but are still in use in older systems.

The UCVE and UCVF may also be used to replace earlier revision controllers, but require a backplane upgrade. If replacing a UCVB, an Ethernet cabling upgrade from 10Base2 to 10Base-T is also required.

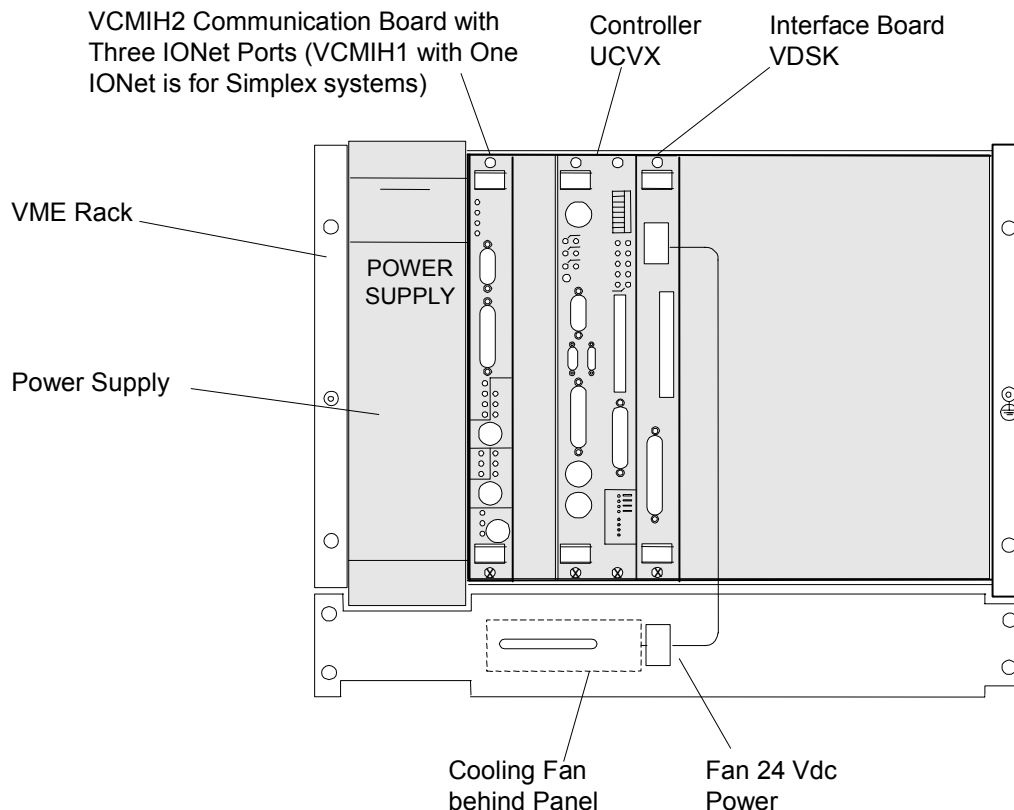
Diagnostics

If a failure occurs in the Mark VI controller while it is running application code, the rotating status LEDs (if supported) on the front panel stop and an internal fault code is generated.

If a failure occurs in the Mark VI controller, a diagnostic alarm is generated that can be read from the toolbox. In the UCVB and UCVD, these diagnostics are also encoded by flashing LEDs on the front panel. The error numbers and descriptions are available on the toolbox help screen. Additional information can also be obtained from the controller COM1 serial port. For further information, refer to *GEH-6421, Vol. I Mark VI System Guide, Chapter 7, Troubleshooting and Diagnostics*.

Installation

A control module contains (at a minimum) the controller and a VCM. Three rack types can be used: the GE Fanuc integrator's rack shown in the following figure and two sizes of Mark VI racks shown in the section, VCM - Bus Master Controller. The GE Fanuc rack is shorter and is used for stand-alone modules with remote I/O only. The Mark VI racks are longer and can be used for local or remote I/O. Whichever rack is used, a cooling fan is mounted either above or below the controller. The stand-alone control module implemented with a GE Fanuc integrator's rack also requires a VDSK board to supply fan power and provide the rack identification through an ID plug.



Typical Controller Mounted in Rack with Communication Board

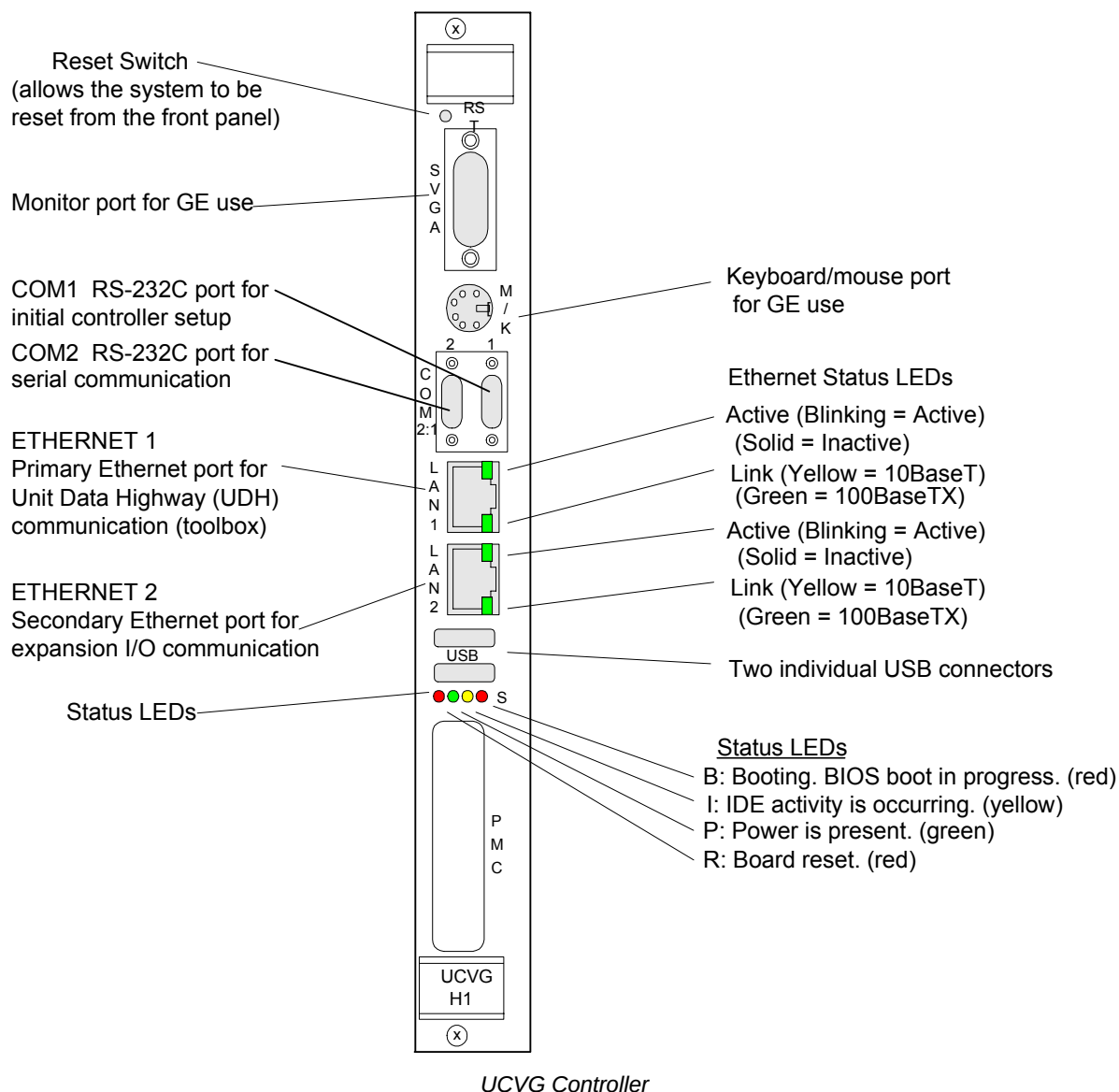
UCVG Controller

The UCVG is a single-slot board using an Intel[®] Ultra Low Voltage Celeron[™] 650 MHz processor with 128 MB of flash memory and 128 MB of SDRAM. Two 10BaseT/100BaseTX (RJ-45 connector) Ethernet ports provide connectivity. The first Ethernet port allows connectivity to the UDH for configuration and peer-to-peer communication.

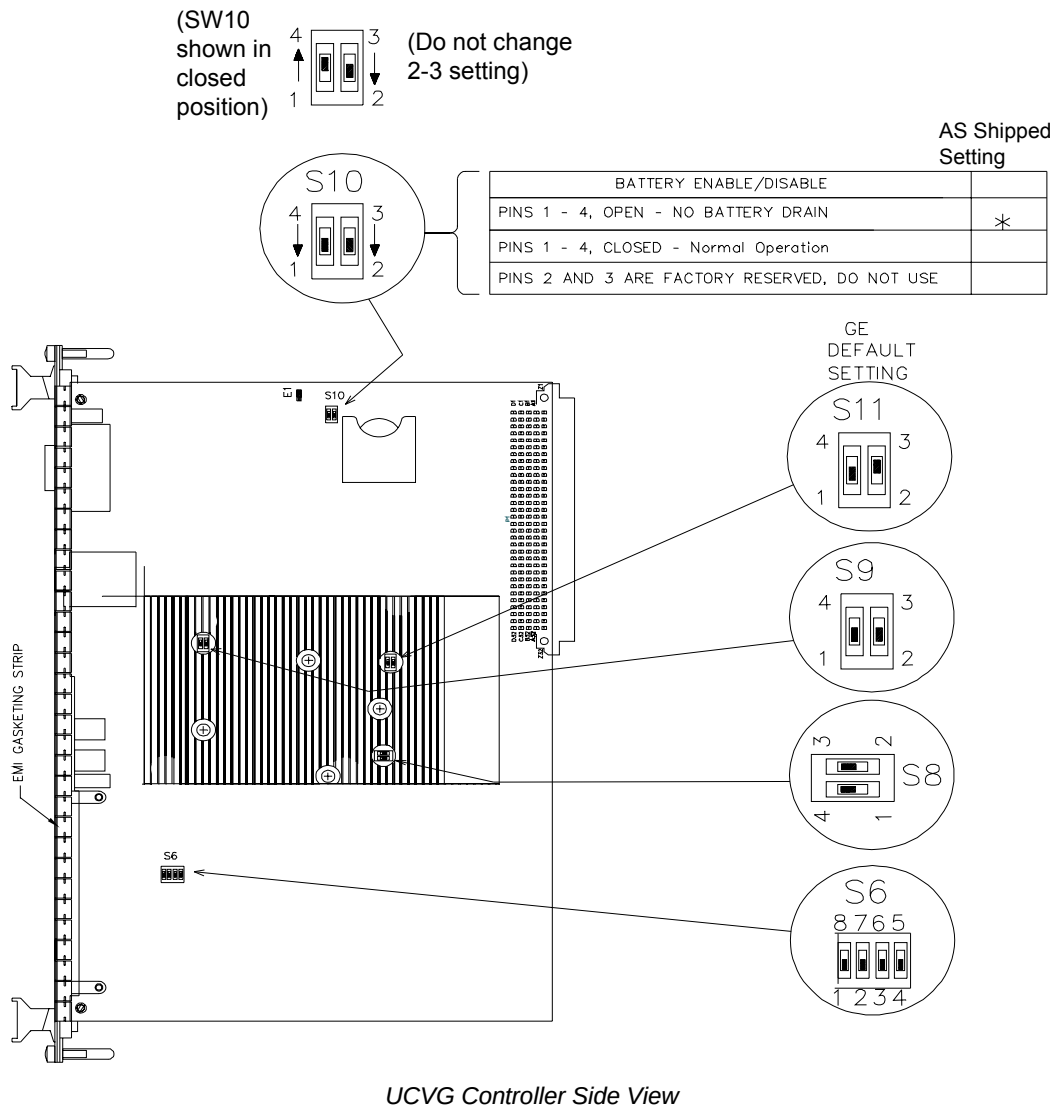
The second Ethernet port is for use on a separate IP logical subnet and can be used for Modbus or private Ethernet Global Data (EGD) network. This Ethernet port is configured through the toolbox. The controller validates its toolbox configuration against the existing hardware each time the rack is powered up.

Note A separate subnet address allows the controller to uniquely identify an Ethernet port. IP subnet addresses are obtained from the Ethernet network administrator (for example, 192.168.1.0, 192.168.2.0).

Mark VI Controller UCVGH1



Note The factory setting of the battery is in the disabled position. To enable the battery, set SW10 to the closed position as shown in the following drawing.



Item	Specification
Microprocessor	Intel Ultra Low Voltage Celeron 650 MHz
Memory	128 MB SDRAM 128 MB Compact Flash Module 256 KB Advanced Transfer Cache
Operating System	QNX
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 32-bit signed integer 32-bit floating point 64-bit long floating point
Primary Ethernet Interface (Ethernet 1)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: TCP/IP protocol used for communication between controller and toolbox EGD protocol for communication with CIMPLICITY [®] HMI, and Series 90-70 programmable logic controllers (PLCs) Ethernet Modbus protocol supported for communication between controller and third-party DCS
Secondary Ethernet Interface (Ethernet 2)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: EGD protocol Ethernet Modbus protocol supported for communication between controller and third-party DCS
COM Ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Used for serial Modbus [®] communication, 9600 or 19200 baud
Power Requirements UCVGH1	+5 V dc, 4 A typical, 5.4 A maximum +12 V dc, less than 1 mA typical - 12 V dc, less than 1 mA typical
Expansion site	PMC expansion site available, IEEE [®] 1386.1 5V PCI
Environment	Operating temperature: 0°C to 70°C (32 °F to 158 °F) Storage temperature: -40°C to 80°C (-40 °F to 176 °F)
Note The UCVG controller contains a Type 1 Lithium battery. Replace only with equivalent battery type, rated 3.3 V, 200 mA.	

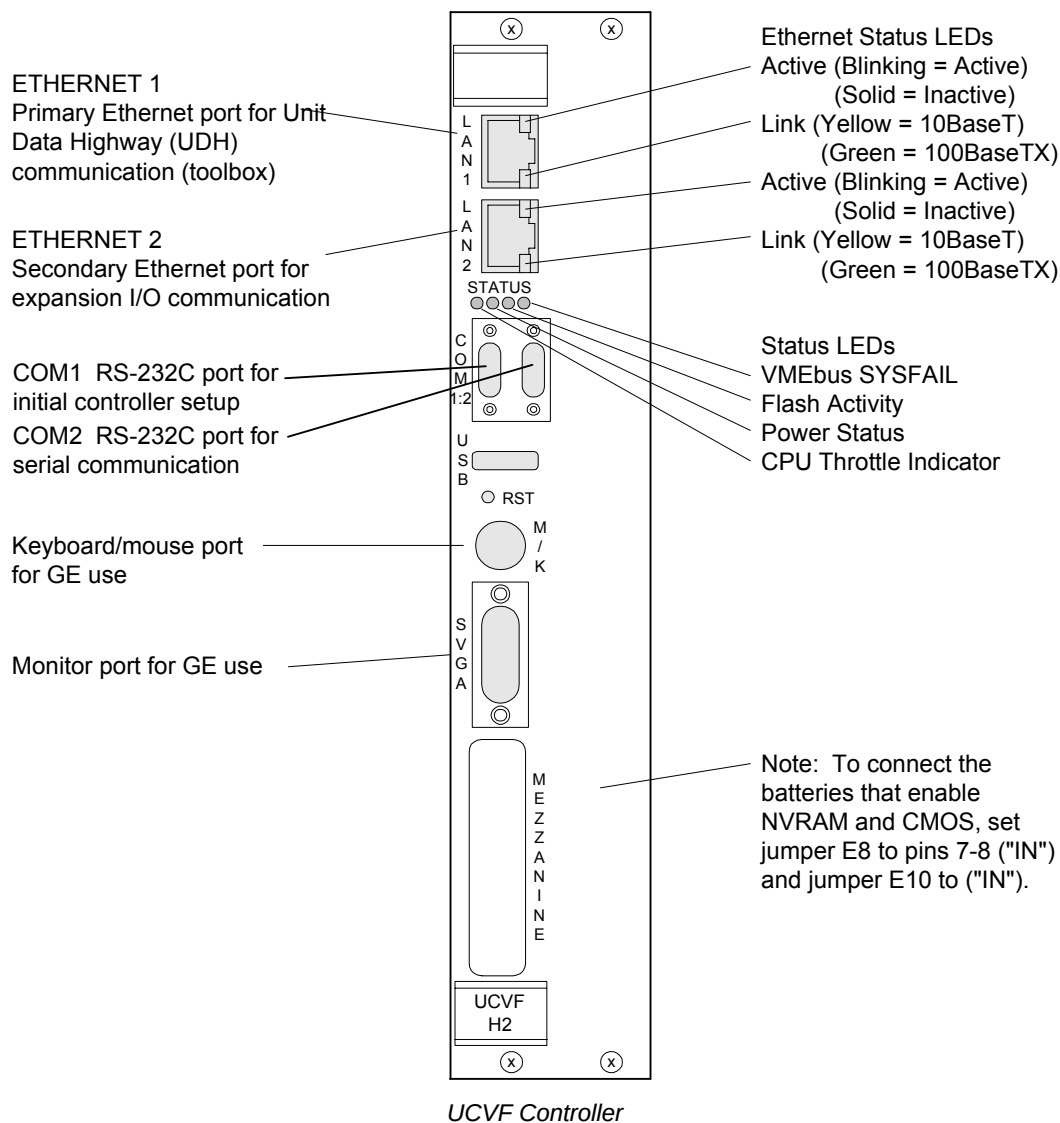
UCVF Controller

The UCVF is a double-slot board using an 850 MHz Intel Pentium[®] III processor with 16 or 128 MB of flash memory and 32 MB of DRAM. Two 10BaseT/100BaseTX (RJ-45 connector) Ethernet ports provide connectivity. The first Ethernet port allows connectivity to the UDH for configuration and peer-to-peer communication.

The second Ethernet port is for use on a separate IP logical subnet. This Ethernet port is configured through the toolbox. The controller validates its toolbox configuration against the existing hardware each time the rack is powered up.

Note A separate subnet address allows the controller to uniquely identify an Ethernet port. IP subnet addresses are obtained from the Ethernet network administrator (for example, 192.168.1.0, 192.168.2.0).

Mark VI Controller UCVFH2



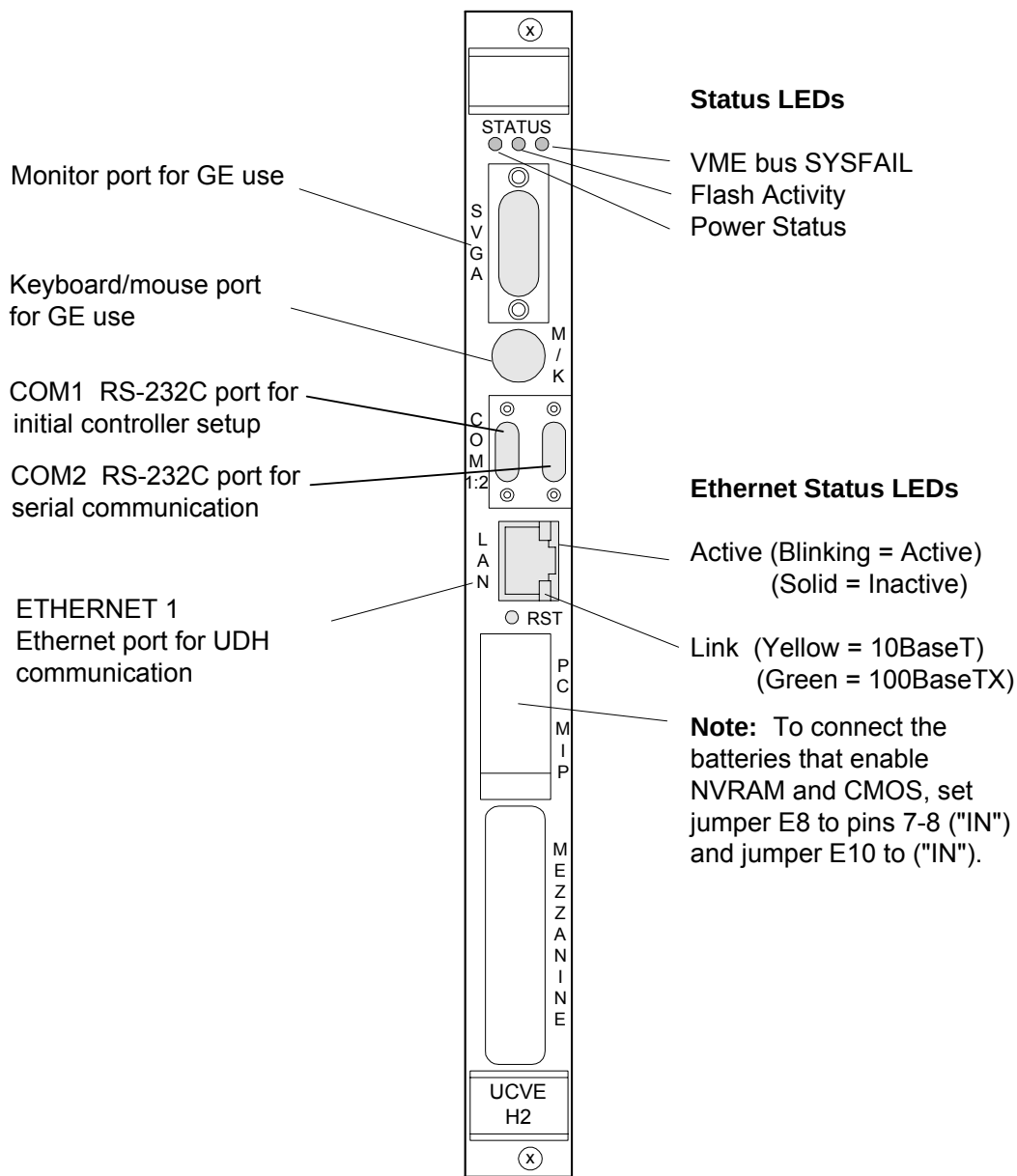
Item	Specification
Microprocessor	Intel Pentium III 850 MHz
Memory	32 MB DRAM 16 or 128 MB Compact Flash Module 256 KB Advanced Transfer Cache Battery-backed SRAM - 8K allocated as NVRAM for controller functions
Operating System	QNX
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 32-bit signed integer 32-bit floating point 64-bit long floating point
Primary Ethernet Interface (Ethernet 1)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: TCP/IP protocol used for communication between controller and toolbox EGD protocol for communication with CIMPLICITY HMI, and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
Secondary Ethernet Interface (Ethernet 2)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: EGD protocol Ethernet Modbus protocol supported for communication between controller and third-party DCS
COM Ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Used for serial Modbus communication, 9600 or 19200 baud
Power Requirements UCVFH2	+5 V dc, 6 A typical, 7 A maximum +12 V dc, 200 mA typical, 400 mA maximum -12 V dc, 2.5 mA typical

UCVE Controllers

The UCVE is available in multiple forms: UCVEH2 and UCVEM01 to UCVMEM05. The UCVEH2 is the standard Mark VI controller. It is a single-slot board using a 300 MHz Intel Celeron processor with 16 or 128 MB of flash memory and 32 MB of DRAM. A single 10BaseT/100BaseTX (RJ-45) Ethernet port provides connectivity to the UDH.

The UCVEM_ _ modules have all the features of the UCVEH2 with the addition of supporting additional Ethernet ports and Profibus. Some UCVEM_ _ modules support secondary 10BaseT/100BaseTX Ethernet ports for use on a separate IP logical subnet. The secondary Ethernet port is configured through the toolbox. The controller validates its toolbox configuration against the existing hardware each time the rack is powered up. A separate subnet address allows the controller to uniquely identify an Ethernet port.

Mark VI Controller UCVEH2



UCVE Controller

UCVE Controller Specifications

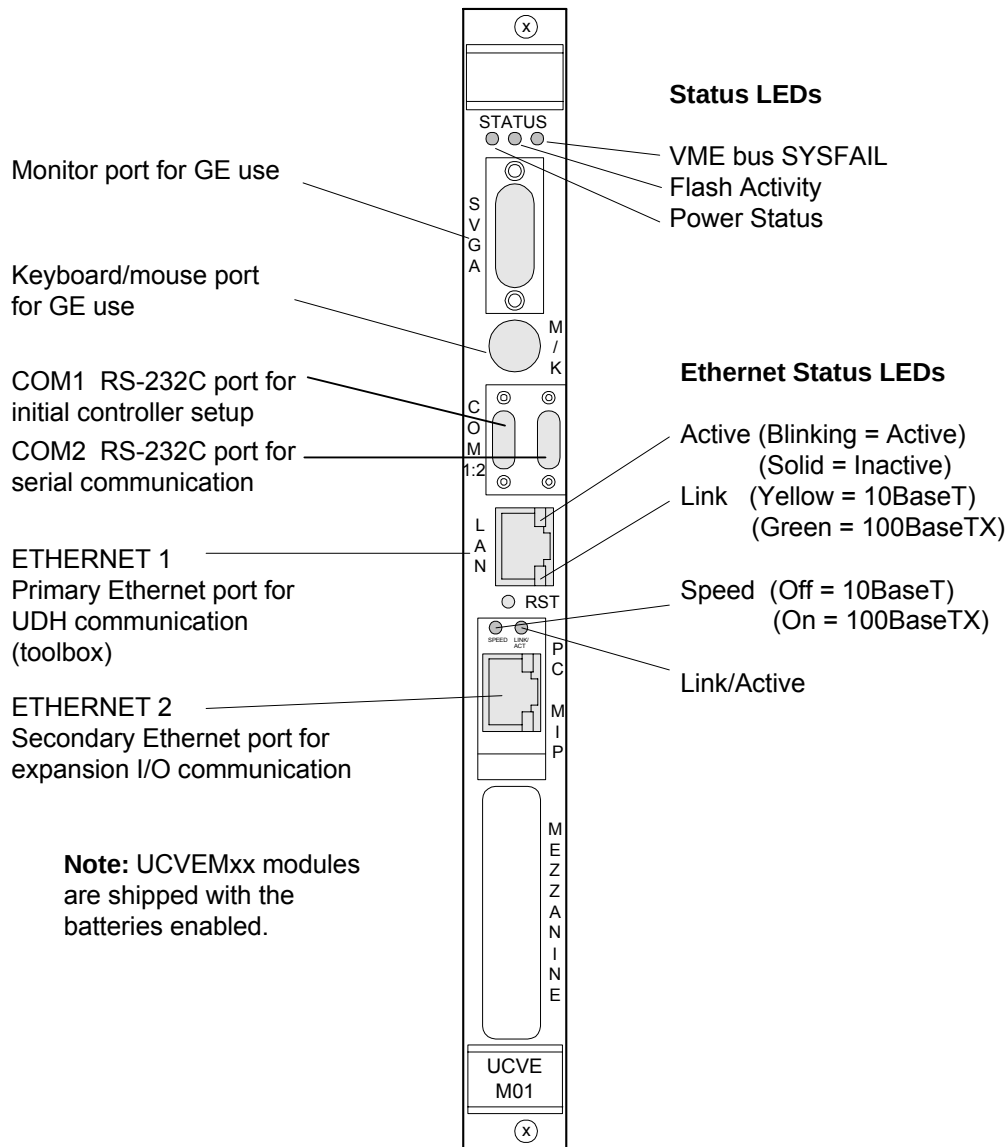
Item	Specification
Microprocessor	Intel Celeron 300 MHz
Memory	32 MB DRAM 16 or 128 MB Compact Flash Module 128 KB L2 cache Battery-backed SRAM - 8K allocated as NVRAM for controller functions
Operating System	QNX
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 32-bit signed integer 32-bit floating point 64-bit long floating point
Primary Ethernet Interface (Ethernet 1)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: TCP/IP protocol used for communication between controller and toolbox EGD protocol for communication with CIMPLICITY HMI and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
COM Ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Used for serial Modbus communication, 9600 or 19200 baud
Power Requirements UCVEH2	+5 V dc, 6 A typical, 8 A maximum +12 V dc, 180 mA typical, 250 mA maximum -12 V dc, 180 mA typical, 250 mA maximum

UCVEM01 Controller Specifications

Item	Specification
Secondary Ethernet Interface (Ethernet 2)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: EGD protocol Ethernet Modbus protocol supported for communication between controller and third party DCS
Power Requirements	+5 V dc, 6.2 A typical, 8.2 A maximum +12 V dc, 180 mA typical, 250 mA maximum -12 V dc, 180 mA typical, 250 mA maximum

Note For specifications common to all UCVE modules, refer to *UCVEH2 Controller Specifications*.

Mark VI Controller UCVEM01



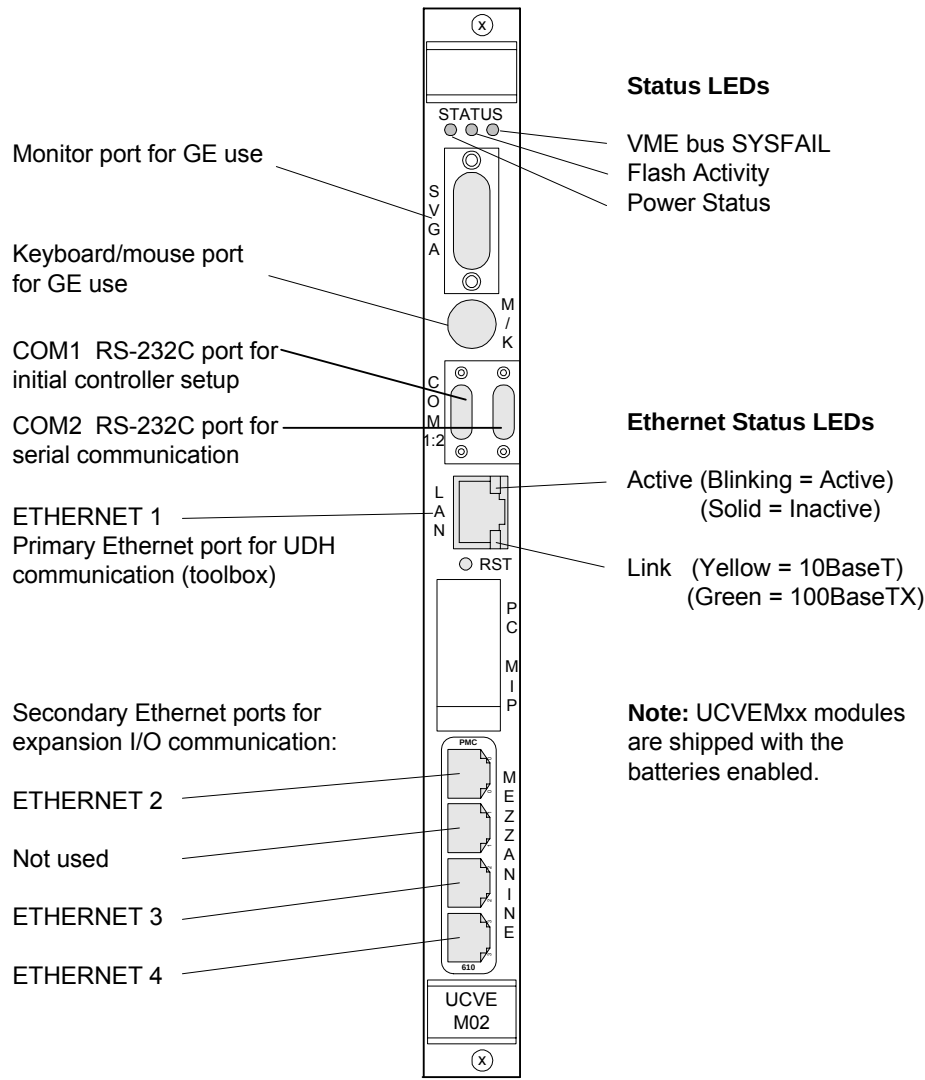
UCVEM01 Front Panel

UCVEM02 Controller Specifications

Item	Specification
Secondary Ethernet Interfaces (Ethernet 2-4)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: EGD protocol Ethernet Modbus protocol supported for communication between controller and third-party DCS
Power Requirements	+5 V dc, 8.3 A typical, 10.3 A maximum +12 V dc, 180 mA typical, 250 mA maximum -12 V dc, 180 mA typical, 250 mA maximum

Note For specifications common to all UCVE modules, refer to *UCVEH2 Controller Specifications*.

Mark VI Controller UCVEM02



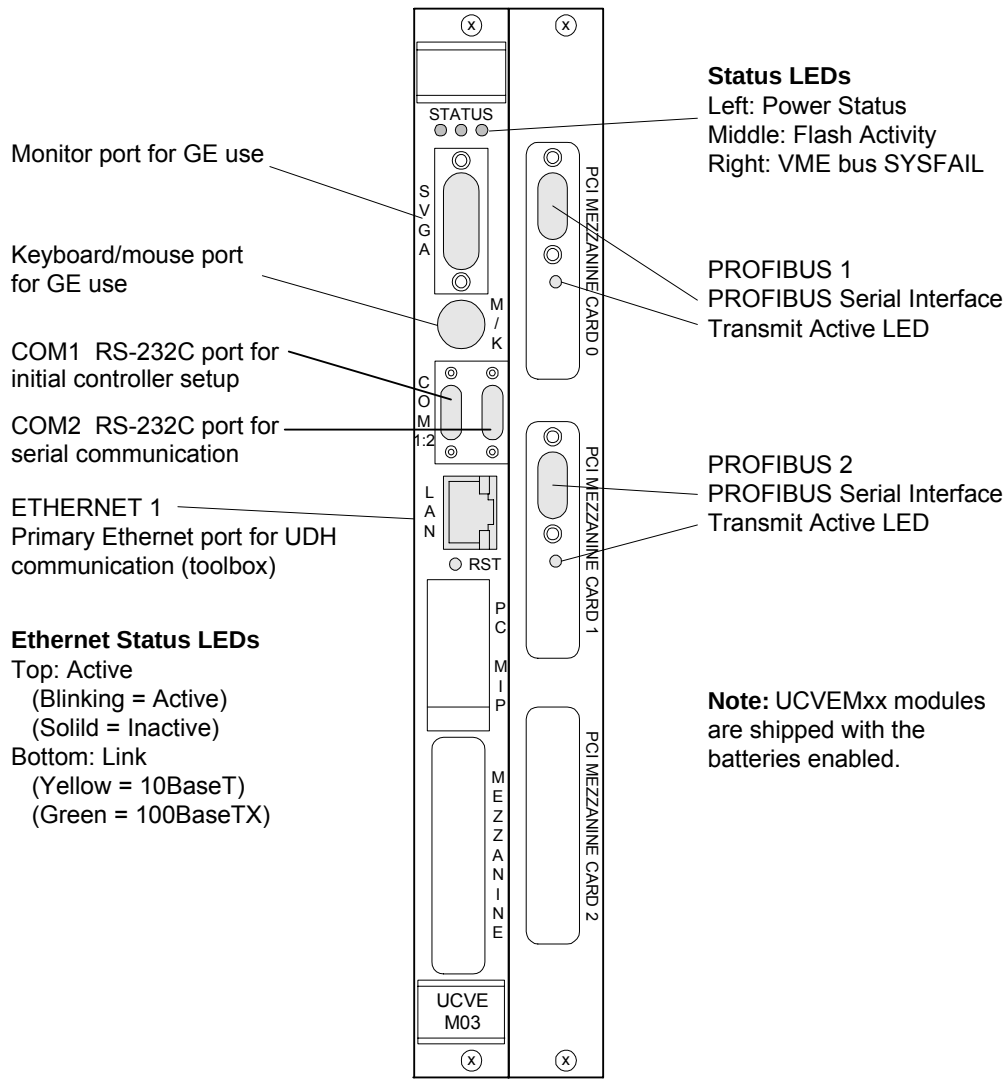
UCVEM02 Front Panel

UCVEM03 Controller Specifications

Item	Specification
PROFIBUS Interface (PROFIBUS 1-2)	PROFIBUS DP master class 1
Power Requirements	+5 V dc, 8.2 A typical, 10.2 A maximum
	+12 V dc, 180 mA typical, 250 mA maximum
	-12 V dc, 180 mA typical, 250 mA maximum

Note For specifications common to all UCVE modules, refer to *UCVEH2 Controller Specifications*.

Mark VI Controller UCVEM03



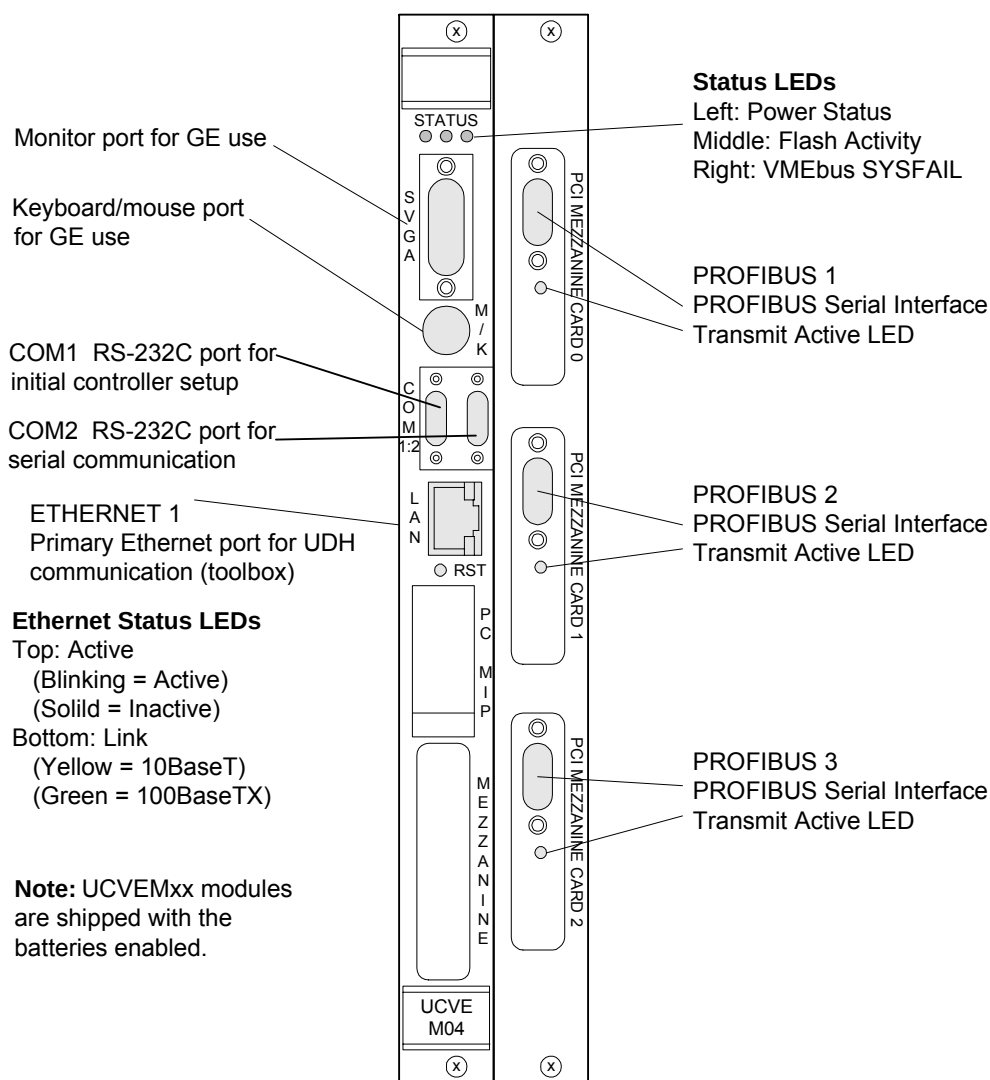
UCVEM03 Front Panel

UCVEM04 Controller Specifications

Item	Specification
PROFIBUS Interface (PROFIBUS 1-3)	PROFIBUS DP master class 1
Power Requirements	+5 V dc, 9.2 A typical, 11.2 A maximum +12 V dc, 180 mA typical, 250 mA maximum -12 V dc, 180 mA typical, 250 mA maximum

Note For specifications common to all UCVE modules, refer to *UCVEH2 Controller Specifications*.

Mark VI Controller UCVEM04



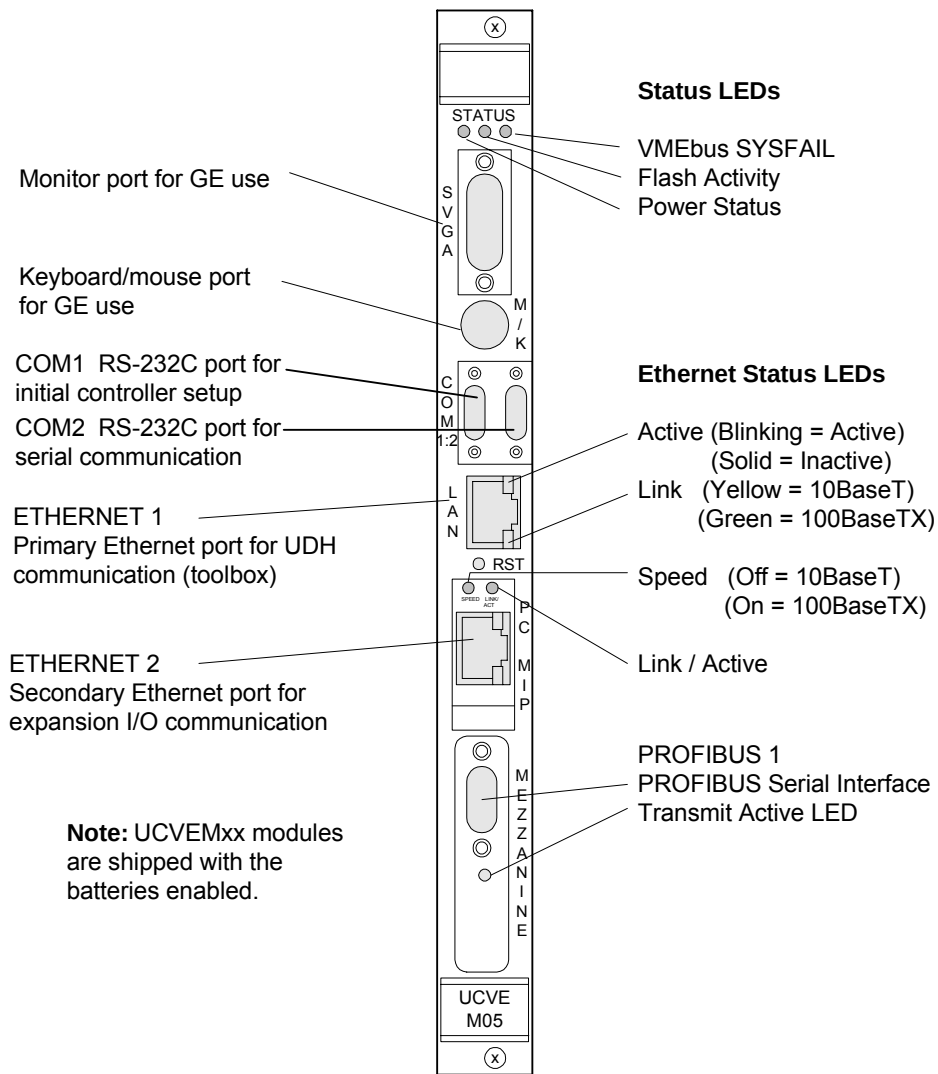
UCVEM04 Front Panel

UCVEM05 Controller Specifications

Item	Specification
Secondary Ethernet Interface (Ethernet 2)	Twisted pair 10BaseT/100BaseTX, RJ-45 connector: EGD protocol Ethernet Modbus protocol supported for communication between controller and third-party DCS
PROFIBUS Interface (PROFIBUS 1)	PROFIBUS DP master class 1
Power Requirements	+5 V dc, 7.2 A typical, 9.2 A maximum +12 V dc, 180 mA typical, 250 mA maximum -12 V dc, 180 mA typical, 250 mA maximum

Note For specifications common to all UCVE modules, refer to *UCVEH2 Controller Specifications*.

Mark VI Controller UCVEM05



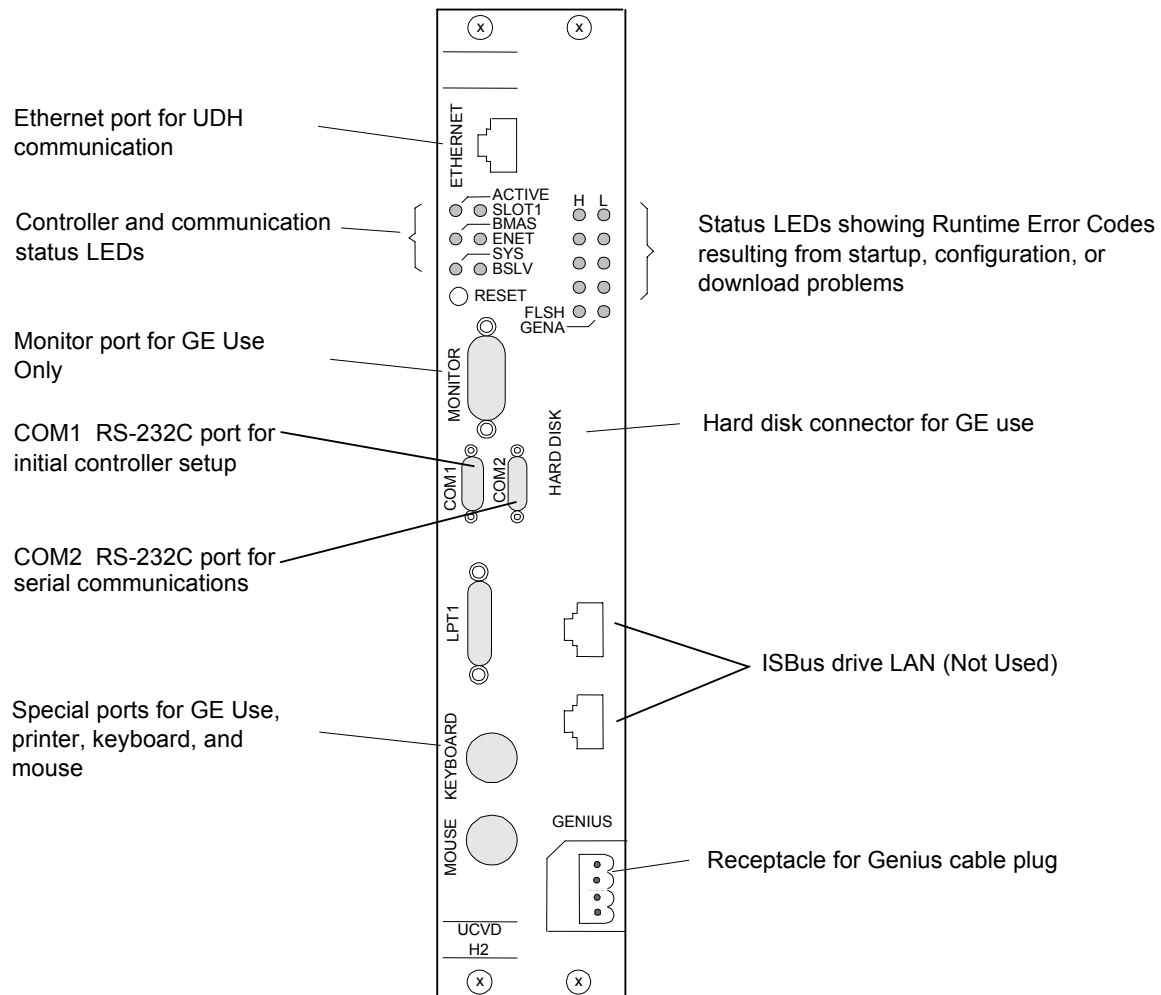
UCVEM05 Front Panel

UCVD Controller

The UCVD is a double-slot board using a 300 MHz AMD K6 processor with 8 MB of flash memory and 16 MB of DRAM. A single 10BaseT (RJ-45 connector) Ethernet port provides connectivity to the UDH.

The UCVD contains a double column of eight status LEDs. These LEDs are sequentially turned on in a rotating pattern when the controller is operating normally. When an error condition occurs, the LEDs display a flashing error code that identifies the problem. For more information, refer to *GEH-6410, Innovation Series Controller System Manual*.

Mark VI Controller UCVDH1, H2



UCVD Controller Front Panel

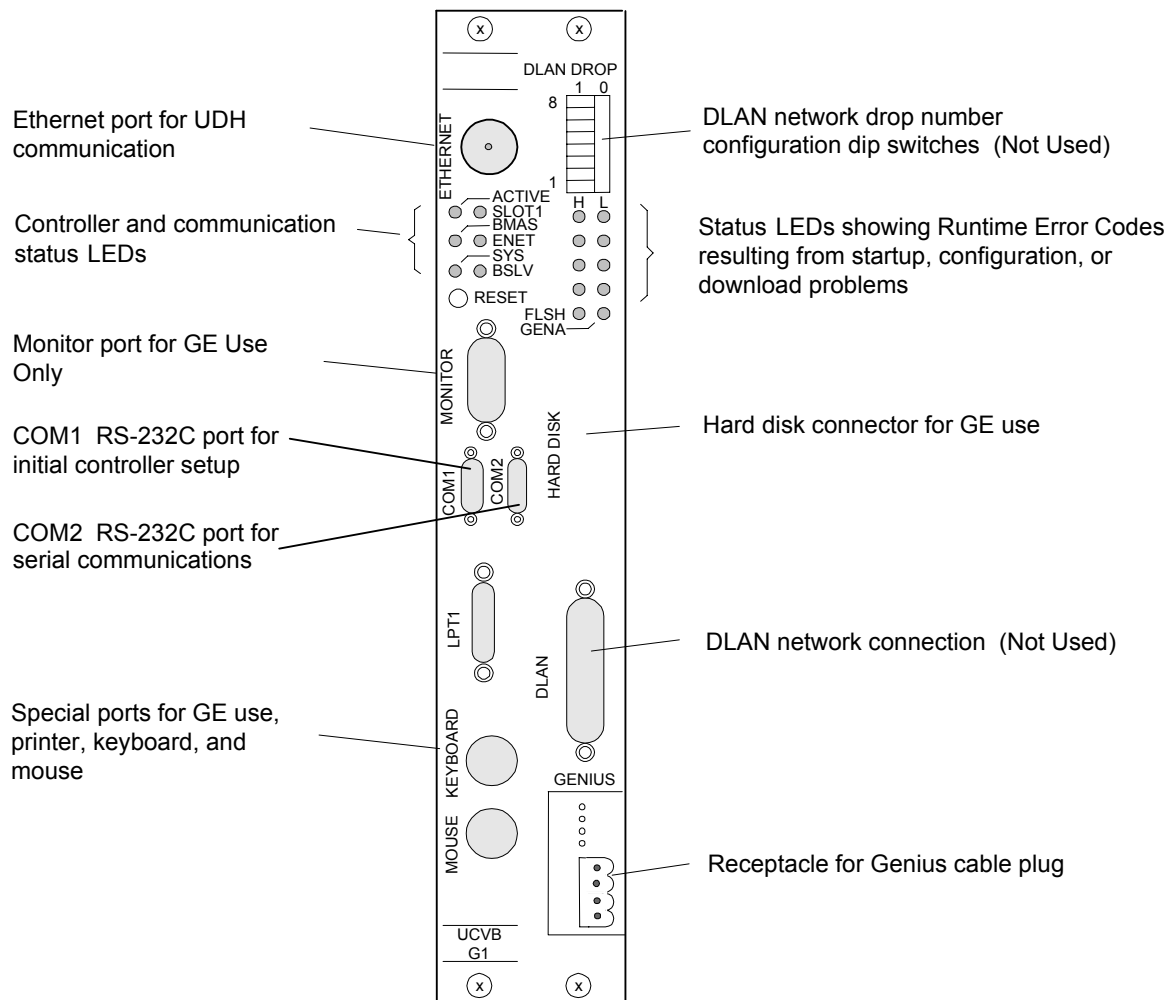
Item	Specification
Microprocessor	AMD-K6 300 MHz
Memory	16 MB DRAM 8 MB Flash Memory in UCVD 256 KB of level 2 cache
Operating System	QNX
LEDs	LEDs on the faceplate provide status information as follows: ACTIVE Processor is active SLOT 1 Controller configured as slot 1 controller in VME rack BMAS VME master access is occurring ENET Ethernet activity BSLV VME slave access is occurring STATUS Display rotating LED pattern when OK Display flashing error code when faulted FLSH Writing to Flash memory GENX Genius I/O is active
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 32-bit signed integer 32-bit floating point 64-bit floating point
Ethernet Interface	Twisted pair 10BaseT, RJ-45 connector TCP/IP protocol used for communication between controller and toolbox Serial Request Transfer Protocol (SRTP) interface between controller and HMI EGD protocol for communication with CIMPLICITY HMI, and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
COM Ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Used for serial Modbus communication, 9600 or 19200 baud
Power Requirements	+5 V dc, 6 A +12 V dc, 200 mA -12 V dc, 200 mA

UCVB Controller

The UCVB is a double-slot board using a 133 MHz Intel Pentium processor with 4 MB of flash memory and 16 MB of DRAM. A single 10Base2 (BNC connector) Ethernet port provides connectivity to the UDH.

The UCVB contains a double column of eight status LEDs. These LEDs are sequentially turned on in a rotating pattern when the controller is operating normally. When an error condition occurs, the LEDs display a flashing error code that identifies the problem. For more information, refer to *GEH-6410, Innovation Series Controller System Manual*.

Mark VI Controller UCVBG1



UCVB Controller Front Panel

Item	Specification
Microprocessor	Intel Pentium 133 MHz
Memory	16 MB DRAM 4 MB Flash Memory in UCVB 256 KB of level 2 cache
Operating System	QNX
LEDs	LEDs on the faceplate provide status information as follows: ACTIVE Processor is active SLOT 1 Controller configured as slot 1 controller in VME rack BMAS VME master access is occurring ENET Ethernet activity BSLV VME slave access is occurring STATUS Display rotating LED pattern when OK Display flashing error code when faulted FLSH Writing to Flash memory GENX Genius I/O is active
Programming	Control block language with analog and discrete blocks; Boolean logic represented in relay ladder diagram format. Supported data types include: Boolean 16-bit signed integer 32-bit signed integer 32-bit floating point 64-bit long floating point
Ethernet Interface	Thinwire™ 10Base2, BNC connector: TCP/IP protocol used for communication between controller and toolbox SRTP interface between controller and HMI EGD protocol for communication with CIMPLICITY HMI, and Series 90-70 PLCs Ethernet Modbus protocol supported for communication between controller and third-party DCS
COM Ports	Two micro-miniature 9-pin D connectors: COM1 Reserved for diagnostics, 9600 baud, 8 data bits, no parity, 1 stop bit COM2 Used for serial Modbus communication, 9600 or 19200 baud
DLAN+ Interface	Interface to DLAN+, a high speed multidrop network based on ARCNET®, using a token passing, peer to peer protocol
Power Requirements	+5 V dc, 5.64 A +12 V dc, 900 mA -12 V dc, 200 mA

Alarms

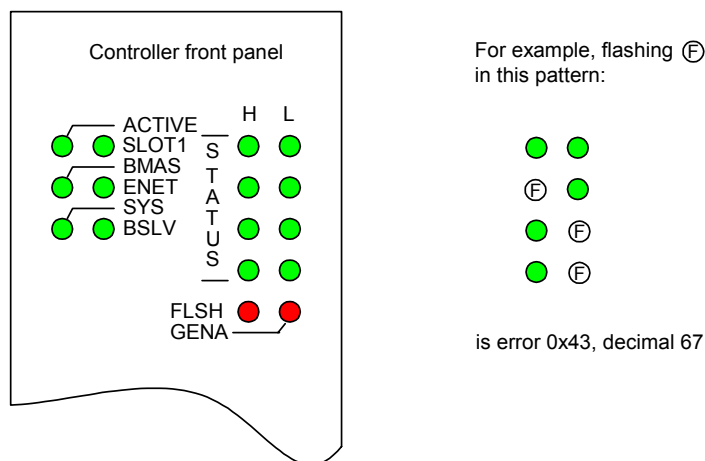
Fault	Fault Description	Possible Cause
31	I/O Compatibility Code Mismatch	Outdated configuration in the VCM
32	Diagnostic Queue Overflow	Too many diagnostics are occurring simultaneously
33	Foreground Process	Outdated runtime version
34	Background Process	Outdated runtime version
37	Idle Process	Outdated runtime version
38	Ambient Air Overt temperature Warning. The rack is beginning to overheat.	The rack fan has failed or the filters are clogged.
39	CPU Over temperature Fault. The controller CPU has overheated and may fail at any time.	The rack fan has failed or the filters are clogged.
40	Genius I/O Driver Process	Outdated runtime version
41	Register I/O Process	Outdated runtime version
42	Modbus Driver Process	Outdated runtime version
43	Ser Process	Outdated runtime version
44	Rcvr Process	Outdated runtime version
45	Trans Process	Outdated runtime version
46	Mapper Process	Outdated runtime version
47	SRTTP Process	Outdated runtime version
48	Heartbeat Process	Outdated runtime version
49	Alarm Process	Outdated runtime version
50	Queue Manager Process	Outdated runtime version
51	EGD Driver Process	Outdated runtime version
52	ADL Dispatcher Process	Outdated runtime version
53	ADL Queue Process	Outdated runtime version
54	DPM Manager Process	Outdated runtime version
68	Genius IOCHRDY Hangup	Outdated runtime version
70	Genius Lock Retry	Outdated runtime version
71	Genius	Outdated runtime version
72	Application Code Online Load Failure	Application code error
74	Application Code Startup Load Failure	Application code error
75	Application Code Expansion Failure	Application code error
76	ADL/BMS Communication Failure with the VCM	The VCM firmware version is too old to work with this controller runtime version.
77	NTP Process	Outdated runtime version
78	Outdated Controller Topology	Download application code and reboot
79	Outdated VCM Topology	Download configuration to VCM and reboot
80	No VCM Topology	Old VCM firmware doesn't support controller/VCM topology checking. Upgrade VCM firmware.
81	Platform Process	Outdated runtime version
82	Hardware Configuration Error	The controller hardware doesn't match the configuration specified by the toolbox. Use the toolbox to view the errors in the controller trace buffer (for example: View General Dump the trace buffer).
83	Register I/O Write/Command Limit Exceeded	Verify that the total command rate of all Modbus interfaces does not exceed the maximum.
84	State Exchange Voter Packet Mismatch	Verify that all three controllers are executing the same application code.
85	Maximum Number of Boolean State Variables Exceeded	The application code is using too many Boolean variables. Move some functions to other controllers.

Fault	Fault Description	Possible Cause
86	Too Many EGD Producers Configured for Fault Tolerant Support	The controller can redirect data over the IONET from a maximum of 16 EGD producers. Data from subsequent producers will be lost in the event of an Ethernet failure.
87	Too Many EGD Points Configured for Fault Tolerant Support	The controller can redirect a maximum of 1400 bytes of data over the IONET. Subsequent EGD points will be lost in the event of an Ethernet failure.
88	Producing Fault Tolerant EGD Data	The controller is redirecting data from the Ethernet to another controller over the IONET.
89	Requesting Fault Tolerant EGD Data	The controller is requesting that Ethernet data be redirected to it over the IONET from another controller.
90	Process Alarm Queue Is Full	Subsequent process alarms will be lost unless the current alarms are acknowledged and cleared by the operator.
91	Hold List Queue Is Full	Subsequent hold alarms will be lost unless the current alarms are acknowledged and cleared by the operator.
92	Data Initialization Failure	Verify that all controllers are executing the same application code. If no VCMI is used (simulation mode), verify that the clock source is set to internal. If a VCMI is used, verify that the clock source is set to external.
93	Pcode mismatch between TMR controllers	Download the same application code to all three controllers
94	Unable to start up Dynamic Data Recorder	Outdated runtime version - download runtime and restart.
95	Dynamic Data Recorder Configuration Fault	Revalidate the application code and then select the Update Dynamic Data Recorder button from the toolbox toolbar
96	Dynamic Data Recorder Process	Outdated runtime version - download runtime and restart

UCV Board UCVD Controller Runtime Errors

In addition to generating diagnostic alarms, the UCVB and the UCVD controller boards display status information on front panel LEDs. The Status LED group on these controllers contains eight segments in a two vertical column layout as shown in the following figure. These LEDs display controller errors if a problem occurs. The right-most column makes up the lower hexadecimal digit and the left-most column makes up the upper digit (the least significant bits on the bottom). Numerical conversions are provided with the fault code definitions.

Note For all controllers, refer to the stats line in the toolbox.



Flashing Controller Status LEDs Indicate Error Codes

If the controller detects certain system errors (typically during boot-up or download), it displays flashing and non-flashing codes on these green status LEDs. These codes correspond to runtime errors listed in the toolbox help file. The following table describes the types of errors displayed by the LEDs.

Controller Runtime Errors

Controller Condition	Status LED Display
Controller successfully completes its boot-up sequence and begins to execute application code	Displays a <i>walking ones</i> pattern consisting of a single lighted green LED rotating through the bank of LEDs.
Error occurs during the BIOS phase of the boot-up sequence	Non-flashing error code is displayed
Error occurs during the application code load	Flashing error codes are displayed until the error has been corrected and either the application code is downloaded again, or the controller is rebooted.
Error occurs while the controller is running	May freeze with only a single LED lighted. No useful information can be interpreted from the LED position. Fault codes are generated internally.

Notes

VAIC Analog Input/Output

VAIC Analog Input/Output

Functional Description

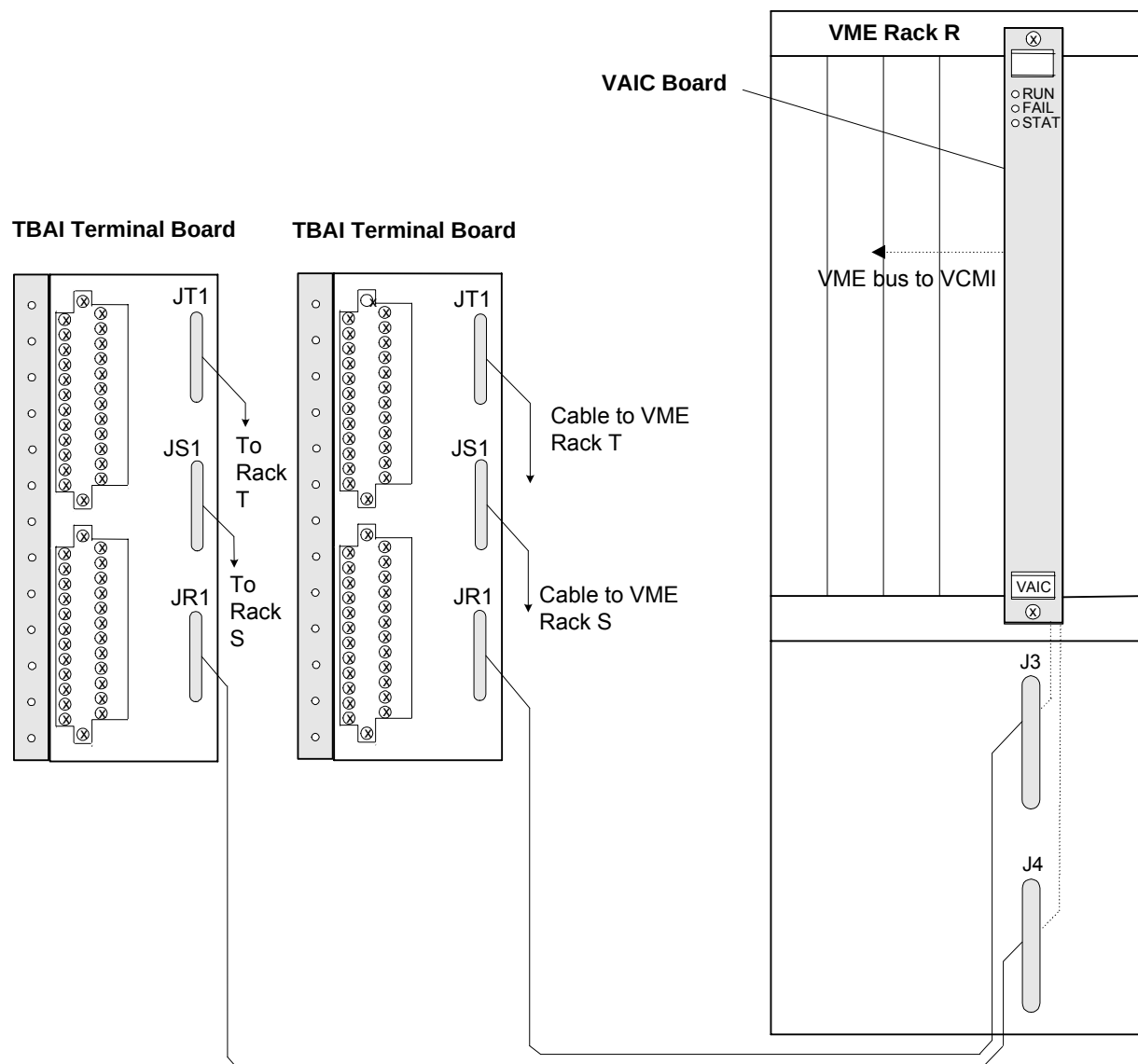
The Analog Input/Output (VAIC) board accepts 20 analog inputs and controls 4 analog outputs. Each terminal board accepts 10 inputs and 2 outputs. Cables connect the terminal board to the VME rack where the VAIC processor board is located. VAIC converts the inputs to digital values and transfers them over the VME backplane to the VCMI board, and then to the controller. For outputs, the VAIC converts digital values to analog currents and drives these through the terminal board into the customer circuit.

VAIC supports both simplex and triple modular redundant (TMR) applications. When used in a TMR configuration, input signals on the terminal board are fanned out to three VME board racks R, S, and T, each containing a VAIC. Output signals are driven with a proprietary circuit that creates the desired current using all three VAICs. In the event of a hardware failure, the bad VAIC is removed from the output and the remaining two boards continue to produce the correct current. When used in a simplex configuration, the terminal board provides input signals to a single VAIC, which provides all of the current for outputs.

Compatibility

There are two generations of the VAIC board with corresponding terminal boards. The original VAIC includes all versions prior to and including VAICH1C. VAICH1B is included in this generation. When driving 20 mA outputs these boards support up to 500 Ω load resistance at the end of 1000 ft of #18 wire. This generation of board requires terminal board TBAIH1B or earlier for proper operation. They also work properly with all revisions of DTAI terminal boards.

The newest VAICH1D and any subsequent releases are designed to support higher load resistance for 20 mA outputs drive voltage: up to 18 V is available at the terminal board screw terminals. This permits operation into loads of 800 Ω with 1000 ft of #18 wire with margin. This generation of the board requires TBAIH1C or later, or any revision of STAI.



VAIC, Analog Input Terminal Boards, and Cabling (TMR System)

Installation

➤ To install the V-type board

- 1 Power down the VME processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel

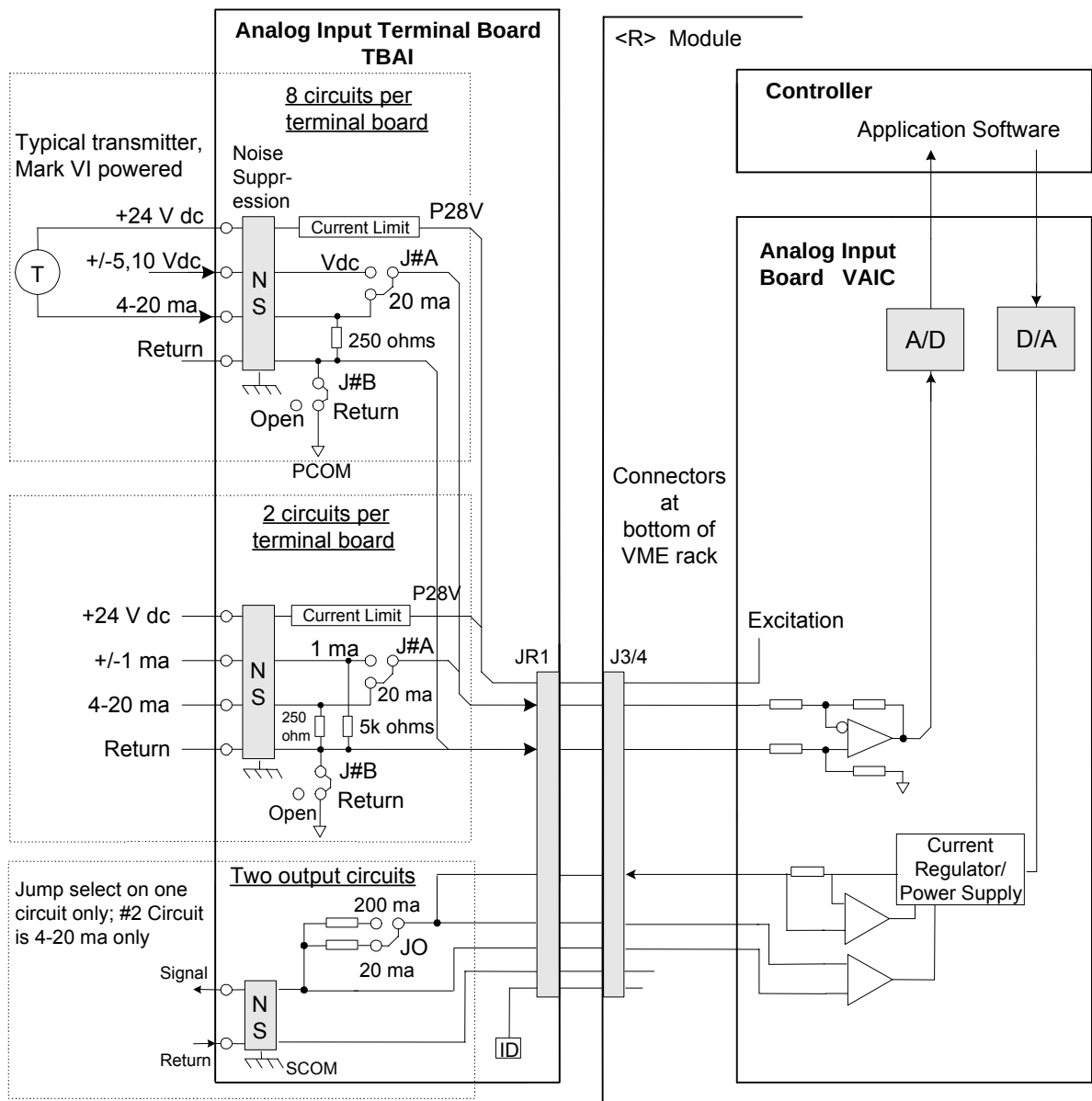
Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the section on diagnostics in this document.

Operation

The VAIC board accepts 20 analog inputs, controls 4 analog outputs, and contains signal conditioning, an analog MUX, A/D converter, and D/A converter. The type of analog input, either voltage, 4-20 mA, or ± 1 mA, is selected by jumpers on the terminal board. Two of the four analog output circuits are 4-20 mA and the other two can be configured for 4-20 mA or 0-200 mA. Inputs and outputs have noise suppression circuitry to protect against surge and high frequency noise.

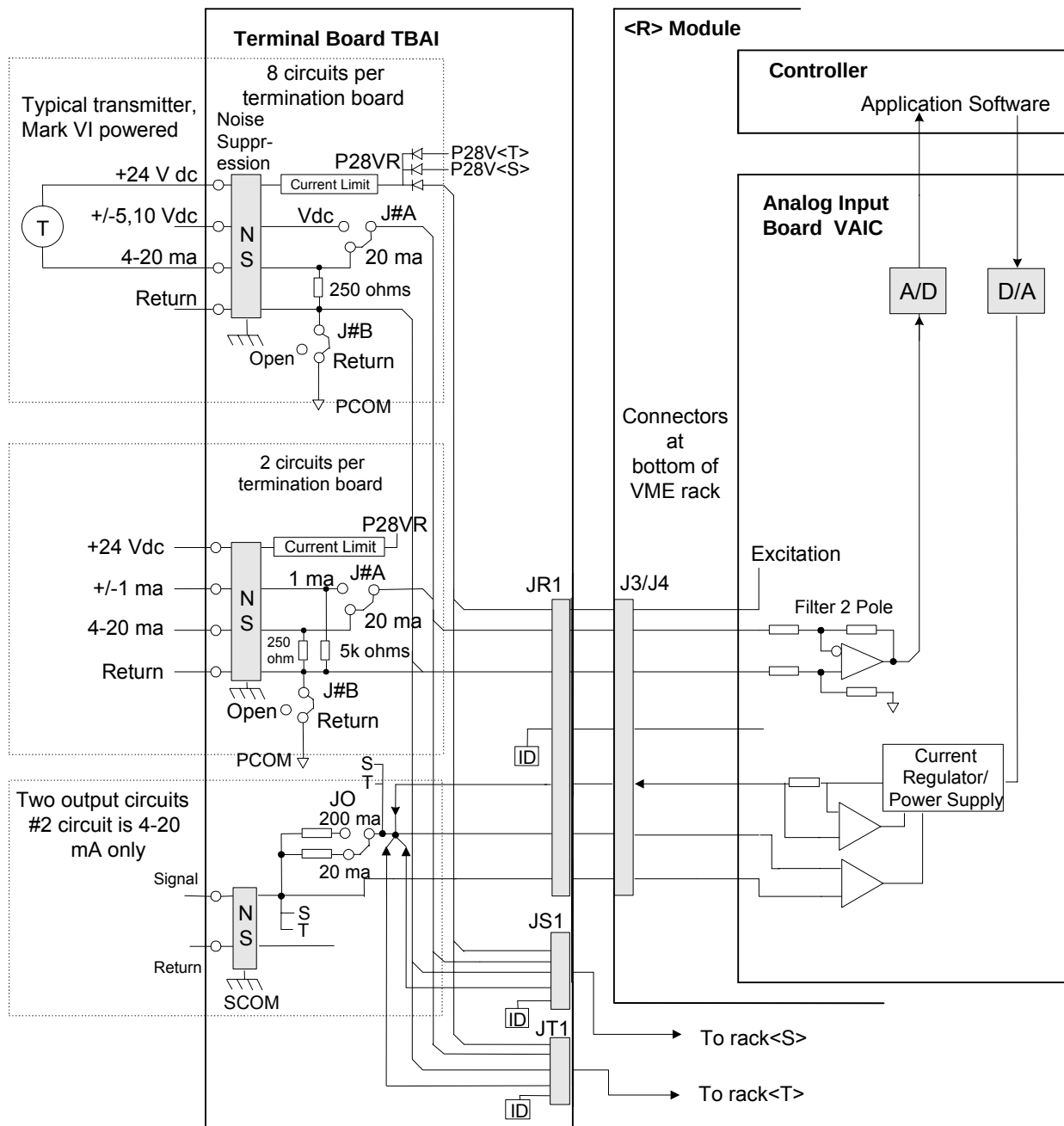
The following table displays the analog I/O capacity of VAIC, using two TBAI terminal boards.

Quantity	Analog Input Types	Quantity	Analog Output Types
16	± 10 V dc, or ± 5 V dc, or 4-20 mA	2	0-20 mA or 0-200 mA
4	4-20 mA, or ± 1 mA	2	0-20 mA



VAIC and Analog Input Terminal Board, Simplex System

In a TMR system, analog inputs fan out to the three control racks from JR1, JS1, and JT1. The 24 V dc power to the transducers comes from all three VME racks and is diode OR selected on the terminal board. Each analog current output is fed by currents from all three VAICs. The actual output current is measured with a series resistor, which feeds a voltage back to each VAIC. The resulting output is the voted middle value (median) of the three currents. The following figure shows VAIC in a TMR arrangement.



VAIC and Analog Input Terminal Board, TMR System

Note With the noise suppression and filtering, the input ac common mode rejection (CMR) is 60 dB, and the dc CMR is 80 dB.

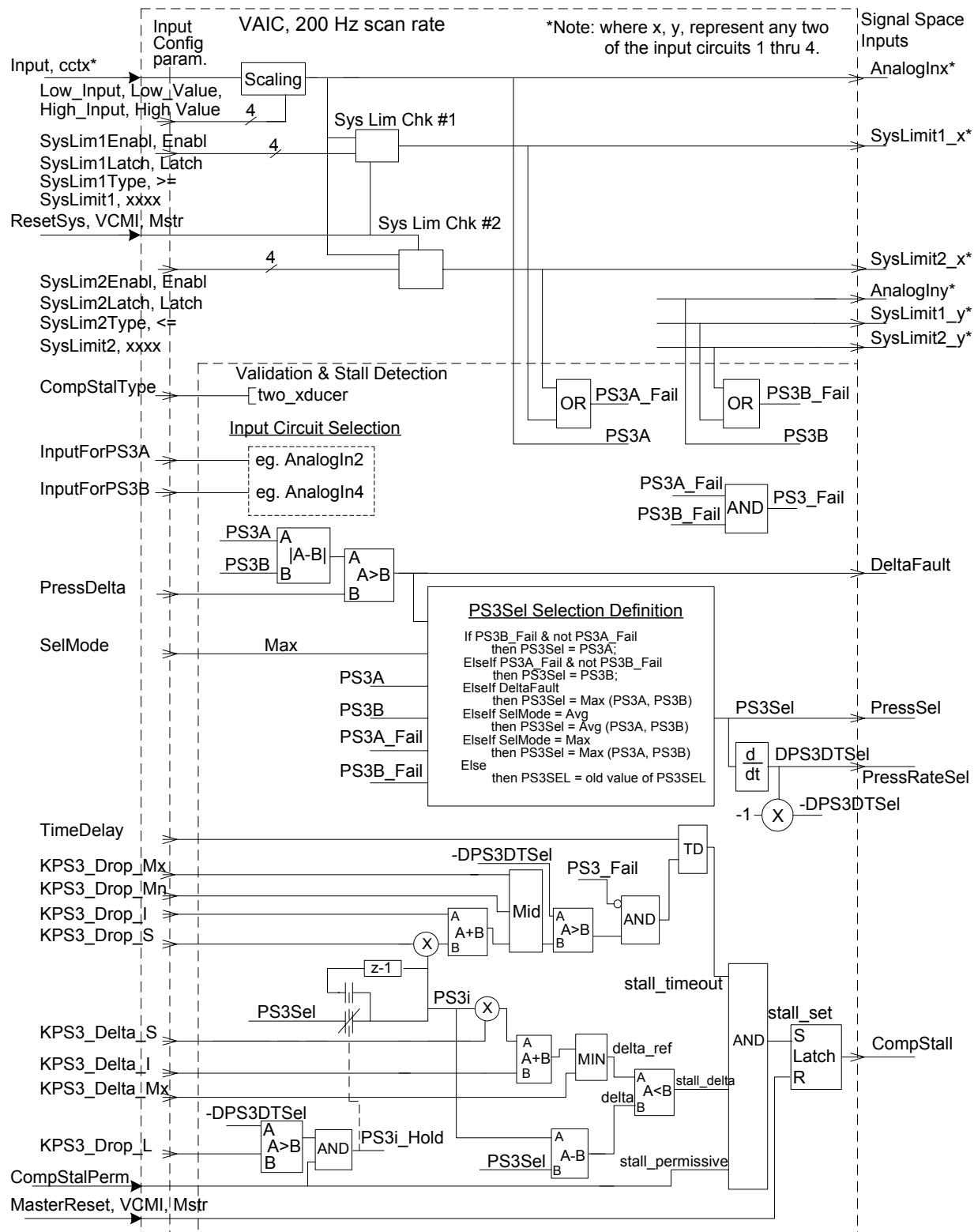
Transmitters/transducers can be powered by the 24 V dc source in the control system, or can be powered independently. Diagnostics monitor each output and a suicide relay disconnects the corresponding output if a fault cannot be cleared by a command from the processor. Hardware filters on the terminal board suppress high frequency noise. Additional software filters on VAIC provide configurable low pass filtering.

Compressor Stall Detection

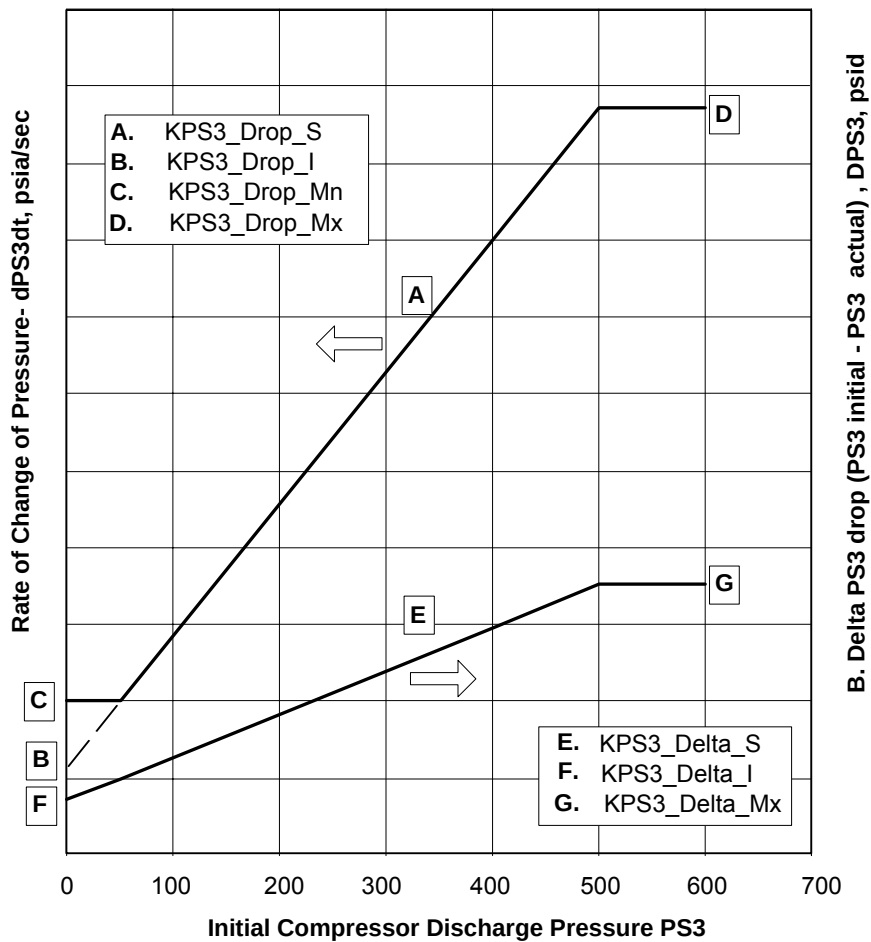
VAIC firmware includes gas turbine compressor stall detection, executed at 200 Hz. Two stall algorithms can be selected. Both use the first four analog inputs, scanned at 200 Hz. One algorithm is for small LM gas turbines and uses two pressure transducers (refer to the figure, *Small (LM) Gas Turbine Compressor Stall Detection Algorithm*). The other algorithm is for heavy-duty gas turbines and uses three pressure transducers (refer to the figure, *Heavy Duty Gas Turbine Compressor Stall Detection Algorithm*).

Real-time inputs are separated from the configured parameters for clarity. The parameter CompStalType selects the type of algorithm required, either two transducers or three. PS3 is the compressor discharge pressure. A drop in this pressure (PS3 drop) indicates possible compressor stall. The algorithm also calculates the rate of change of discharge pressure, dPS3dt, and compares these values with configured stall parameters (KPS3 constants).

The compressor stall trip is initiated by VAIC, which sends the signal to the controller where it is used to initiate a shutdown. The shutdown signal can be used to set all the fuel shut-off valves (FSOV) through any relay output.



Small (LM) Gas Turbine Compressor Stall Detection Algorithm



Configurable Compressor Stall Detection Parameters

The variables used by the stall detection algorithm are defined as follows:

Variable	Variable Description
PS3	Compressor discharge pressure
PS3I	Initial PS3
KPS3_Drop_S	Slope of line for PS3I versus dPS3dt
KPS3_Drop_I	Intercept of line for PS3I versus dPS3dt
KPS3_Drop_Mn	Minimum value for PS3I versus dPS3dt
KPS3_Drop_Mx	Maximum value for PS3I versus dPS3dt
KPS3_Delta_S	Slope of line for PS3I versus Delta PS3 drop
KPS3_Delta_I	Intercept of line for PS3I versus Delta PS3 drop
KPS3_Delta_Mx	Maximum value for PS3I versus Delta PS3 drop

Specifications

Item	Specification
Number of channels	24 channels per VAIC board (20 AI, 4 AO) with two terminal boards
Input span	4-20 mA, ± 1 mA, ± 5 V dc, ± 10 V dc
Input Impedance	250 Ω at 4-20 mA 5,000 Ω at 1 mA 500,00 Ω at voltage input
Input converter resolution	16-bit A/D converter with 14-bit resolution
Scan time	Normal scan 10 ms (100 Hz) Inputs 1 through 4 available for scan at 200 Hz
Measurement accuracy	Better than 0.1% full scale
Noise suppression on inputs	The first 10 circuits (J3) have a hardware filter with single pole down break at 500 rad/sec The second 10 circuits (J4) have a hardware filter with a two pole down break at 72 and 500 rad/sec A software filter, using a two pole low pass filter, is configurable for 0, .75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
Common mode rejection	Ac CMR 60 dB @ 60 Hz, with up to ± 5 V common mode voltage Dc CMR 80 dB with -5 to +7 peak volt common mode voltage
Common mode voltage range	± 5 V (± 2 V CMR for the ± 10 V inputs)
Output converter	12-bit D/A converter with 0.5% accuracy
Output load	500 Ω for 4-20 mA output – board revisions prior to and including VAICH1C (requires TBAIH1B or DTAI) 800 Ω for 4-20 mA output, board revisions VAICH1D and later (requires TBAIH1C or STAI) 50 Ω for 200 mA output
Power consumption	Less than 31 MW
Compressor stall detection	Detection and relay operation within 30 ms
Fault detection	Analog input out of limits Monitor D/A outputs, output currents, and total current Monitor suicide relay and 20/200 mA scaling relays Compare input signals with the voted value and check difference against the TMR limit Failed I/O chip
Physical	
Temperature	0 to 60°C (32 to 140 °F)
Size	26.04 cm high x 1.99 cm wide x 18.73 cm deep (10.26 in x 0.782 in x 7.375 in)

Diagnostics

Three LEDs at the top of the VAIC front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED displays STATUS and is normally off, but displays a steady orange if a diagnostic alarm condition exists in the board. Diagnostic checks include the following:

- Each analog input has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG_VAIC, which refers to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets the out of limits.
- In TMR systems, if one signal varies from the voted value (median value) by more than a predetermined limit, that signal is identified and a fault is created. This can provide early indication of a problem developing in one channel.
- Monitor D/A outputs, output currents, total current, suicide relays and 20/200 mA scaling relays; these are checked for reasonability and can create a fault.
- TBAI has its own ID device that is interrogated by VAIC. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When the chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Parameter	Description	Choices
Configuration		
System limits	Enable or disable system limits	Enable, disable
Output voting	Select type of output voting	Simplex, simplex TMR
Min_ MA_Input	Select minimum current for healthy 4-20 mA input	0 to 21 mA
Max_ MA_Input	Select maximum current for healthy 4-20 mA input	0 to 21 mA
CompStalType	Select compressor stall algorithm (# of transducers)	0, 2, or 3
InputForPS3A	Select analog input circuit for PS3A	Analog in 1, 2, 3, or 4
InputForPS3B	Select analog input circuit for PS3B	Analog in 1, 2, 3, or 4
InputForPS3C	Select analog input circuit for PS3C	Analog in 1, 2, 3, or 4
SelMode	Select mode for excessive difference pressure	Maximum, average
PressDelta	Excessive difference pressure threshold	5 to 500
TimeDelay	Time delay on stall detection, in milliseconds	10 to 40
KPS3_Drop_Min	Minimum pressure rate	10 to 2000
KPS3_Drop_I	Pressure rate intercept	10 to 100
KPS3_Drop_S	Pressure rate slope	0.05 to 10
KPS3_Delta_S	Pressure delta slope	0.05 to 10
KPS3_Delta_I	Pressure delta intercept	10 to 100
KPS3_Delta_Mx	Pressure delta maximum	10 to 100
KPS3_Drop_L	Threshold pressure rate	10 to 2000
KPS3_Drop_Mx	Max pressure rate	10 to 2000
J3:IS200TBAIH1A	Terminal board connected to VAIC through J3	Connected, not connected
AnalogIn1	First of 10 analog inputs - board point	Point edit (input FLOAT)
Input type	Current or voltage input type	Unused, 4-20 mA, ± 5 V, ± 10 V
Low_Input	Value of current at the low end of scale	-10 to +20
Low_Value	Value of input in engineering units at low end of scale	-3.4082e + 038 to 3.4028e + 038
High_Input	Value of current at the high end of scale	-10 to +20
High_Value	Value of input in engineering units at high end of scale	-3.4082e + 038 to 3.4028e + 038
Input_Filter	Bandwidth of input signal filter	Unused, 0.75, 1.5 Hz, 3 Hz, 6 Hz, 12 Hz
TMR_Diff_Limit	Difference limit for voted inputs in % of high-low values	0 to 100
Sys_Lim_1_Enable	Input fault check	Enable, disable
Sys_Lim_1_Latch	Input fault latch	Latch, unlatch
Sys_Lim_1_Type	Input fault type	Greater than or equal Less than or equal
Sys_Lim_1	Input limit in engineering units	-3.4082e + 038 to 3.4028e + 038
Sys_Lim_2_Enable	Input fault check	Enable, disable
Sys_Lim_2_Latch	Input fault latch	Latch, unlatch
Sys_Lim_2_Type	Input fault type	Greater than or equal Less than or equal
Sys_Lim_2	Input limit in engineering units	-3.4082e + 038 to 3.4028e + 038
AnalogOut1	First of two analog outputs - board point	Point edit (output FLOAT)
Output_MA	Type of output current	Unused, 0-20 mA, 0-200 mA
Low_MA	Output mA at low value	0 to 200 mA
Low_Value	Output in engineering units at low mA	-3.4082e + 038 to 3.4028e + 038
High_MA	Output mA at high value	0 to 200 mA
High_Value	Output value in engineering units at high mA	-3.4082e + 038 to 3.4028e + 038

Parameter	Description	Choices
TMR Suicide	Suicide for faulty output current, TMR only	Enable, disable
Diff Limit	Current difference for suicide, TMR only	0 to 200 mA
D/A Err Limit	Difference between D/A reference and output, in % for suicide, TMR only	0 to 100 %
J4:IS200TBAIH1A	Terminal board connected to VAIC via J4	Connected, not connected
AnalogIn11	First of 10 analog inputs - board point	Point edit (input FLOAT)
AnalogOut3	First of two analog outputs - board point	Point edit (output FLOAT)

Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VAIC1	Board diagnostic	Input	BIT
L3DIAG_VAIC2	Board diagnostic	Input	BIT
L3DIAG_VAIC3	Board diagnostic	Input	BIT
SysLimit1_1	System limit 1	Input	BIT
:	:	Input	BIT
SysLimit1_20	System limit 1	Input	BIT
SysLimit2_1	System limit 2	Input	BIT
:	:	Input	BIT
SysLimit2_20	System limit 2	Input	BIT
OutSuicide1	Status of suicide relay for output 1	Input	BIT
:	:	Input	BIT
OutSuicide4	Status of suicide relay for output 4	Input	BIT
DeltaFault	Excessive difference pressure	Input	BIT
CompStall	Compressor stall	Input	BIT
:	:	Input	FLOAT
Out4MA	Feedback, total output current, mA	Input	FLOAT
CompPressSel	Selected compressor press, by stall Algor.	Input	FLOAT
PressRate Sel	Selected compressor press rate, by stall Algor.	Input	FLOAT
CompStallPerm	Compressor stall permissive	Output	BIT

Alarms

Fault	Fault Description	Possible Cause
2	Flash memory CRC failure	Board firmware programming error (board will not go online)
3	CRC failure override is active	Board firmware programming error (board is allowed to go online)
16	System limit checking is disabled	System checking was disabled by configuration
17	Board ID failure	Failed ID chip on the VME I/O board
18	J3 ID failure	Failed ID chip on connector J3, or cable problem
19	J4 ID failure	Failed ID chip on connector J4, or cable problem
24	Firmware/hardware incompatibility. The firmware on this board cannot handle the terminal board it is connected to	Invalid terminal board connected to VME I/O board-check the connectors and call the factory
30	ConfigCompatCode mismatch. Firmware: [] ; Tre: [] The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory
31	IOCompatCode mismatch. Firmware: [] ; Tre: [] The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory
32-65	Analog input [] unhealthy	Excitation to transducer, bad transducer, open or short-circuit
66-69	Output [] individual current too high relative to total current. An individual current is N mA more than half the total current, where N is the configurable TMR_Diff Limit	Board failure
70-73	Output [] total current varies from reference current. Total current is N mA different than the reference current, where N is the configurable TMR_Diff Limit	Board failure or open circuit
74-77	Output [] reference current error. The difference between the output reference and the input feedback of the output reference is greater than the configured DA_Err Limit measured in percent	Board failure (D/A converter)
78-81	Output [] individual current unhealthy. Simplex mode only alarm if current out of bounds	Board failure
82-85	Output [] suicide relay non-functional. The shutdown relay is not responding to commands	Board failure (relay or driver)
86-89	Output [] 20/200 mA selection non-functional. feedback from the relay indicates incorrect 20/200 mA relay selection (not berg jumper selection)	Configured output type does not match the jumper selection, or VAIC board failure (relay)
90-93	Output [] 20/20 mA suicide active. One output of the three has suicided, the other two boards have picked up current	Board failure
94	J3 terminal board and configuration incompatible	
95	J4 terminal board and configuration incompatible	
128-223	Logic Signal [] voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable
224-249	Input Signal # voting mismatch, Local [], Voted []. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable

TBAI Analog Input/Output

Functional Description

The Analog Input/Output (TBAI) terminal board supports 10 analog inputs and 2 outputs. The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The analog outputs can be set up for 0-20 mA or 0-200 mA current. Inputs and outputs have noise suppression circuitry to protect against surge and high frequency noise.

TBAI has three DC-37 pin connectors provided on TBAI for connection to the I/O processors. Simplex applications are supported using a single connector (JR1). TMR applications are supported using all three connectors.

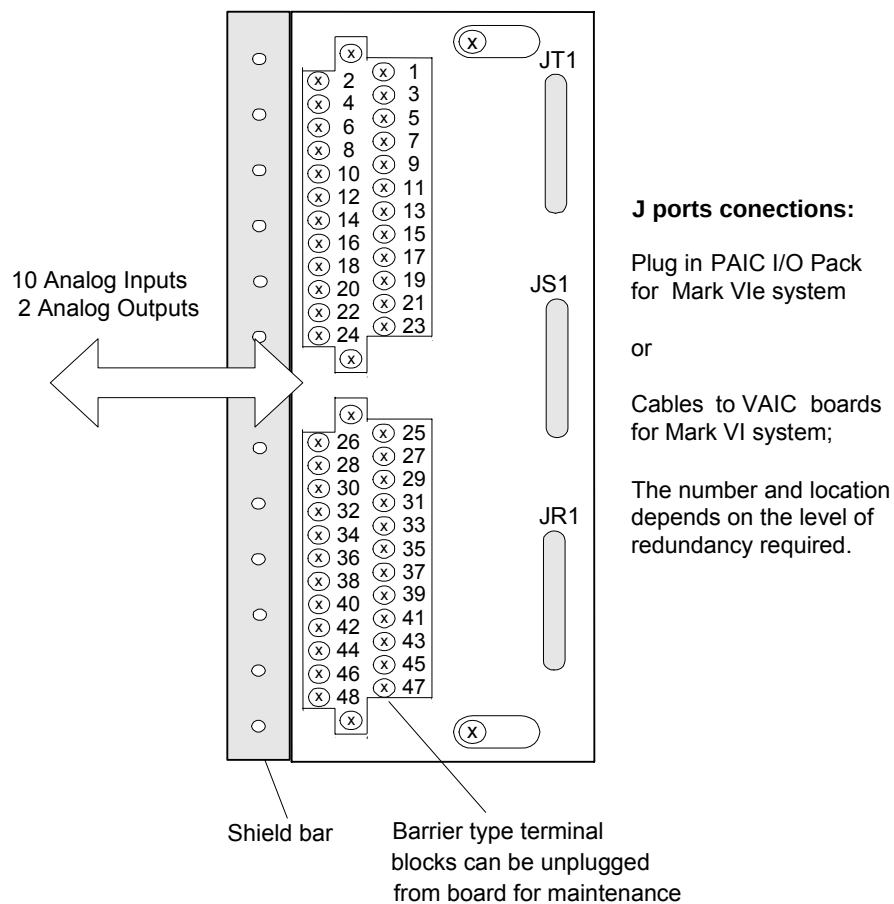
In TMR applications, the input signals are fanned to the three connectors for the R, S, and T controls. TMR outputs combine the current of the three connected output drivers and determine the total current with a measuring shunt. TBAI then presents the total current signal to the I/O processors for regulation to the commanded setpoint.

Mark VI Systems

In the Mark* VI system, TBAI works with VAIC processor and supports simplex and TMR applications. One or two TBAs can be connected to the VAIC. In TMR systems, TBAI is cabled to three VAIC boards.

Mark VIe Systems

In the Mark VIe system, TBAI works with the PAIC I/O pack and supports simplex and TMR applications. In TMR systems, three PAICs plug directly into the TBAI.



TBAI Input Terminal board

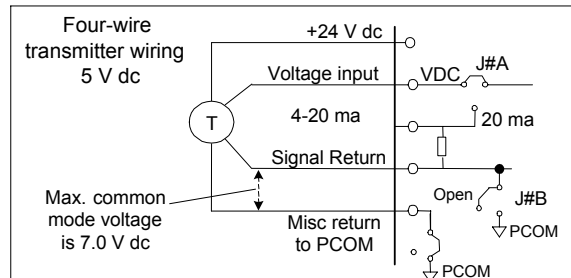
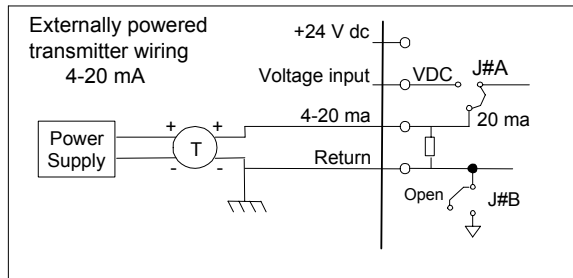
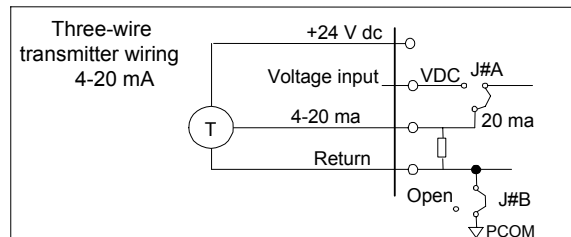
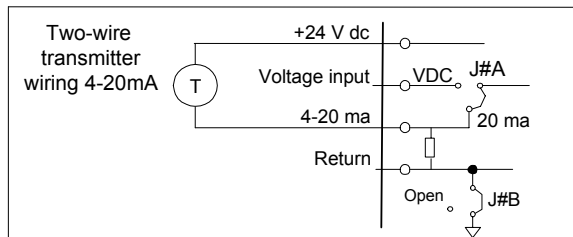
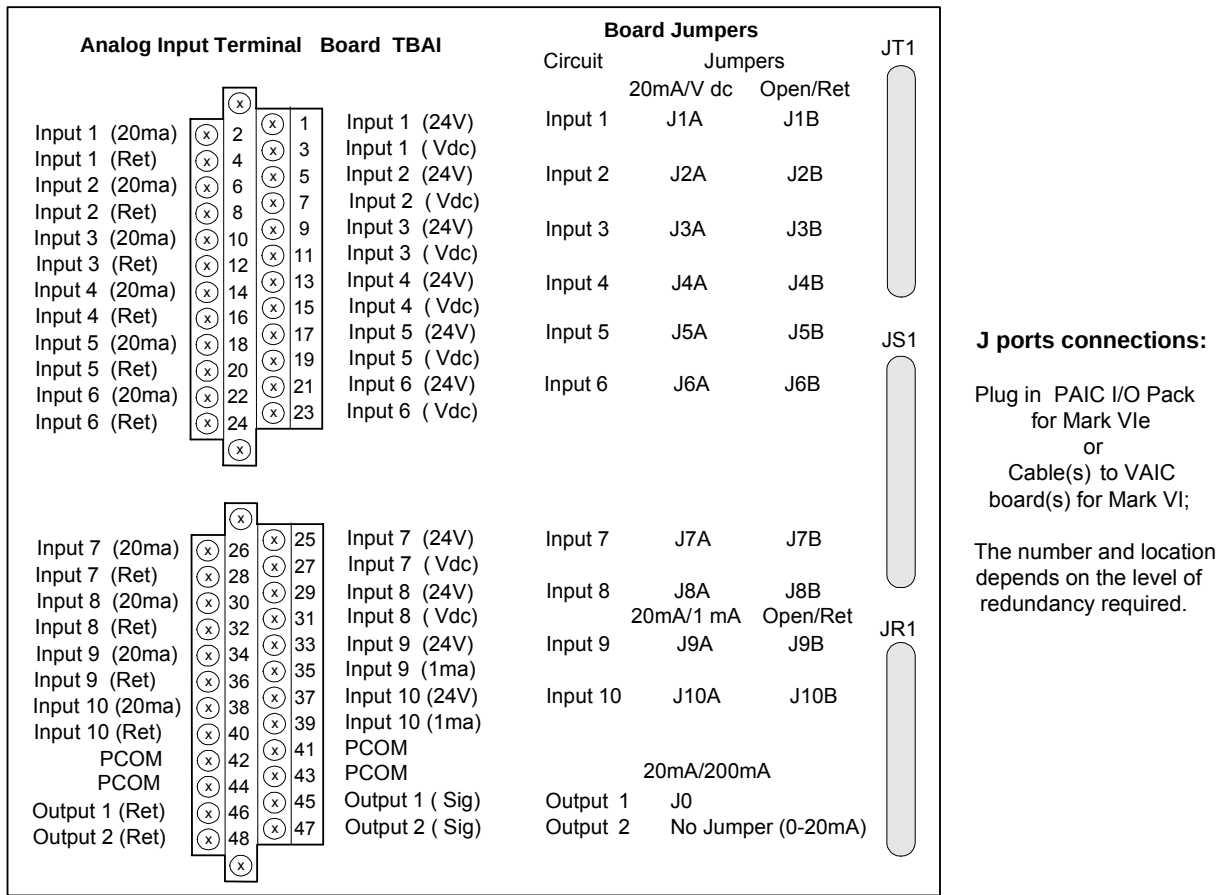
Installation

Connect the input and output wires directly to two I/O terminal blocks mounted on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal attachment point is located adjacent to each terminal block.

TBAI can accommodate the following analog I/O types:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ± 5 V, ± 10 V dc
- Analog output, 0-20 mA
- Analog output, 0-200 mA

The following diagram shows the wiring connections, jumper positions, and cable connections for TBAI.



TBAI Terminal Board Wiring

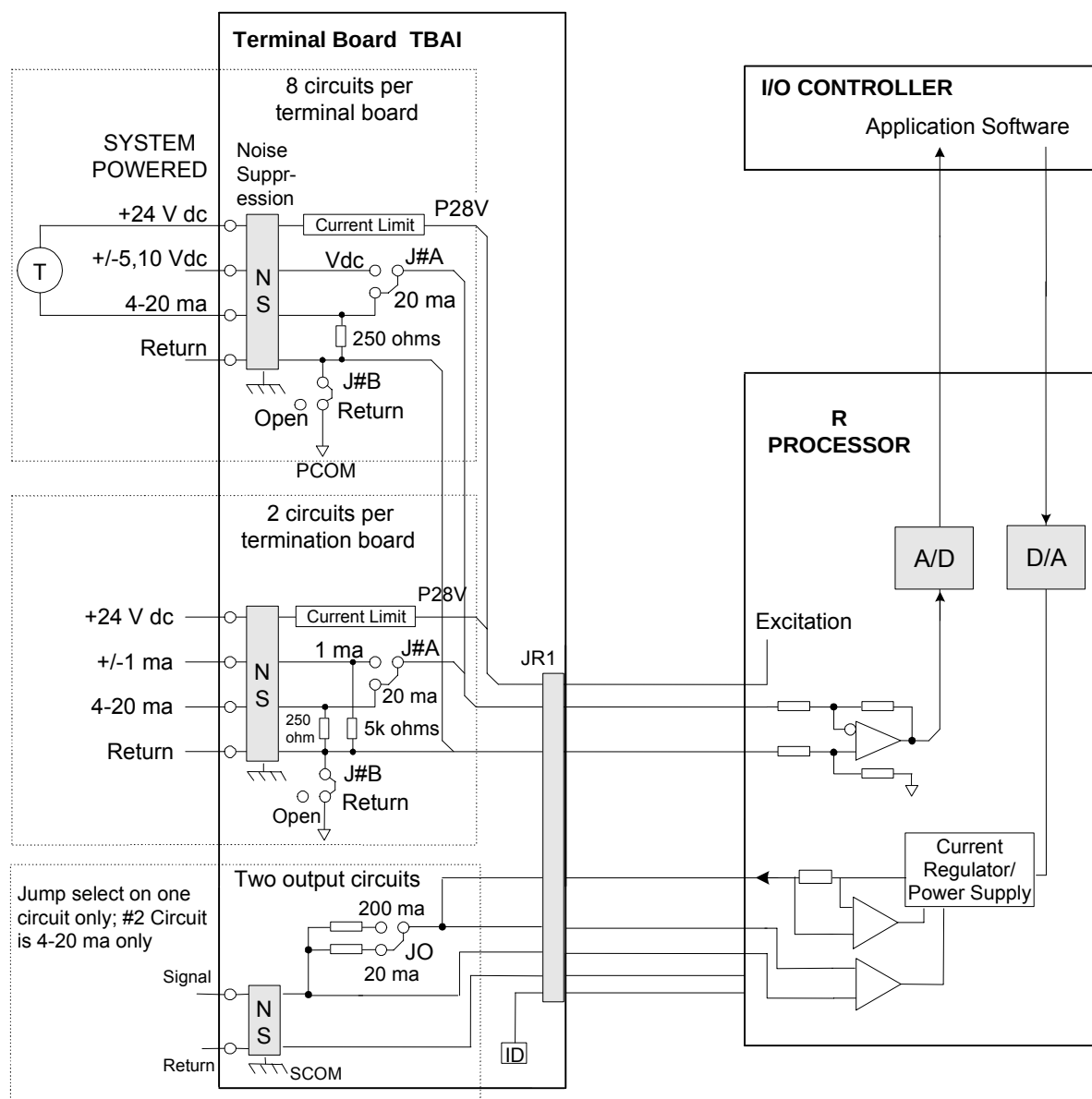
Operation

TBAI provides a 24 V dc power source for all the transducers. The inputs can be configured as current or voltage inputs using jumpers (J#A and J#B). One of the two analog output circuits is 4-20 mA and the other can be configured as 4-20 mA or 0-200 mA. The following table displays the analog I/O capacity of TBAI.

Quantity	Analog Input Types	Quantity	Analog Output Types
8	± 10 V dc, or ± 5 V dc, or 4-20 mA	1	0-20 mA or 0-200 mA
2	4-20 mA, or ± 1 mA	1	0-20 mA

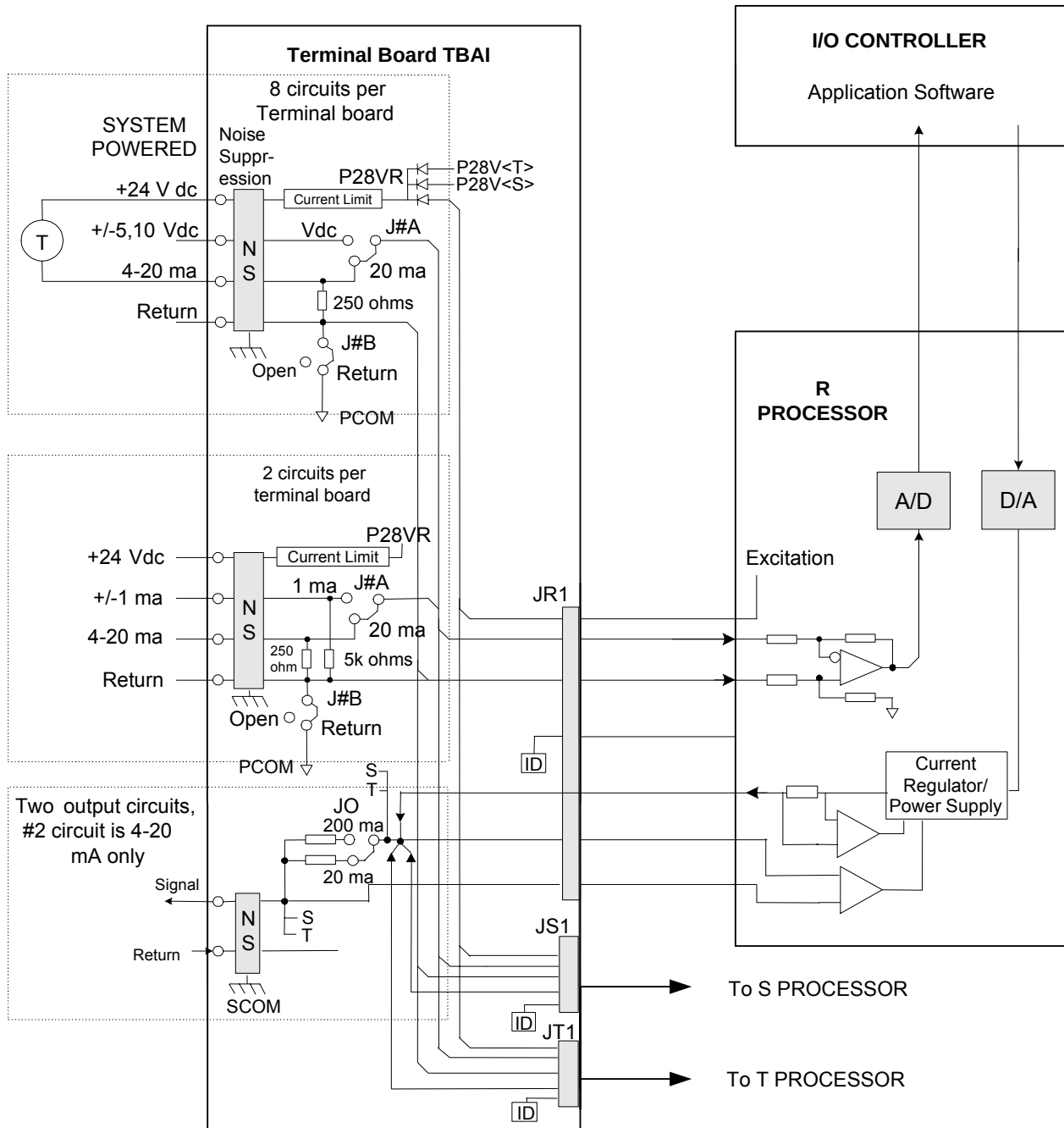
Note With the noise suppression and filtering, the input ac CMR is 60 dB, and the dc CMR is 80 dB.

Each 24 V dc power output is rated to deliver 21 mA continuously and is protected against operation into a short circuit. Transmitters/transducers can be powered by the 24 V dc source in the control system, or can be independently powered. Jumper JO selects the type of current output. Diagnostics monitor each output and a suicide relay in the I/O controller disconnects the corresponding output if a fault cannot be cleared by a command from the processor.



Simplex Analog Inputs and Outputs

In a TMR system, analog inputs fan out to the three I/O controllers (VAIC or PAIC). The 24 V dc power to the transducers comes from all three controllers and is diode shared on TBAI. Each analog current output is fed by currents from all three controllers. The actual output current is measured with a series resistor, which feeds a voltage back to each I/O controller. The resulting output is the voted middle value (median) of the three currents. The following figure shows TBAI in a TMR system.



Analog Inputs and Outputs, TMR

Specifications

Item	Specification
Number of channels	12 channels (10 AI, 2 AO)
Input span, transmitters	1-5 V dc from 4-20 mA current input
Outputs	24 V outputs provide 21 mA each connection
Maximum lead resistance	15 Ω maximum two-way cable resistance, cable length up to 300 m (984 ft)
Output load	500 Ω for 4-20 mA output, TBAIH1B with VAICH1C 800 Ω for 4-20 mA output, TBAIH1C with VAICH1D 800 Ω for 4-20 mA output, TBAIH1C with PAIC 50 Ω for 200 mA
Physical	
Fault detection	Monitor total output current Check connector ID chip for hardware incompatibility
Temperature	-30 to 65°C (-22 to +149 °F)
Size	10.16 cm wide x 33.02 cm high (4.0 in x 13 in)

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers J1A through J8A select either current input or voltage input.
- Jumpers J1B through J8B select whether the return is connected to common or is left open.
- Jumpers J9A and J10A select either 1 mA or 20 mA input current.
- Jumpers J9B and J10B select whether the return is connected to common or is left open.
- Jumper J0 sets output 1 to either 20 mA or 200 mA.

DTAI Simplex Analog Input/Output

Functional Description

The Simplex Analog Input/Output (DTAI) terminal board is a compact analog input terminal board designed for DIN-rail mounting. The board has 10 analog inputs and 2 analog outputs and connects to the VAIC processor board with a single cable. This cable is identical to those used on the larger TBAI terminal board. The terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space.

The 10 analog inputs accommodate two-wire, three-wire, four-wire, or externally powered transmitters. The two analog outputs are 0-20 mA, but one can be jumper configured to a 0-200 mA current. Two DTAI boards can be connected to VAIC for a total of 20 analog inputs and 4 analog outputs. Only a simplex version of the board is available.

The functions and on-board noise suppression are the same as those on the TBAI. High-density euro-block type terminal blocks are permanently mounted to the board, with two screw connections for the ground connection (SCOM). An on-board ID chip identifies the board to the VAIC for system diagnostic purposes.

Installation

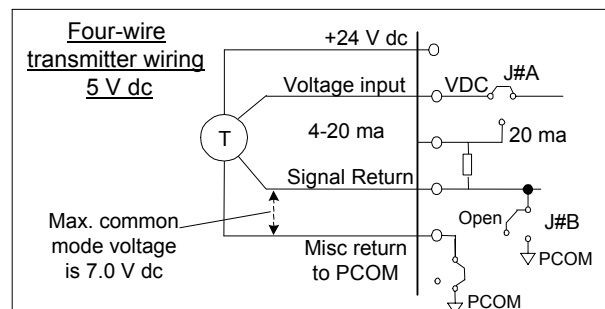
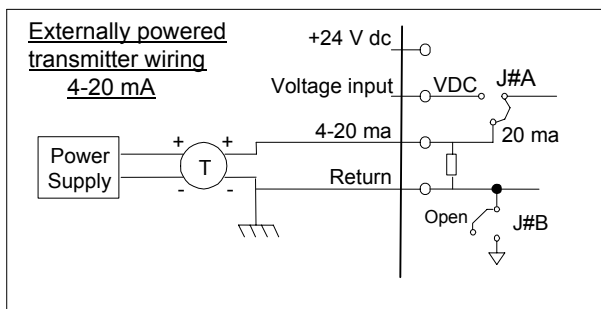
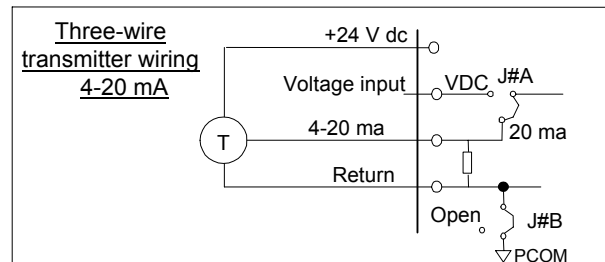
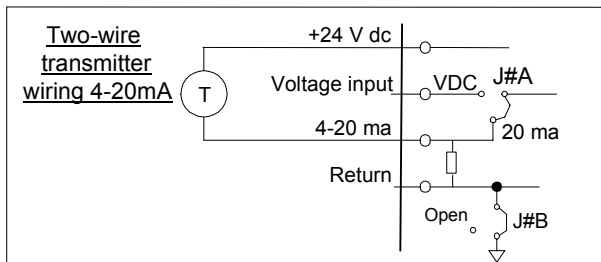
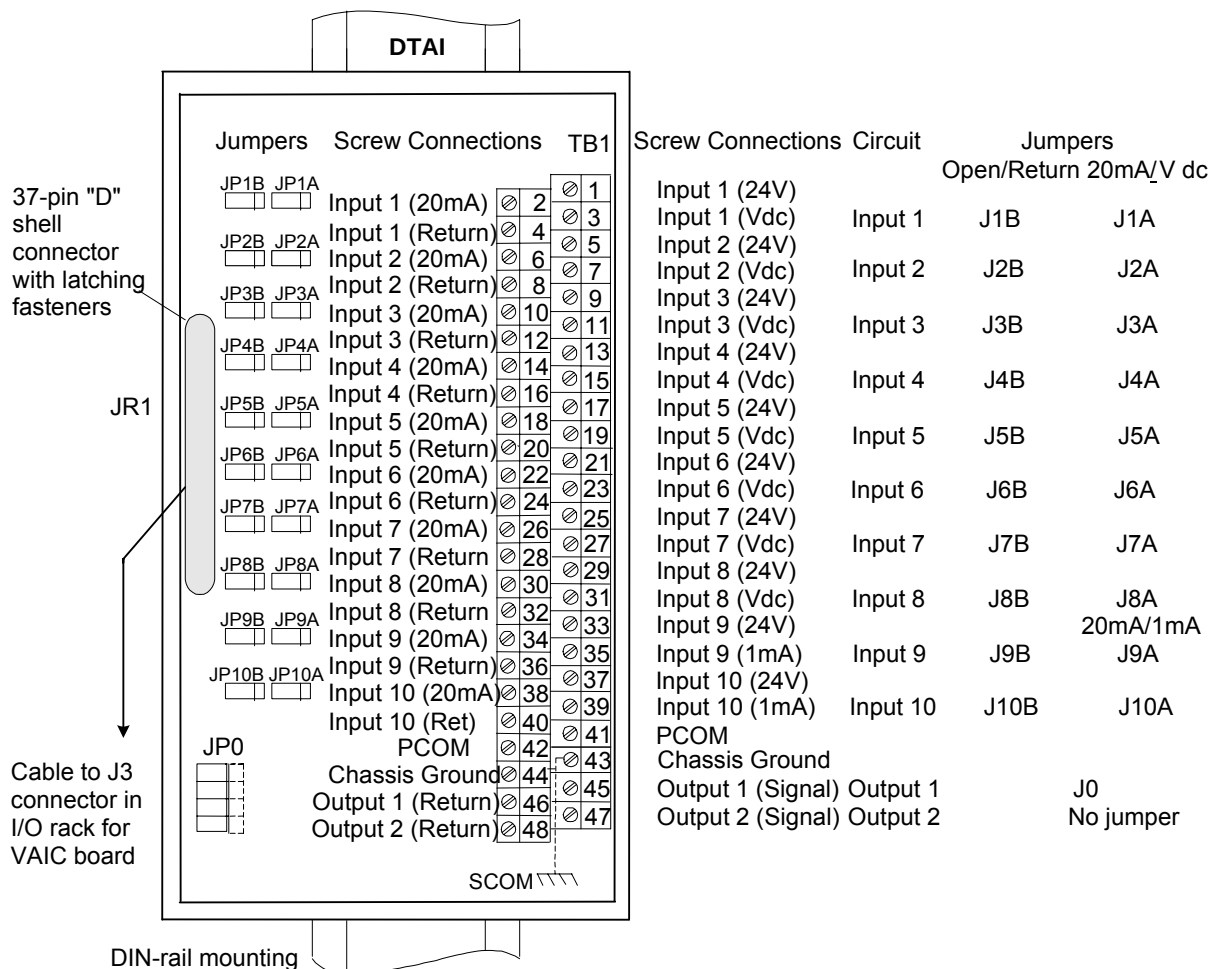
Mount the plastic holder on the DIN-rail and slide the DTAI board into place. Connect the RTD wires directly to the terminal block. The Euro-block type terminal block has 48 terminals and is permanently mounted on the board. Typically, #18 AWG wires (shielded twisted pair) are used. Two screws, 43 and 44, are provided for the SCOM (ground) connection, which should be as short a distance as possible.

Note There is no shield terminal strip with this design.

DTAI accommodates the following analog I/O types:

- Analog input, two-wire transmitter
- Analog input, three-wire transmitter
- Analog input, four-wire transmitter
- Analog input, externally powered transmitter
- Analog input, voltage ± 5 V, ± 10 V dc
- Analog output, 0-20 mA current
- Analog output, 0-200 mA current
- Wiring, jumper positions, and cable connections appear on the wiring diagram

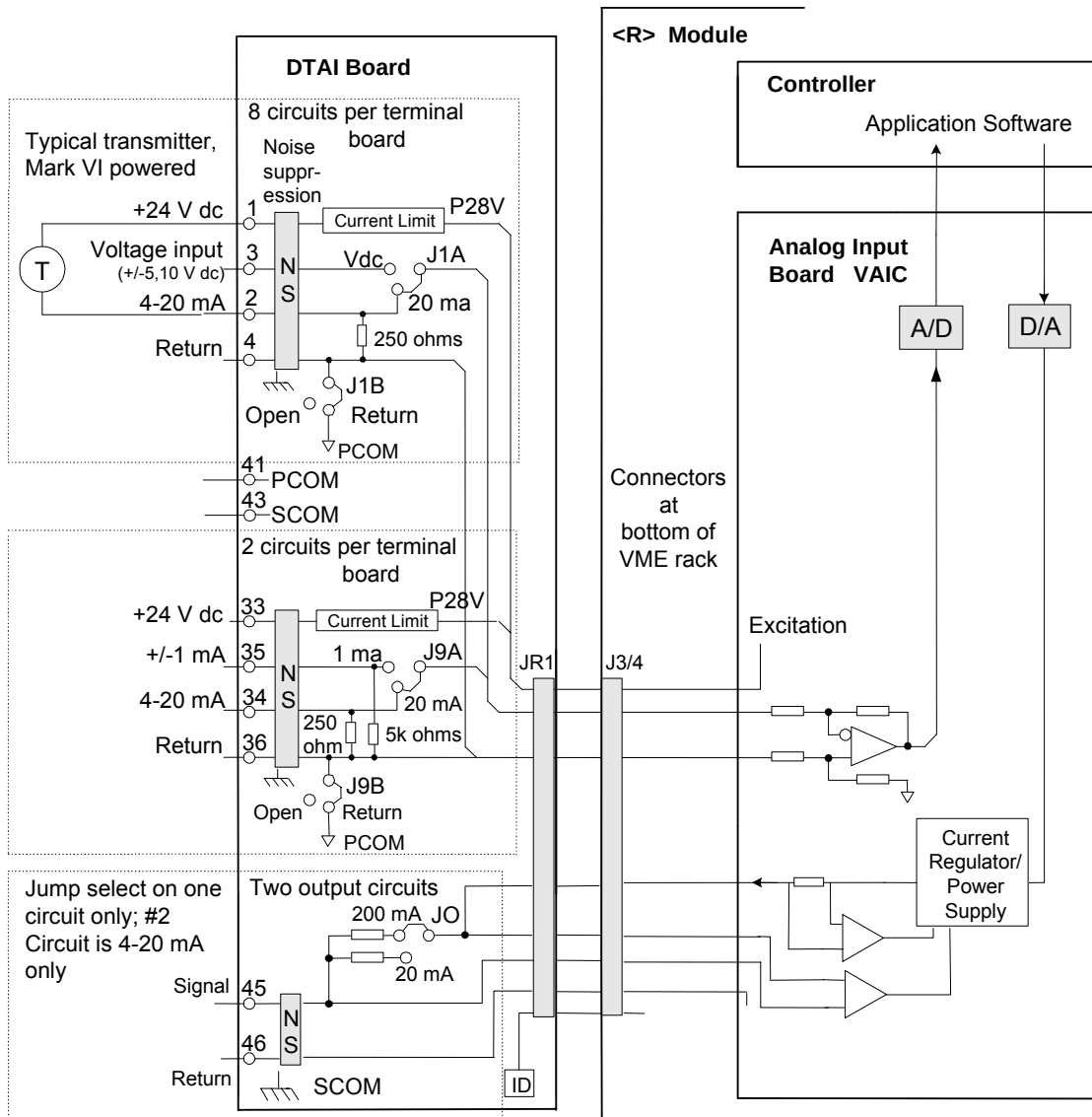
Note SCOM, terminal 43, must be connected to chassis ground.



DTAI Wiring, Cabling, and Jumper Positions

Operation

24 V dc power is available on DTAI for all the transducers and the inputs can be configured as current or voltage inputs using jumpers. One of the two analog output circuits is 4-20 mA, and the other can be jumper configured for 4-20 mA or 0-200 mA. DTAI has only one cable connection so it cannot be used for TMR applications as with TBAI.



DTAI Terminal Board and VAIC I/O Processor

The following table displays the analog I/O capacity of DTAI.

Quantity	Analog Input Types	Quantity	Analog Output Types
8	±10 V dc, or ±5 V dc, or 4-20 mA	1	0-20 mA or 0-200 mA
2	4-20 mA, or ±1 mA	1	0-20 mA

Specifications

Item	Specification
Number of channels	12 channels (10 AI, 2 AO)
Input span, transmitters	1 - 5 V dc from 4-20 mA current input
Maximum lead resistance to transmitters	15 Ω maximum two-way cable resistance, cable length up to 300m (984 ft)
Outputs	24 V outputs provide 21 mA for each connection
Maximum lead resistance	15 Ω maximum two-way cable resistance, cable length up to 300m (984 ft).
Output load	500 Ω for 4-20 mA output. 50 Ω for 200 mA output with VAICH1C
Fault detection	Monitor output current Check ID chip on connector
Physical	
Temperature	0 to 60°C (32 to 140 °F)
Size, with support plate	8.6 cm wide x 16.2 cm high (3.4 in x 6.37 in)

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

The terminal board is configured by jumpers. For the location of these jumpers, refer to the installation diagram. The jumper choices are as follows:

- Jumpers J1A through J8A select either current input or voltage input.
- Jumpers J1B through J8B select whether the return is connected to common or is left open.
- Jumpers J9A and J10A select either 1 mA or 20 mA input current.
- Jumpers J9B and J10B select whether the return is connected to common or is left open.
- Jumper J0 sets output 1 to either 20 mA or 200 mA.

Notes

VAMA Acoustic Monitoring

VAMA Acoustic Monitoring

Functional Description

The Acoustic Monitoring (VAMA) board monitors acoustic or pressure waves in the turbine combustion chamber. Inputs are wired to the DIN-rail mounted DDPT terminal board. DDPT supports the simplex mode only and connects to VAMA through the J3 connector on the VME rack where VAMA is located.

The VAMA/DDPT meets environment rating for hazardous gases of Class I, Division 2 and provides suppression at all points of signal entry or exit. Each cable has a unique ID chip. The VAMA provides two point calibration, based on a reference offset and gain signal.

Gas turbine combustion chambers can experience pressure oscillations that cause noise in the audible hearing range. The H1A version of the VAMA offers signal conditioning and software that allows the turbine control to monitor the pressure/acoustic waves by reading the conditioned signals from a dynamic pressure transducer. The VAMA provides two channels to read the pressure/acoustic wave signals from third party equipment from Vibro-Meter® or Bently-Nevada*. VAMA provides two dedicated signal conditioning paths to remove the dc component of the signal, modify the gain, and provide an eighth order or better low-pass filter for anti-aliasing.

Installation

➤ To install the V-type board

- 1 Power down the VME processor rack.
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors.
- 3 Tighten the captive screws at the top and bottom of the front panel. These screws serve to hold the board firmly in place and enhance the board front ground integrity. The screws should not be used to actually seat the board.

Note Cable connections to the terminal board are made at the J3 connector on the lower portion of the VME rack, and the J5 connector on the front of the board. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to *Diagnostics* section in this document.

It may be necessary to update the VAMA firmware to the latest level. For instructions, refer to *GEH-6403, Control System Toolbox for Configuring the Mark VI Turbine Controller*.

Operation

Pressure/Acoustic Wave Signal Conditioning

VAMA provides signal conditioning for two pressure/acoustic wave inputs and can supply either ± 24 V dc to power the pressure sensing equipment. VAMA supports the following third party vendor equipment:

- Vibro-Meter Galvanic Separation Unit types GSI 1_ _
- Bently-Nevada 86517 with modifications 142533 or 159840 charge amplifier
- Bently-Nevada dynamic pressure charge amplifier 350500

Note The Vibro-Meter GSI 1_ _ unit prevents problems due to voltage differences between the measuring point and signal processing (such as ground loops).

The Vibro-Meter setup conditions a pico-coulomb output from a dynamic pressure transducer (Vibro-Meter CP216 or CP231) through a charge amplifier (Vibro-Meter IPC 704) with a current output representing approximately 125 μ A/psi. The GSI unit outputs an ac signal (approx. ± 2 V peak) that represents the dynamic pressure (gain expressed in mV/psi) riding on top of a dc bias voltage of approximately +7 V dc. The Vibro-Meter GSI unit requires a +24 V dc power supply. Normally, the power supply return for the GSI is grounded externally and the PCOM on the terminal board is not used. PCOM should only be used when the external return ground is not used.

The Bently-Nevada 86517 interface module converts the dynamic pressure transducer charge signal from pico-coulombs to milli-volts, which represents the pressure in psi. The interface module outputs ac signal (approx. ± 1.2 V peak) riding on top of a negative dc bias voltage of approximately -10 V dc. The Bently-Nevada unit requires a -24 V dc power supply.

VAMA/DDPT Vendor Equipment Power Supply Specifications

Vendor	Power Supply	Nominal Voltage	Nominal Current
Vibro-Meter	Positive 24 V dc	+24 V dc ($\pm 5\%$)	0.04 A (± 0.02 A)
Bently-Nevada	Negative 24 V dc	-24 V dc ($\pm 5\%$)	0.02 A (± 0.01 A)

The pressure/acoustic signal is read differentially by connecting the DDPT inputs, Pressure Wave Channel A High (ASIG) and Pressure Wave Channel A Low (ARET). Voltage clamping and high frequency suppression is applied on the DDPT before the signal is routed to the VAMA through the 37-pin cable to the J3 connector on the VME rack. The jumpers, JP1A/B and JP2A/B, are used to add a bias corresponding to the dc bias provided by the third party interface unit to detect open circuit conditions.

Therefore, a +28 V dc bias is added for the Vibro-Meter connection and a -28 V dc bias is added for the Bently-Nevada system. The DDPT pressure wave outputs are ASIG/ARET for the output pair for channel A, and BSIG/BRET for the output pair for channel B.

Signal Conditioning for Fast Fourier Transform (FFT) Input

Note The FFT signal conditioning provides open-wire detection circuitry and any dc bias monitoring circuitry, if needed. The output from channel A and channel B feeds into a high-speed multiplexed A/D section.

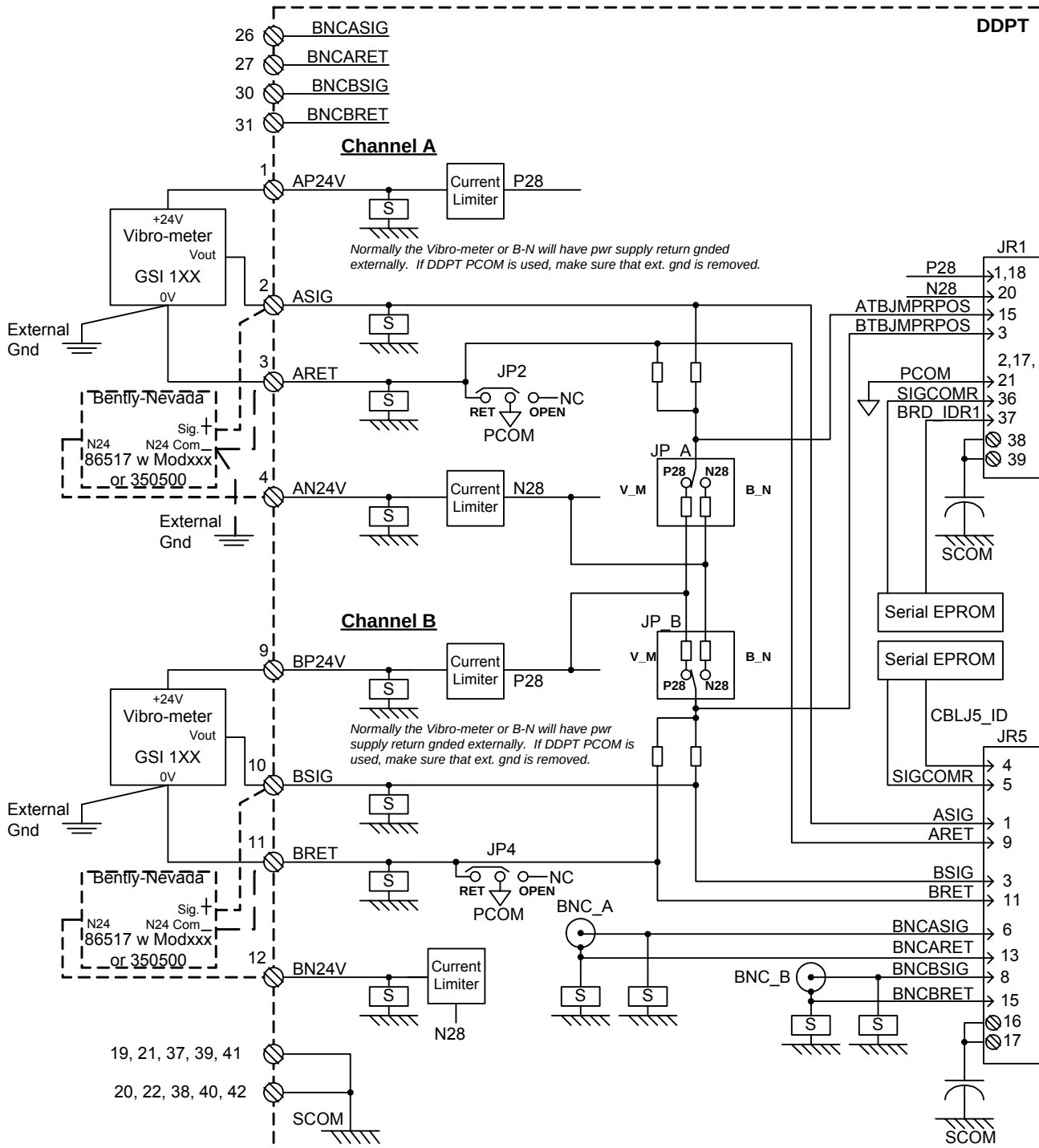
VAMA provides differential inputs for both channel A and B pressure wave signals. The signal conditioning includes a high pass filter, gain adjustment, and a low pass filter with adjustable break frequencies. The high-pass filter is a single pole filter (6 dB/octave) with a break at 1.5 Hz. The gain block provides two gain options, 2.25 or 4.5 V/V. The low pass filter is an eight-pole (48 dB/octave) Butterworth filter with three selectable break frequencies, 600, 1000, and 3600 Hz. The gain options and the low-pass filter break frequency adjustments are selectable through software.

Signal Conditioning for the RMS Circuit

VAMA provides an RMS rectifier circuit for both channel A and channel B pressure waves. Each circuit includes a high pass filter, a low pass filter, and the RMS detector. The band-pass filters are 260 to 970 Hz , before the detector and the RMS detector. The input signal range is from 0 to 10 psi peak-to-peak, which is represented by an ac signal with the scaling of 0.1 V/psi. The rms detector output from channel A and channel B feeds into a multiplexed A/D section.

BNC Signal Conditioning

VAMA provides a buffered signal conditioning circuit for each BNC output on the DDPT terminal board. The BNC buffered circuit takes its input from the ac pressure wave input without the dc bias signal. The gain of the buffer is 1. The signal for the buffered BNC output ranges from 0 to 40 psi peak-to-peak, which is represented by an ac signal with the scaling of 0.1 V/psi.



DDPT Board Block Diagram



Pressure/Acoustic Wave FFT Algorithms

The firmware performs a spectral analysis of the pressure wave to determine the spectral components with the largest magnitude and the frequency associated with each magnitude. The local sort function sorts the three largest magnitudes for a given frequency band. The FFT algorithm supports three frequency bands.

Note The magnitude and frequency information for each spectral component that meets the criteria of the sorts is stored in Signal Space for the VAMA memory space.

Discontinuities at the beginning and end of the 8192 collected data points of the pressure wave produce high frequency components that alias down into the spectrum of interest. Using a Windowing function on the data attenuates the high frequency components. The user can select from seven different windowing functions that affect spectral content of these high frequency components. An FFT is performed on the windowed data to determine the spectral component's magnitude and the frequency associated with it. A Global Sort function ranks the spectral components from the largest in magnitude to the smallest. Then a Local Sort function selects the three largest magnitudes and their associated frequencies for a frequency band defined by the user.

The composite pressure wave signal that includes both the ac and dc offset component of the signal is read by the slow A/D on VAMA. Firmware monitors this signal to perform continuity and out of range checks. The pressure wave has a normal operating range of ± 1 psi with the trip level set at 2 psi. The FFT magnitude is significantly attenuated when spectral content is off the bin center. Attenuation factor (approx. 0.6 to 0.9) is determined by the Windowing technique used.

Functions

Windowing Function

The Windowing function provides a way to reduce the false spectral components caused by the beginning and ending points of the 8192 data points collected. The discontinuities caused by the end point data produces high frequency components that alias down into the frequency spectrum of interest. Each windowing function affects the magnitude and spectral leakage. Seven windowing techniques are provided, as follows:

- Rectangular
- Hamming
- Hanning
- Triangular
- Blackman
- Blackman-Harris
- Flat Top

The configuration constant, *WindowSelect*, is the window select control for both channel A and channel B pressure waves. The configuration constant, *BinReject*, determines the number of side bins rejected from a spectral peak found in the FFT analysis. *BinReject* controls the number of side bins removed from the FFT analysis for both channel A and B. An FFT is performed on the *windowed* data to determine the spectral content of the pressure wave. The power is calculated for each FFT element and the magnitude and frequency are calculated from the power. The windowing type and the associated sideband rejection are shown in the following table.

Selection	Function	Rejected Sidebands (Default)
1	Rectangular	3
2	Hamming	3
3	Hanning	3
4	Triangular	3
5	Blackman	3
6	Blackman-Harris	3
7	Flat Top	4

Sort Function

The Sort function tests for the three largest FFT element magnitudes in a user specified frequency band. The user can specify up to three frequency bands with three magnitudes and associated frequency for each stored in signal space.

The following table defines the user defined configuration constants, FminFrqbandx and FmaxFrqbandx, that are supported by the Sort function. The firmware provides separate scaling for channel A and B and defines the transfer function from two given points.

Signal Space Variables to Support Pressure Wave FFT Algorithm

Variable	Description	Units	Min.	Max.
PW1MagFb1ChA	Pressure wave 1 magnitude in frequency band 1 of ChA	EU	-3.4e+38	-3.4e+38
PW2MagFb1ChA	Pressure wave 2 magnitude in frequency band 1 of ChA	EU	-3.4e+38	-3.4e+38
PW3MagFb1ChA	Pressure wave 3 magnitude in frequency band 1 of ChA	EU	-3.4e+38	-3.4e+38
PW1MagFb2ChA	Pressure wave 1 magnitude in frequency band 2 of ChA	EU	-3.4e+38	-3.4e+38
PW2MagFb2ChA	Pressure wave 2 magnitude in frequency band 2 of ChA	EU	-3.4e+38	-3.4e+38
PW3MagFb2ChA	Pressure wave 3 magnitude in frequency band 2 of ChA	EU	-3.4e+38	-3.4e+38
PW1MagFb3ChA	Pressure wave 1 magnitude in frequency band 3 of ChA	EU	-3.4e+38	-3.4e+38
PW2MagFb3ChA	Pressure wave 2 magnitude in frequency band 3 of ChA	EU	-3.4e+38	-3.4e+38
PW3MagFb3ChA	Pressure wave 3 magnitude in frequency band 3 of ChA	EU	-3.4e+38	-3.4e+38
PW1MagFb1ChB	Pressure wave 1 magnitude in frequency band 1 of ChB	EU	-3.4e+38	-3.4e+38
PW2MagFb1ChB	Pressure wave 2 magnitude in frequency band 1 of ChB	EU	-3.4e+38	-3.4e+38
PW3MagFb1ChB	Pressure wave 3 magnitude in frequency band 1 of ChB	EU	-3.4e+38	-3.4e+38
PW1MagFb2ChB	Pressure wave 1 magnitude in frequency band 2 of ChB	EU	-3.4e+38	-3.4e+38
PW2MagFb2ChB	Pressure wave 2 magnitude in frequency band 2 of ChB	EU	-3.4e+38	-3.4e+38
PW3MagFb2ChB	Pressure wave 3 magnitude in frequency band 2 of ChB	EU	-3.4e+38	-3.4e+38
PW1MagFb3ChB	Pressure wave 1 magnitude in frequency band 3 of ChB	EU	-3.4e+38	-3.4e+38
PW2MagFb3ChB	Pressure wave 2 magnitude in frequency band 3 of ChB	EU	-3.4e+38	-3.4e+38
PW3MagFb3ChB	Pressure wave 3 magnitude in frequency band 3 of ChB	EU	-3.4e+38	-3.4e+38

Determination of Fc and Fs

The following table is used to determine the filter break frequency for the eighth order Butterworth filter for each channel of the pressure wave signal conditioning (ac out). It is also used to derive the sample frequency for the fast A/D and the FFT algorithm sample frequency. The configuration constant used as the input to the lookup table is the constant FFTFrqRngChA for channel A and FFTFrqRngChB for channel B.

FFTFrqRngChA or FFTFrqRngChB	FFT Frequency Range of Interest (Hz)	Sample Frequency, Fs (Hz)	Bin Resolution (Hz)	Update Rate (seconds)
260_970HzBPF	260 – 970	12000	1.46	0.68
600Hz_LPF	1.5 – 600	12000	1.46	0.68
1000Hz_LPF	1.5 – 1000	12000	1.46	0.68
3600Hz_LPF	1.5 – 3600	12000	1.46	0.68
260/970HzDBP	260 – 970	12000	1.46	0.68

Display Format of the Data Through TelNet

The following figure shows a portion of the TelNet display for pressure wave channels 1 and 2. The display shows the bin center frequency with the magnitude of the spectral content in peak voltage and psi.

TelNet Display Example of FFT Magnitudes over Frequency Range

VAMA Card's Power Spectrum Screen

Frequency	Transducer 1		Transducer 2	
	MAGN (Vpk)	MAGN (PSI)	MAGN (Vpk)	MAGN (PSI)
0.000	0.0001548	0.0015481	0.0119116	0.1191164
1.465	0.0001836	0.0018366	0.0106850	0.1068505
2.930	0.0000924	0.0009238	0.0037215	0.0372151
4.930	0.0000752	0.0007519	0.0025366	0.0253656
5.860	0.0000685	0.0006848	0.0021200	0.0212001
7.325	0.0000419	0.0004188	0.0013643	0.0136432
v	v	v	v	v

The following figure shows the TelNet screen for transducer channels A and B. The display provides up to three frequency bands defined by configuration constants and outputs the three largest peaks in each frequency band.

TelNet Display Example of FFT Magnitudes over Frequency Range

Signal Space Input	Transducer Channel			
	CH A		CH B	
	MAG (PSI)	FREQ (HZ)	MAG (PSI)	FREQ (HZ)
5 <= FREQ BAND1 <= 500Hz				
1st Highest Peak	0.534	58.6	0.521	60.07
2nd Highest Peak	0.214	102.55	0.204	101.09
3rd Highest Peak	0.102	139.18	0.112	137.71
500 <= FREQ BAND2 <= 1000Hz				
1st Highest Peak	0.211	586	0.227	586
2nd Highest Peak	0.142	732.5	0.135	733.97
3rd Highest Peak	0.087	879	0.079	879
1000 <= FREQ BAND1 <= 3000Hz				
1st Highest Peak	0.334	1465	0.317	1465
2nd Highest Peak	0.134	1611.5	0.128	1612.96
3rd Highest Peak	0.076	2197.75	0.055	2199.22

RMS Peak-to-Peak Calculator

The VAMA firmware includes an rms peak-to-peak calculator for both channel A and channel B signals from the true rms detector. The calculator multiplies the dc rms value read in by 2.828 to convert the A/D reading back to a peak-to-peak value.

Signal Space Variables to Support Pressure Wave FFT

Variable	Description	Units	Min.	Max.
PW_RMStotChA	Channel A pressure wave – total rms value	psi	0	3.54
PW_RMSFb1ChA	Channel A pressure wave – rms value in frequency band 1	psi	0	3.54
PW_RMSFb2ChA	Channel A pressure wave – rms value in frequency band 2	psi	0	3.54
PW_RMSFb3ChA	Channel A pressure wave – rms value in frequency band 3	psi	0	3.54
PW_RMStotChB	Channel B pressure wave – total rms value	psi	0	3.54
PW_RMSFb1ChB	Channel B pressure wave – rms value in frequency band 1	psi	0	3.54
PW_RMSFb2ChB	Channel B pressure wave – rms value in frequency band 2	psi	0	3.54
PW_RMSFb3ChB	Channel B pressure wave – rms value in frequency band 3	psi	0	3.54

Specification

Item	Specification
Number of Transducers	Two, either: Vibro-Meter Galvanic separation Unit types GSI 1__ Bentley-Nevada 86517, 142533, or 159840 charge amplifier Bentley-Nevada 350500 dynamic pressure charge amplifier
Transducer Power Supply	Vibro-Meter: Positive 24 V dc, current of 0.04 A nominal Bentley-Nevada: Negative 24 V dc, current of 0.02 A nominal
Buffered signal outputs	Two channels with ac component only, 0.1 V/psi, available at BNC outputs on DDPT
Pressure wave magnitude range	Mag.min = -14 psi Mag.max = +14 psi
Pressure wave frequency range	Fmin = 1.5 Hz Fmax = 3600 Hz
Maximum FFT sampling frequency	F = 12000 Hz
FFT record length	8192
Windowing techniques supported (side-band rejection)	Rectangular (3) Hamming (3) Hanning(3) Triangular (3) Blackman (3) Blackman-Harris (3) Flat Top (4)
Format for magnitudes and associated frequencies.	Configurable frequency bands with three peaks per band
Display of full FFT spectrum results	Telnet display

Diagnostics

Three LEDs at the top of the VAMA front panel provide status information. The normal RUN condition is a flashing green, FAIL is a solid red. The third LED is STATUS and is normally off but shows a steady orange if a diagnostic alarm condition exists in the board.

VAMA runs continuous diagnostic tests on the signals and hardware. Variables checked include transducer open wire, DAC bias voltage, differential amplifier output voltage, FFT ac gain corrections, FFT LPF, gain and frequency settings, FFT and RMS frequency ranges, gain and frequency settings, and FFT A/D bit integrity (peak bin counts). If any of these go outside of configured limits, VAMA creates a fault. Refer to the *Alarms* section for a complete list of faults (diagnostic alarms).

Configuration

Like all I/O boards, VAMA is configured using the toolbox. This software usually runs on a data-highway connected CIMPLICITY[®] station or workstation. The following tables summarize the configuration choices and defaults. For details, refer to *GEH-6403, Control System Toolbox for the Mark VI Turbine Controller*.

Configuration Constant Name	Description	Units	Min.	Max.
High_Input2	Defines the X-axis value in millivolts for point 2 that is used in calculating the gain and offset for the conversion to engineering units for channel A for the rms circuit	mV	-10000	10000
High_Value2	Defines the Y-axis value in engineering units for point 2 that is used in calculating the gain and offset for the conversion from millivolts to engineering units for rms circuit channel A	E.U.	-3.4e+38	3.4e+38
Low_Input2	Defines the X-axis value in millivolts for point 1 that is used in calculating the gain and offset for the conversion to engineering units for rms circuit channel A	mV	-10000	10000
Low_Value2	Defines the Y-axis value in engineering units for point 1 that is used in calculating the gain and offset for the conversion from millivolts to engineering units for rms circuit channel A	E.U.	-3.4e+38	3.4e+38

Configuration Constants to Support Pressure Wave FFT Algorithm

Configuration Constant Name	Description	Units	Min.	Max.
BinReject	Defines the number of side bins that will be rejected for the FFT results for both channel A and B. 0 = no bins rejected	None	0	5
FFTFreqRange	FFT frequency range (3db points) for both channel A and B. The selections are: 260_970HzBPF (0.0) - 260 to 970 Hz analog band pass filter 600Hz_LPF (600.0) - 600 Hz analog Low Pass filter 1000Hz_LPF (1000.0) - 1000 Hz analog Low Pass filter 3600Hz_LPF (3600.0) - 3600 Hz analog Low Pass filter 260/970HzDBP (260) - 260 to 970 Hz Digital Band pass filter	None	600 Hz	3600 Hz
FminFrqband1	Minimum frequency for frequency band 1 in both channel A and B	Hz	0	3600
FmaxFrqband1	Maximum frequency for frequency band 1 in both channel A and B	Hz	0	3600
FminFrqband2	Minimum frequency for frequency band 2 in both channel A and B	Hz	0	3600
FmaxFrqband2	Maximum frequency for frequency band 2 in both channel A and B	Hz	0	3600

Configuration Constant Name	Description	Units	Min.	Max.
FminFrqband3	Minimum frequency for frequency band 3 in both channel A and B	Hz	0	3600
FmaxFrqband3	Maximum frequency for frequency band 3 in both channel A and B	Hz	0	3600
High_Input	Defines the X-axis value in millivolts for point 2 that is used in calculating the gain and offset for the conversion to engineering units for channel A and B	mV	-10000	10000
High_Value	Defines the Y-axis value in engineering units for point 2 that is used in calculating the gain and offset for the conversion from millivolts to engineering units for channel A and B	E.U.	-3.4 e+038	3.4 e+038
Low_Input	Defines the X-axis value in millivolts for point 1 that is used in calculating the gain and offset for the conversion to engineering units for ch A and B	mV	-10000	10000
Low_Value	Defines the Y-axis value in engineering units for point 1 that is used in calculating the gain and offset for the conversion from millivolts to engineering units for channel A and B	E.U.	-3.4 e+038	3.4 e+038
Min_mV_Input	Minimum millivolts that defines the lower out of range point for the pressure wave input	mV	-10000	10000
Max_mV_Input	Maximum millivolts that defines the upper out of range point for the pressure wave input	mV	-10000	10000
WindowSelect	Selects the <i>Windowing</i> function to be used on the sampled data for both Channel A and B: 1 = Rectangular 4 = Triangular 7 = Flat Top 2 = Hamming 5 = Blackman 3 = Hanning 6 = Blackman-Harris	None	1	7

Alarms

Fault Description	Possible Cause
ASIG Open Wire Detection V dc	Terminal board or cable problem
ARET Open Wire Detection V dc Possible Cause	Terminal board or cable problem
BSIG Open Wire Detection V dc	Terminal board or cable problem
BRET Open Wire Detection V dc	Terminal board or cable problem
Chan A DAC Bias V dc	Board failure
Chan B DAC Bias V dc	Board failure
Chan A Diff Amp Out V dc	Board failure
Chan B Diff Amp Out V dc	Board failure
Chan A FFT Filtered Null Counts	Board failure
Chan B FFT Filtered Null Counts	Board failure
Chan A FFT Filtered Reference Counts	Board failure
Chan B FFT Filtered Reference Counts	Board failure
Chan A (Slow) Filtered RMS Null Counts	Board failure
Chan B (Slow) Filtered RMS Null Counts	Board failure
Chan A (Slow) Filtered RMS Reference Counts	Board failure
Chan B (Slow) Filtered RMS Reference Counts	Board failure
Chan A FFT Null	Board failure
Chan B FFT Null Counts	Board failure
Chan A FFT Reference Counts	Board failure
Chan B FFT Reference Counts	Board failure
Chan A (Slow) RMS Null Counts	Board failure
Chan B (Slow) RMS Null Counts	Board failure

Fault Description	Possible Cause
Chan A (Slow) RMS Reference Counts	Board failure
Chan B (Slow) RMS Reference Counts	Board failure
Ch A FFT AC Gain Corr LPF=600 Hz Gain=4.5 Freq=300	Board failure
Ch B FFT AC Gain Corr LPF=600 Hz Gain=4.5 Freq=300	Board failure
Ch A FFT AC Gain Corr LPF=1 kHz Gain=4.5 Freq=600	Board failure
Ch B FFT AC Gain Corr LPF=1 kHz Gain=4.5 Freq=600	Board failure
Ch A FFT AC Gain Corr LPF=3.6 kHz Gain=4.5 Freq=2160	Board failure
Ch B FFT AC Gain Corr LPF=3.6 kHz Gain=4.5 Freq=2160	Board failure
Ch A FFT AC Gain Corr 260_970 Hz Gain=2.25 Freq=600	Board failure
Ch B FFT AC Gain Corr 260_970 Hz Gain=2.25 Freq=600	Board failure
Slow Ch A RMS Gain Corr 270_970 Hz Gain=4.5 Freq=600	Board failure
Slow Ch B RMS Gain Corr 270_970 Hz Gain=4.5 Freq=600	Board failure
CHAN A FFT LPF=3.6 kHz Gain=4.5 Freq=0	Board failure
CHAN B FFT LPF=3.6 kHz Gain=4.5 Freq=0	Board failure
CHAN A FFT LPF=600 Hz Gain=1.0 Freq=300	Board failure
CHAN B FFT LPF=600 Hz Gain=1.0 Freq=300	Board failure
CHAN A FFT LPF=600 Hz Gain=2.25 Freq=300	Board failure
CHAN B FFT LPF=600 Hz Gain=2.25 Freq=300	Board failure
CHAN A FFT LPF=600 Hz Gain=4.5 Freq=300	Board failure
CHAN B FFT LPF=600 Hz Gain=4.5 Freq=300	Board failure
CHAN A FFT LPF=1 kHz Gain=4.5 Freq=600	Board failure
CHAN B FFT LPF=1 kHz Gain=4.5 Freq=600	Board failure
CHAN A FFT LPF=3.6 kHz Gain=4.5 Freq=2160	Board failure
CHAN B FFT LPF=3.6 kHz Gain=4.5 Freq=2160	Board failure
CHAN A FFT LPF=3.6 kHz Gain=4.5 Freq=600	Board failure
CHAN B FFT LPF=3.6 kHz Gain=4.5 Freq=600	Board failure
CHAN A FFT LPF=600 Hz Gain=4.5 Freq=706 –12db	Board failure
CHAN B FFT LPF=600 Hz Gain=4.5 Freq=706 –12db	Board failure
CHAN A FFT LPF=1 kHz Gain=4.5 Freq=1192 –12db	Board failure
CHAN B FFT LPF=1 kHz Gain=4.5 Freq=1192 –12db	Board failure
CHAN A FFT LPF=3.6 kHz Gain=4.5 Freq=3854 –6db	Board failure
CHAN B FFT LPF=3.6 kHz Gain=4.5 Freq=3854 –6db	Board failure
CHAN A FFT LPF=600 Hz Gain=4.5 Freq=5 –3db	Board failure
CHAN B FFT LPF=600 Hz Gain=4.5 Freq=5 –3db	Board failure
CHAN A FFT LPF=600 Hz Gain=2.25 Freq=600 –3db	Board failure
CHAN B FFT LPF=600 Hz Gain=2.25 Freq=600 –3db	Board failure
CHAN A FFT LPF=1 kHz Gain=2.25 Freq=1000 – 3db	Board failure
CHAN B FFT LPF=1 kHz Gain=2.25 Freq=1000 – 3db	Board failure
CHAN A FFT LPF=3.6 kHz Gain=2.25 Freq=3600 – 3db	Board failure
CHAN B FFT LPF=3.6 kHz Gain=2.25 Freq=3600 – 3db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=400	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=400	Board failure
CHAN B FFT 260-970Hz Gain=2.25 Freq=400	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=400	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=600	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=600	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=600	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=600	Board failure

Fault Description	Possible Cause
CHAN A FFT 260-970 Hz Gain=2.25 Freq=235 –3db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=235 –3db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=235 –3db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=235 –3db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=220 –9db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=220 –9db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=220 –9db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=220 –9db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=205 –15db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=205 –15db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=205 –15db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=205 –15db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=1065 –3db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=1065 –3db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=1065 –3db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=1065 –3db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=1150 –9db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=1150 –9db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=1150 –9db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=1150 –9db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=1235 –15db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=1235 –15db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=1235 –15db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=1235 –15db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=130 <–36db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=130 <–36db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=130 <–36db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=130 <–36db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=250	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=250	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=250	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=250	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=260	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=260	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=260	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=260	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=270	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=270	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=270	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=270	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=930	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=930	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=930	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=930	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=950	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=950	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=950	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=950	Board failure

Fault Description	Possible Cause
CHAN A FFT 260-970 Hz Gain=2.25 Freq=970	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=970	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=970	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=970	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=990	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=990	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=990	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=990	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=1000	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=1000	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=1000	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=1000	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=1940 <-36db	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=1940 <-36db	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=1940 <-36db	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=1940 <-36db	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=600 50%	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=600 50%	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=600 50%	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=600 50%	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=600 25%	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=600 25%	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=600 25%	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=600 25%	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=600 12.5%	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=600 12.5%	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=600 12.5%	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=600 12.5%	Board failure
CHAN A FFT 260-970 Hz Gain=2.25 Freq=0 0%	Board failure
CHAN A RMS 260-970 Hz Gain=2.25 Freq=0 0%	Board failure
CHAN B FFT 260-970 Hz Gain=2.25 Freq=0 0%	Board failure
CHAN B RMS 260-970 Hz Gain=2.25 Freq=0 0%	Board failure
Chan A Dac Bias V dc Set to 0.0V dc	Board failure
Chan B Dac Bias V dc Set to 0.0V dc	Board failure
Chan A Dac Bias V dc Set to 1.0V dc	Board failure
Chan B Dac Bias V dc Set to 1.0V dc	Board failure
Chan A Dac Bias V dc Set to -1.0V dc	Board failure
Chan B Dac Bias V dc Set to -1.0V dc	Board failure
FFT Chan A A/D Bit Integrity - Peak bin cnts 80-100Hz	Board failure
FFT Chan B A/D Bit Integrity - Peak bin cnts 80-100Hz	Board failure

DDPT Simplex Dynamic Pressure Transducer Input

Functional Description

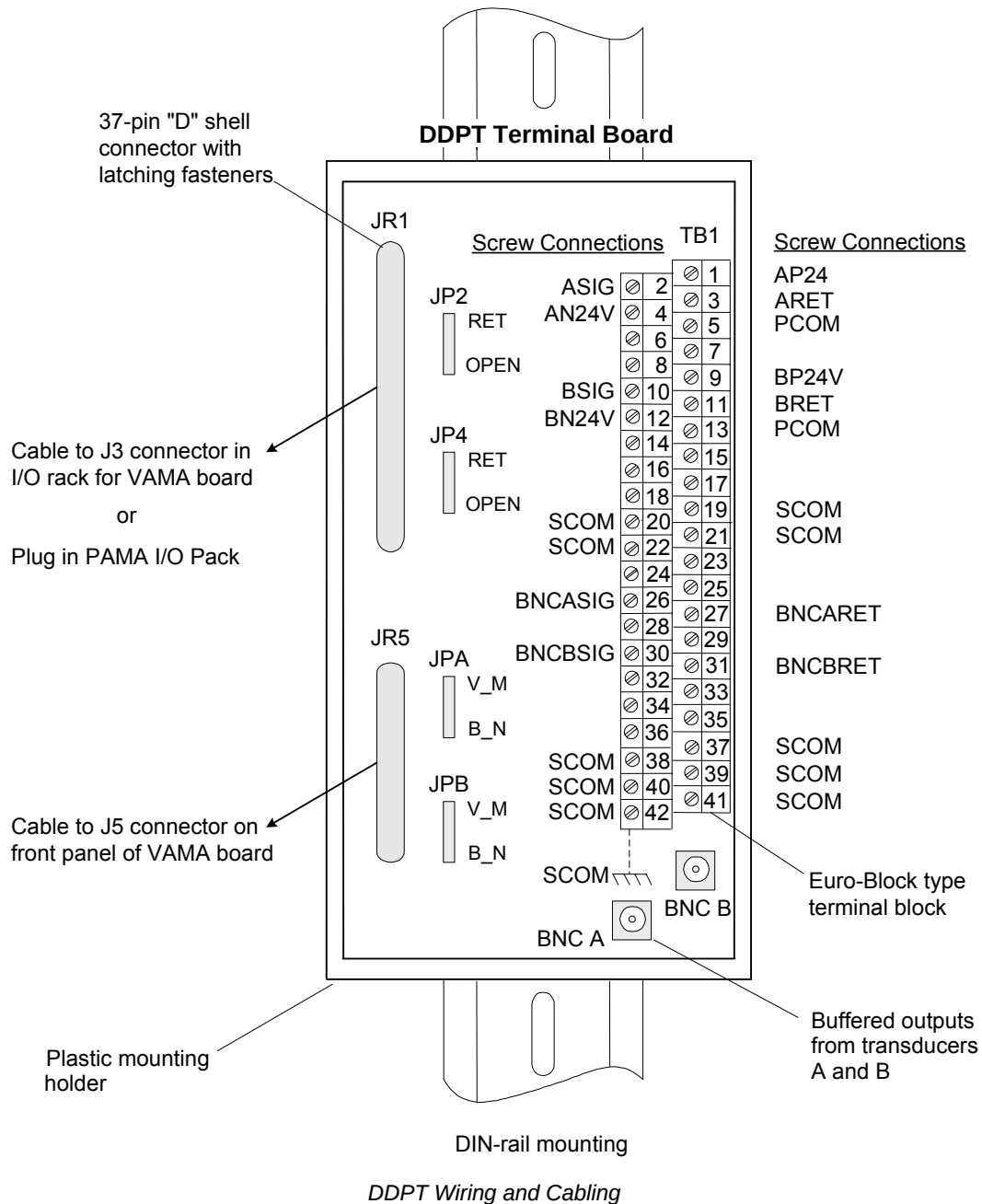
The Simplex Dynamic Pressure Transducer Input (DDPT) terminal board is a compact acoustic terminal board for DIN-rail mounting. The board accepts two pressure transducers for monitoring pressure waves in gas turbine combustion chambers, using either Vibro-Meter[®] or Bently Nevada* transducers. It connects to the VAMA with two cables, and is designed to meet Class 1, Division 2 environmental requirements for hazardous gases.

Note DDPT is only available in a simplex version.

Installation

Mount the plastic holder on the DIN-rail and slide the DDPT board into place. Connect the wires for the pressure transducers to the permanently mounted Euro-Block type terminal block, which has 42 terminals. Typically #18 AWG shielded twisted triplet wiring is used. Ten screws are provided for the SCOM (ground) connection.

Connect cables from the DDPT JR1 connector to the VAMA J3 connector on the lower portion of the VME rack, and from DDPT JR5 connector to the J5 connector on the front panel of the VAMA. These are latching type connectors to secure the cables.



Operation

VAMA supplies a ± 24 V dc to the DDPT to power the pressure sensing equipment. VAMA/DDPT supports the following third party vendor equipment:

- Vibro-Meter Galvanic Separation Unit types GSI 1_
- Bently-Nevada 86517 with modifications 142533 or 159840 charge amplifier
- Bently-Nevada dynamic pressure charge amplifier 350500.

Note The Vibro-Meter GSI 1_ _ unit prevents problems due to voltage differences between the measuring point and signal processing (such as ground loops).

The Vibro-Meter GSI setup conditions a pico-coulomb output from a dynamic pressure transducer (Vibro-Meter CP216 or CP231) through a charge amplifier (Vibro-Meter IPC 704) with a current output representing approximately $125 \mu\text{A/psi}$. The GSI unit provides an output ac signal (approx. ± 2 V peak) that represents the dynamic pressure (gain expressed in mV/psi) riding on top of a dc bias voltage of approximately $+7$ V dc. The GSI unit requires a $+24$ V dc power supply. Normally, the power supply return for the GSI is grounded externally and the PCOM on the terminal board is not used. PCOM should only be used when the external return ground is not used.

The Bently-Nevada 86517 interface module converts the dynamic pressure transducer charge signal from pico-coulombs to milli-volts which represents the pressure in psi. The interface module outputs an ac signal (approx. ± 1.2 V peak) riding on top of a negative dc bias voltage of approximately -10 V dc. The Bently-Nevada unit requires a -24 V dc power supply.

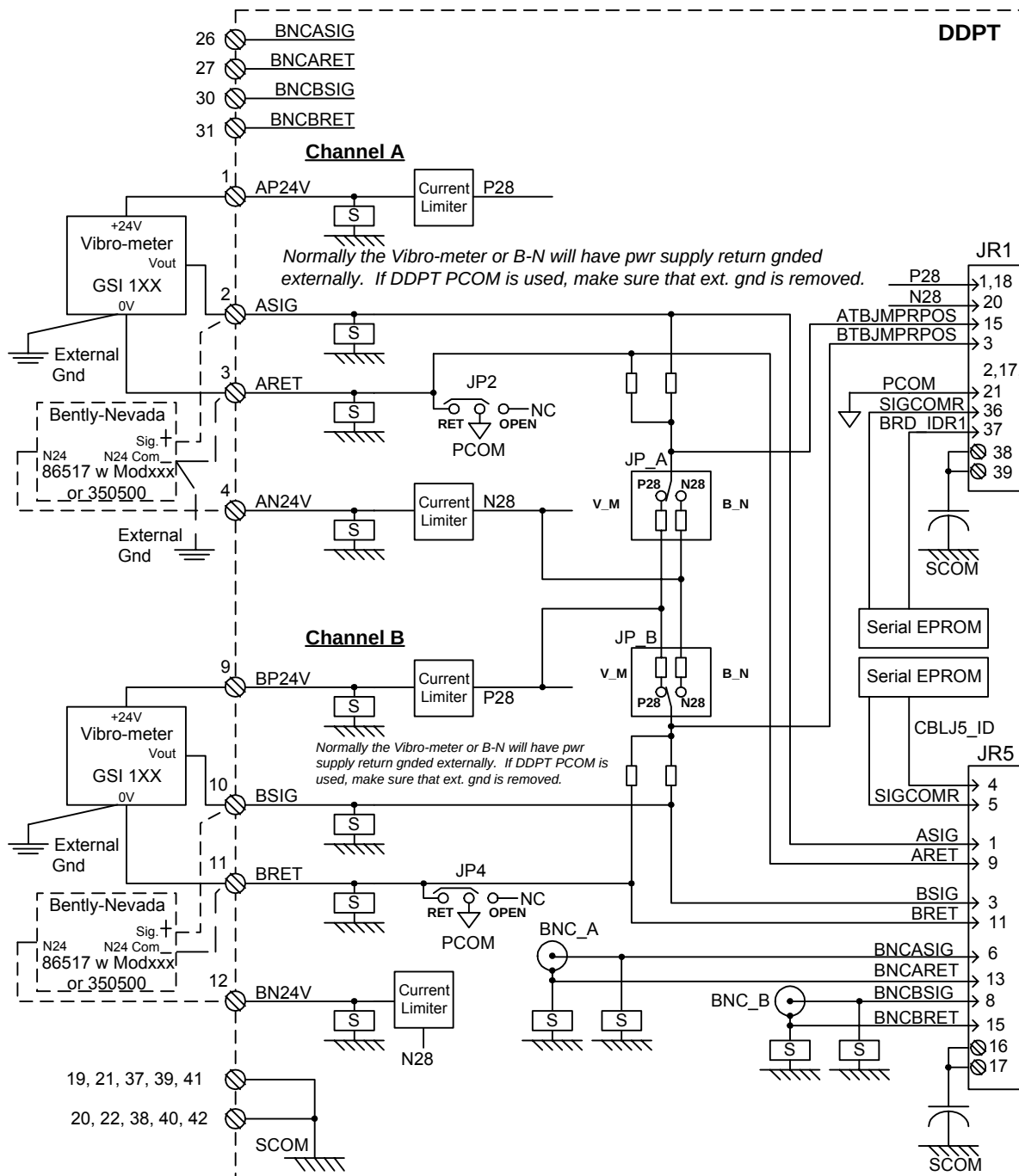
DDPT Vendor Equipment Power Supply Specifications

Vendor	Power Supply	Nominal Voltage	Nominal Current
Vibro-Meter	Positive 24 V dc	$+24$ V dc ($\pm 5\%$)	0.04 A (± 0.02 A)
Bently-Nevada	Negative 24 V dc	-24 V dc ($\pm 5\%$)	0.02 A (± 0.01 A)

The pressure/acoustic signal is read differentially by connecting Pressure Wave Channel A High (ASIG) and Pressure Wave Channel A Low (ARET) to the DDPT inputs. Voltage clamping and high frequency suppression is applied on the DDPT before the signal is routed to VAMA.

The jumpers, JPA and JPB, are used to add a bias corresponding to the dc bias provided by the third party interface unit to detect open circuit conditions. Therefore, a $+28$ V dc bias is added for the Vibro-Meter connection and a -28 V dc bias is added for the Bently-Nevada system. The DDPT board pressure wave outputs are ASIG/ARET for the output pair for channel A and BSIG/BRET for the output pair for channel B.

VAMA provides a buffered signal conditioning circuit for each BNC output on the DDPT terminal board. The BNC buffered circuit takes its input from the ac pressure wave input without the dc bias signal. The gain of the buffer is 1. The signal for the buffered BNC output ranges from 0 to 40 psi peak-to-peak, which is represented by an ac signal with the scaling of 0.1 V/psi.



DDPT Board Block Diagram

Specifications

Item	Specification
Number of Transducers	Two, either: Vibro-Meter Galvanic separation Unit types GSI 1_ __, or Bentley-Nevada 86517, 142533, or 159840 charge amplifier, or Bentley-Nevada 350500 dynamic pressure charge amplifier
Transducer Power Supply	Vibro-Meter: Positive 24 V dc, current of 0.04 A nominal from I/O board Bentley-Nevada: Negative 24 V dc, current of 0.02 A nominal from I/O board
Buffered signal outputs	Two channels with ac component only, 0.1 V/psi, available at BNC outputs
Pressure wave magnitude range	Mag.min = -14 psi Mag.max = +14 psi
Pressure wave frequency range	Fmin = 1.5 Hz Fmax = 3600 Hz
Environment	For use in Class 1, Division 2 environments (hazardous gases)
Temperature	Operating: -30 to 65°C (-22 to 149 °F)
Technology	Surface mount

Diagnostics

VAMA runs continuous diagnostic tests on the signals and hardware. Conditions such as open-wire on the transducers is checked. If any signals go outside of configured limits, VAMA creates a fault. The cable connectors on DDPT have their own ID device that is interrogated by VAMA. The ID device is a read-only chip coded with the terminal board serial number, board type, and revision number. If a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Two jumpers set the bias voltage for the transducers, and two jumpers set the power return from the transducers:

- JPA and JPB apply either a +28 V bias or -28 V bias to the transducer signals.
- JP2 and JP4 connect the transducer power return to PCOM or to Open.

Refer to the *Installation* and *Operation* sections for further details.

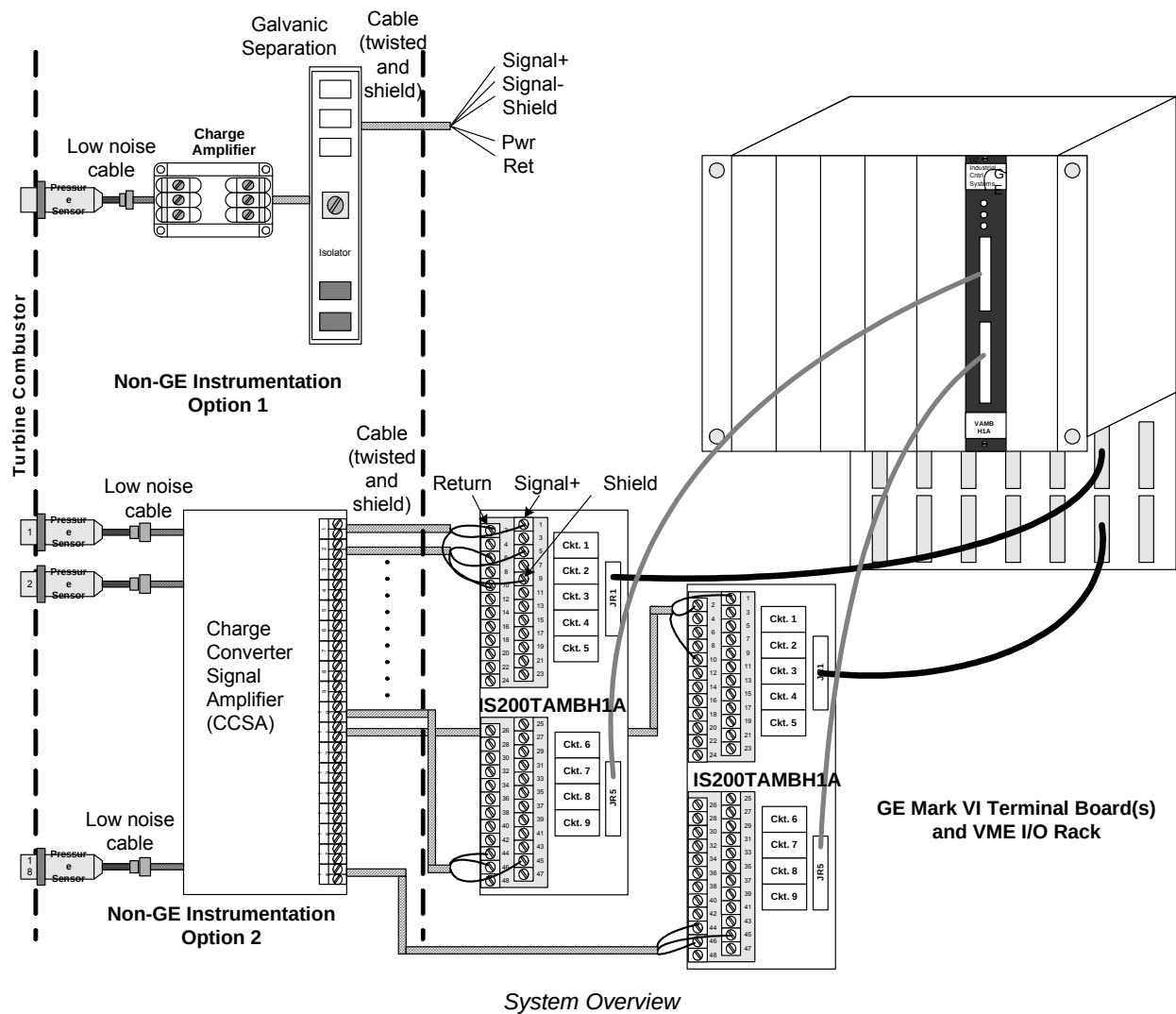
Notes

VAMB Acoustic Monitoring Input

VAMB Acoustic Monitoring

Functional Description

The Acoustic Monitoring (VAMB) board provides 18 channels of signal conditioning through two nine channel acoustic monitoring terminal boards IS200TAMB (TAMB) and one 18 channel I/O acoustic monitoring sub-assembly IS215VAMB (VAMB). The TAMB supports third party vendors such as, Bentley-Nevada[®], Vibro-meter[®], GE/Reuter-Stokes[®], and others.



The selected product combination determines the system requirements as follows:

- 18 channels of signal conditioning for sensing dynamic pressure output from third party charge amplifiers
 - Bentley-Nevada, Vibro-meter, PCB Piezotronics®, GE PS CCSA and GE/Reuter-Stokes vendors are supported
 - Differential inputs and adjustable gains
 - Fast synchronous-sampled analog/digital with 8x over-sampling capability to minimize analog filtering
 - Field Programmable Gate Array (FPGA) pre-processor with Finite Impulse Response (FIR) filters
 - Open wire detection
- Analysis capability per channel
 - Proprietary functions
 - RMS value for the ac input signal
 - Alarm detection if peak amplitude exceeds configurable level
 - List captures capability for all 18-channels if an alarm is detected

The acoustic monitoring function for the frame 6, 7, or 9 size gas turbines is supported by the VAMB and either one or two TAMB terminal boards. The TAMB receives an mV output from the CCSA or a third party charge amplifier. Power for the charge amplifier is supplied by the TAMB using a current limited +24V or -24V supply or from an external source. Other than electro-magnetic transient suppression, the differential input signal is routed directly to the VAMB through a cable with 18 twisted-pairs to the Versa Module Eurocard (VME) card front edge.

Gas Turbine Frame Size	No. of Combustors	No. of Flame Detectors	No. of VAMB I/O	No. of TAMB	Max. No. of channels supported
6FA	6	4	1	1	9
7EA	10	8	1	2	18
7FA, 7FB	14	4	1	2	18
9FA	18	4	1	2	18

Installation

Note A GE field service technician should install the VAMB. Technicians should refer to *GII-100014, VAMB Acoustic Monitoring Module*, for complete installation instructions.

The figure TAMB Acoustic Monitoring Terminal Board shows the functionality of one of the nine channels supported on the TAMB. Each channel provides current limited +24 V dc and +24 V dc power supply outputs. A constant current source is connected to the SIGx line for the PCB sensors. The input signal, CCSELx, is False when the signal is a logic-level low through an output on the VAMB. At power-up, the output must be False (logic-level low), leaving the constant current output deselected until the configuration parameters are loaded.

Each channel provides a hardware jumper, JPx, where x equals an even number, which selects a current input, I_IN, or a voltage input, V_IN. The current input provides a 250 W burden resistor for any 4-20 mA circuits connected to that channel.

Each channel has a jumper, JP_x, where x equals an odd number, which checks whether the return line, RET_x, is tied to the terminal board's power common, PCOM. If JP_x= PCOM, then the RET_x line is tied to PCOM. If JP_x= OPEN, then the RET_x line is not tied to PCOM.

A high impedance dc bias allows the VAMB to detect an open connection between the charge amplifier or sensor and the TAMB. The dc bias control provides three options:

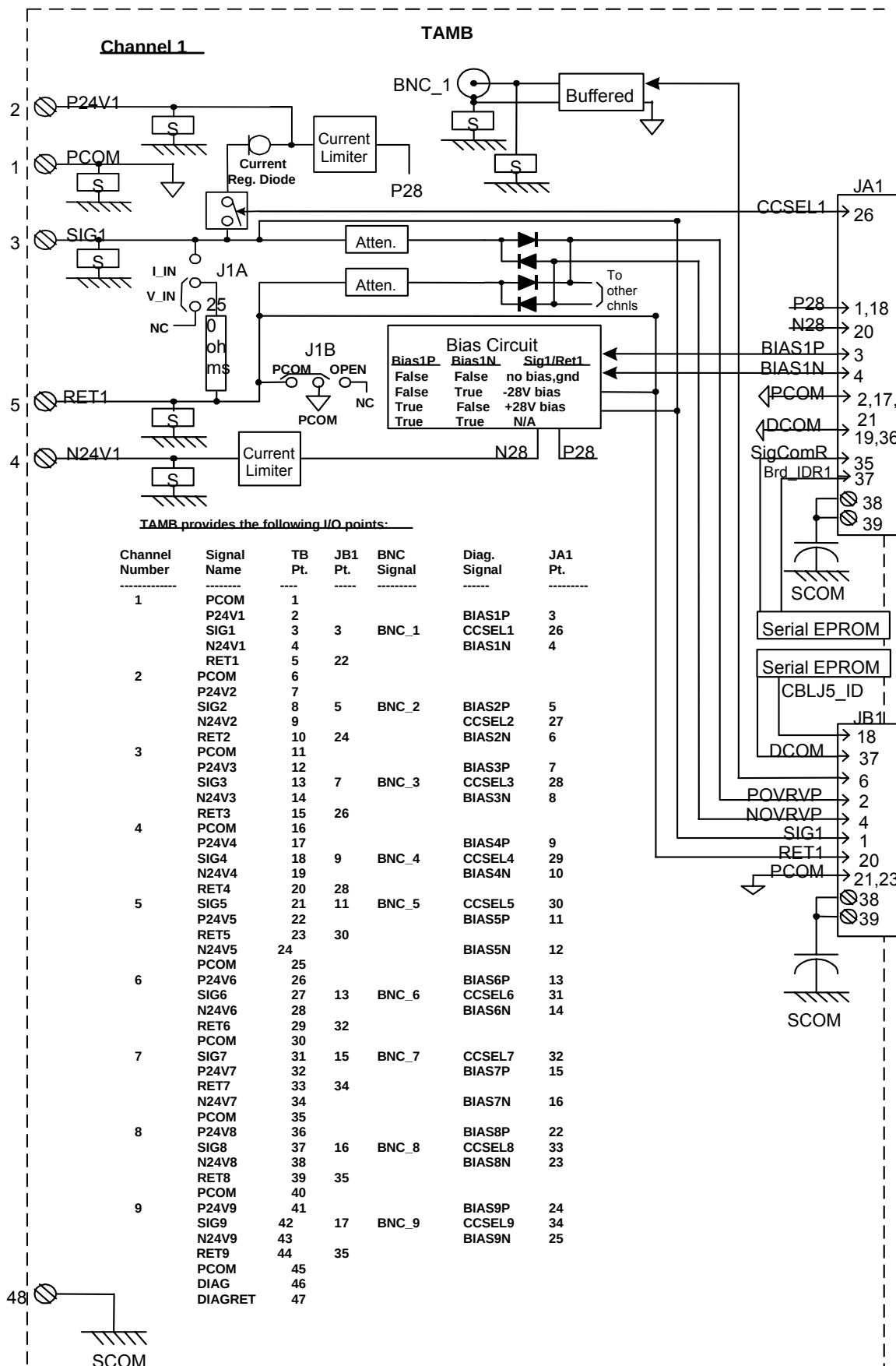
- 28 V bias or ground applied to the signal line
- SIG_x and return line
- RET_x

These inputs are activated or the signal select is True if the Mark* VI I/O board outputs a logic-level low signal from the TTL output. The table shows the selections:

BIAS _x P	BIAS _x N	SIG _x /RET _x Biased to
True	True	Illegal combination. Bias circuit protects power supplies from shorting
True	False	+28 V bias selected
False	True	-28 V bias selected
False	False	No bias selected, but both SIG _x and RET _x are pulled to ground to keep the unused input electrically quiet.

The sensor or charge amplifier signal output is connected to the terminal board point, SIG_x, and the Kelvin or low-current return is connected to RET_x. The terminal board provides signal suppression and EMI protection and passes the signal on to the VAMB through a 37-pin connector.

Each channel provides a buffered BNC output. The buffered signal is the input signal minus the dc bias.



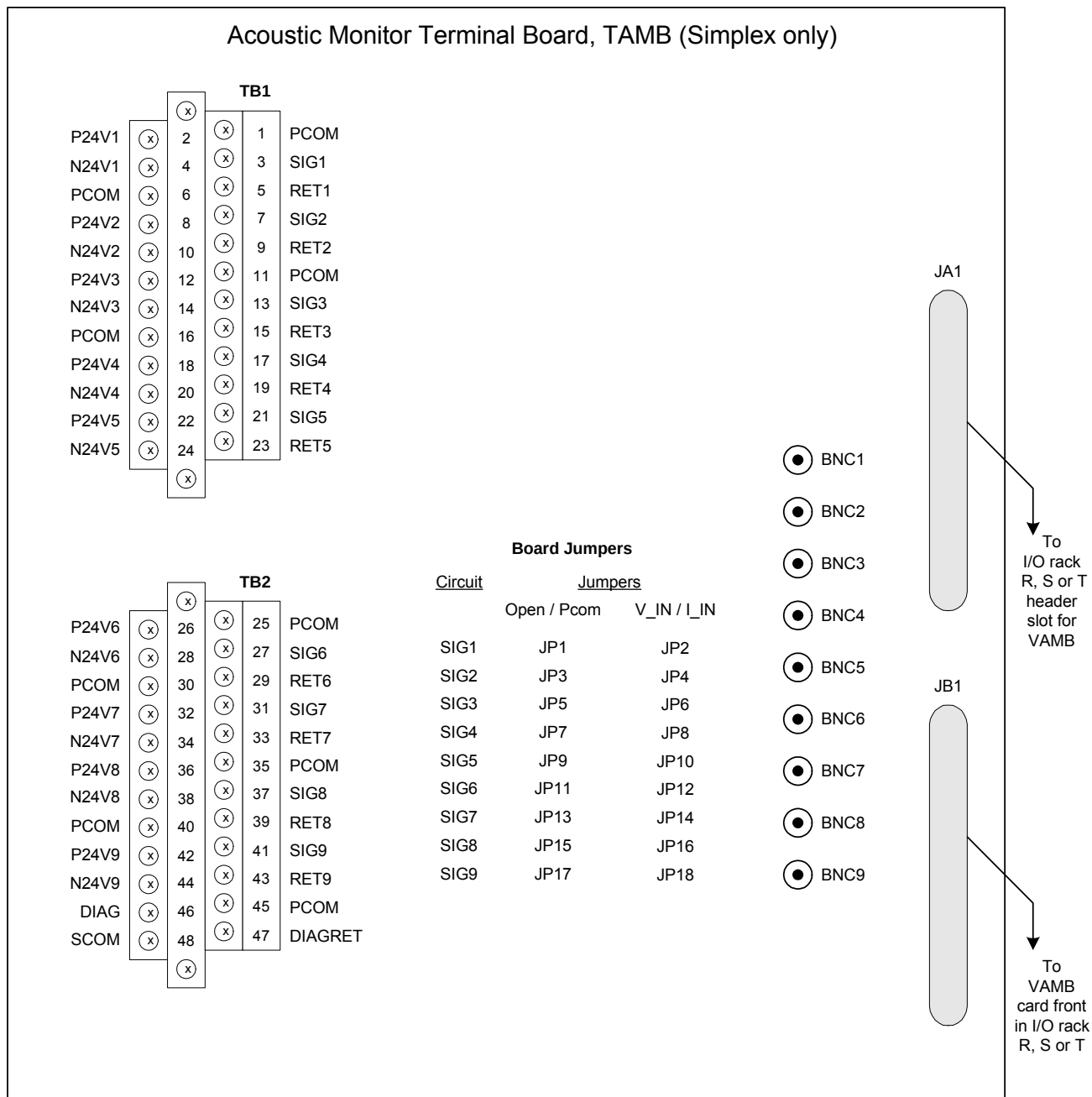
TAMB Acoustic Monitoring Terminal Board

Terminal Point Definitions

Signal Name	Pin #	Description of 48-pin Customer Terminal Points
PCOM	1	Power supply returns for either the P24 V or N24 V supply
P24V1	2	+24 V output feed for input #1's charge amplifier (used with Vibro-meter equipment)
SIG1	3	Dynamic pressure differential voltage input #1 signal side
N24V1	4	-24 V output feed for input #1's charge amplifier (used with Bently-Nevada equipment).
RET1	5	Dynamic pressure differential voltage input #1 return
PCOM	6	Power supply returns for either the P24 V or N24 V supply
P24V2	7	+24 V output feed for input #2's charge amplifier (used with Vibro-meter equipment)
SIG2	8	Dynamic pressure differential voltage input #2 signal side.
N24V2	9	-24 V output feed for input #2's charge amplifier. (used with Bently-Nevada equipment)
RET2	10	Dynamic pressure differential voltage input #2 return
PCOM	11	Power supply returns for either the P24 V or N24 V supply.
P24V3	12	+24 V output feed for input #3's charge amplifier (used with Vibro-meter equipment)
SIG3	13	Dynamic pressure differential voltage input #3 signal side.
N24V3	14	-24 V output feed for input #3's charge amplifier. (used with Bently-Nevada equipment)
RET3	15	Dynamic pressure differential voltage input #3 return
PCOM	16	Power supply returns for either the P24 V or N24 V supply
P24V4	17	+24 V output feed for input #4's charge amplifier (used with Vibro-meter equipment)
SIG4	18	Dynamic pressure differential voltage input #4 signal side
N24V4	19	-24 V output feed for input #4's charge amplifier (used with Bently-Nevada equipment)
RET4	20	Dynamic pressure differential voltage input #4 return
SIG5	21	Dynamic pressure differential voltage input #5 signal side
P24V5	22	+24 V output feed for input #5's charge amplifier (used with Vibro-meter equipment)
RET5	23	Dynamic pressure differential voltage input #5 return
N24V5	24	-24 V output feed for input #5's charge amplifier. (used with Bently-Nevada equipment)
PCOM	25	Power supply returns for either the P24 V or N24 V supply
P24V6	26	+24 V output feed for input #6's charge amplifier (used with Vibro-meter equipment)
SIG6	27	Dynamic pressure differential voltage input #6 signal side
N24V6	28	-24 V output feed for input #6's charge amplifier (used with Bently-Nevada equipment)
RET6	29	Dynamic pressure differential voltage input #6 return
PCOM	30	Power supply returns for either the P24 V or N24 V supply
SIG7	31	Dynamic pressure differential voltage input #7 signal side
P24V7	32	+24 V output feed for input #7's charge amplifier (used with Vibro-meter equipment)
RET7	33	Dynamic pressure differential voltage input #7 return
N24V7	34	-24 V output feed for input #7's charge amplifier (used with Bently-Nevada equipment)
PCOM	35	Power supply returns for either the P24 V or N24 V supply
P24V8	36	+24 V output feed for input #8's charge amplifier (used with Vibro-meter equipment)
SIG8	37	Dynamic pressure differential voltage input #8 signal side
N24V8	38	-24 V output feed for input #8's charge amplifier (used with Bently-Nevada equipment)
RET8	39	Dynamic pressure differential voltage input #8 return
PCOM	40	Power supply returns for either the P24 V or N24 V supply
P24V9	41	+24 V output feed for input #9's charge amplifier (used with Vibro-meter equipment)
SIG9	42	Dynamic Pressure differential voltage input #9 signal side
N24V9	43	-24 V output feed for input #9's charge amplifier (used with Bently-Nevada equipment)
RET9	44	Dynamic pressure differential voltage input #9 return

Signal Name Pin # Description of 48-pin Customer Terminal Points

PCOM	45	Power supply returns for either the P24 V or N24 V supply
DIAG	46	Diagnostic DAC output
DIAGRET	47	Return for diagnostic DAC output
SCOM	48	Shield ground

*Acoustic Monitor Terminal Board, TAMB*

TAMB Jumper Settings

Vendor	Vendor Model	Vendor I/O Conn.	TAMB Terminal Point (x=1 to 9)	TAMB Jpn (n=even number) Position	TAMB Jpn (n=odd number) Position
Bently-Nevada	350500 3-wire method	NC	P24Vx	V_IN	PCOM
		OUT	SIGx		
		COM	RETx		
		VT	N24Vx		
		NC	PCOM		
Bently-Nevada	350500 4-wire method (better than 3-wire)	NC	P24Vx	V_IN	Open
		OUT	SIGx		
		COM	RETx		
		VT	N24Vx		
		COM	PCOM		
Vibro-meter	IPC 620 or IPC 704 with GSI 122 or 130 3-wire method	+24V	P24Vx	V_IN	PCOM
		VOUT	SIGx		
		0V	RETx		
		NC	N24Vx		
		NC	PCOM		
Vibro-meter	IPC 620 or IPC 704 with GSI 122 or 130 4-wire method	+24V	P24Vx	V_IN	Open
		VOUT	SIGx		
		0V	RETx		
		NC	N24Vx		
		0V	PCOM		
GE Power System's Charge Converter Signal Amp (CCSA)	CCSA	NC	P24Vx	V_IN	Open
		OUT+	SIGx		
		OUT-	RETx		
		NC	N24Vx		
		NC	PCOM		
PCB Piezotronics	111A21, 102A05, 102M43, 102M158, 102M170, 102M174	NC	P24Vx	V_IN	PCOM
		Signal	SIGx		
		Ground	RETx		
		NC	N24Vx		
		NC	PCOM		
GE / Reuter-Stokes	Flame Tracker RS-FS -9001 & -9002 -9004, -9005 & -9006	+ conn.	P24Vx	I_IN	PCOM
		- conn.	SIGx		
		NC	RETx		
		NC	N24Vx		
		NC	PCOM		

Operation

The VAMB software features include:

- 18 channels of acoustic monitoring with
 - Synchronous sampling of all 18 channels of data
 - Configuration of TAMB terminal board controlling open circuit test voltage and constant current mode
 - A/D gain and offset adjustment
 - Dc bias removal from dynamic pressure signal to maximize SNR
 - Proprietary firmware functions
 - RMS calculation of the sampled AC signal data.

Milli-volt to engineering unit's conversion of RMS value

- Configuration constants can be changed through Mark VI toolbox
- 40 ms frame rate updates for signal space variables used by the application software
- Offline and online diagnostics to check the hardware

A/D Compensation

The A/D compensation function nulls any gain or offset error due to initial component variances. The firmware has an auto-calibration function built in for the A/Ds it controls. The auto-calibration function compares each of the 18 analog channels against a gold standard A/D channel. The gold standard A/D channel is calibrated using a standard high-precision voltage reference and the A/D common.

Note Refer to the figure, *Channel x Acoustic Monitoring Block Diagram*, where x equals 1-18.

Input Units to Engineering Value Conversion

The Acoustic Monitoring function provides a conversion from the hardware input units to the engineering units needed for the system calculation. For the mV to psi conversion, the range is 20 to 600 mV per psi. The firmware will be given four configuration parameters per channel to define the equation for the transfer function.

Value (engineering units in counts) = GUnitConversion * Input (milli-volts in counts) + Offset

where

$$\text{GUnitConversion} = (\text{High\_Value} - \text{Low\_Value}) / (\text{High\_Input} - \text{Low\_Input})$$
$$\text{Offset} = \text{High\_Value} - \text{GUnitConversion} * \text{High\_Input}$$

where High_Value, Low_Value, High_Input + Low Input are the configuration parameters.

A/D Gain Adjust

The configuration parameter, Gain defined for each channel controls the channel gain in the hardware. This allows for the amplification of low level signals to provide better resolution in the analog to digital conversion hardware. The gain options are 1, 2, 4 and 8. The channel control writes the gain set up to the FPGA VSPA input amplifier 4x and 2x gain control registers. The signal level calculated by the VAMB firmware will not change with a change in the Gain parameter because the signal is divided by the Gain factor in the firmware to result in a net gain of 1 for the signal regardless of the gain factor used. The maximum expected signal level should not exceed 10 V (saturation) after the gain is applied as indicated in the following table.

Rules for selecting proper value for Gain

Gainx	Maximum magnitude of input signal after dc bias is removed (volts)
1	10
2	5
4	2.5
8	1.25

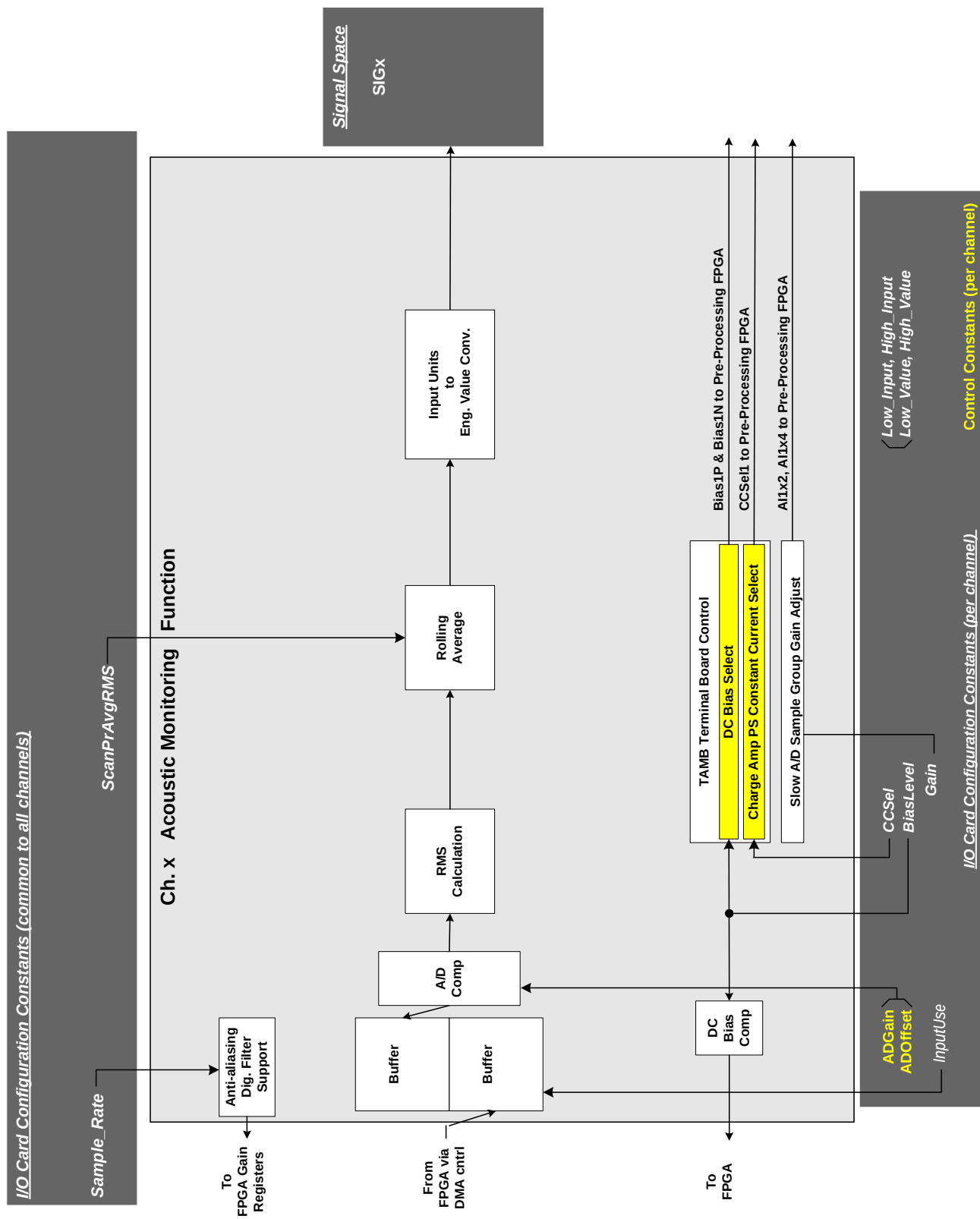
Rms Calculation and Rolling Average

The root-mean-square (rms) calculation performs an rms calculation on the ac acoustic information sampled for a given scan. The rms is defined as follows:

$$\text{rms\_Chx} = \text{SQRT} \left((\text{AC\_Input}(0)**2 + \text{AC\_Input}(1)**2 + \dots + \text{AC\_Input}(\text{Buffer\_Length})**2) / \text{Buffer\_Length} \right)$$

Where x is the channel number.

The rolling average provides a smoothing function to reduce the vibration in the signal.



Channel x Acoustic Monitoring Block Diagram

Specifications

Signal Input Accuracy

Requirement	Limits
RMS Calculation Accuracy for Gain = 1, 2, 4 or 8 volts / volt	±2.0% full scale
Peak-to-Peak FFT Calculation Accuracy for Gains = 1, 2, 4 or 8 volts / volt	±0.5% full scale from 0 to 1600 Hz ±1.5% full scale from 1601 to 3200 Hz

Power Supply

Requirement	Limits
Number of P24 dual-mode outputs (one current-limit output, P24 Vx and one constant current output tied to SIGx selectable through CCSELx)	9 (one per channel)
P24 V (current-limit mode selected)	+22.8 to +25.2 V dc
P24 nominal current (current-limit mode selected) (due to standing current of IPC 704 on GSI 122/130)	44 mA ±10%
P24 minimum/maximum peak current range (current-limit mode selected) (due to ±5 mA ac signal component plus some over range riding on top of standing current of IPC 704 connected to GSI 122/130 from Vibro-meter)	20 – 60 mA
P24 V (constant current mode selected with supply tied to SIGx)	+20 to +30 V dc
P24 nominal current (constant current mode selected)	3.5 mA ±10%
Constant current input type	TTL
Constant current selection logic level for TRUE state. (TAMB ckt. provides a pull-up for the input.)	High
Number of N24 current-limited outputs	9 (one per channel)
N24 V	-18.85 to -26 V dc
N24 nominal current	20 mA
N24 maximum load current	30 mA

Jumper Selections

Requirement	Limits
Number of JPx (even) 3-pin jumpers with one side tied to the signal line, SIGx and the opposite side left open with the center pin tied to the 250 W burden resistor.	9 (one per channel)
Silk screen label for connection from signal line, SIGx to the 250 W burden resistor.	I_IN
Silk screen label for connection from the 250 Ω burden resistor to no-connect pin (open).	V_IN
Number of JPx (odd) 3-pin jumpers with one side tied to the return signal, RETx, and the opposite side left open with the center pin tied to PCOM.	9 (one per channel)
Silk screen label for connection from signal return, RETx to PCOM	PCOM
Silk screen label for connection from PCOM to no connect pin.	OPEN

Requirement	Limits
Number of TAMB channels with bias control.	9 (one per channel)
Control input signal type	TTL
Bias control input true state	Logic high
Dc error to dynamic signal channel produced by the bias control.	< 0.5 %

Constant Current Select for P24

Requirement	Limits
Number of constant current control inputs	9 (one per channel)
Control input signal type	TTL

Buffered BNC Outputs

Requirement	Limits
Number of buffered BNC outputs	9 (one per channel)
Dc gain (Dc bias is removed from signal)	1 $\pm$ 0.5 %
Allowable offset	30 mV $\pm$ 10%
Output impedance	40 Ω $\pm$ 50%
J6 connector type for QC	25-pin D shell

Diagnostics

Three LEDs at the top of the VAMB front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED is normally off but displays a steady orange if a diagnostic alarm exists in the board.

Each input has system limit checking based on two configurable levels. These limits can be configured for enable/disable, $\geq$ or $\leq$, and as latching/nonlatching. RESET_SYS resets the out of limits. If this limit is exceeded a system limit logic signal is set.

Each input has sensor limit checking, open circuit detection, and dc bias autonulling and excessive dc bias detection. Alarms will be generated for these diagnostics. Refer to *I/O Board Alarms and Point Configuration*. RESET_SYS resets these alarms.

The TAMB terminal board has its own ID device, which is interrogated by the I/O board. The board is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. This ID is checked as part of the power-up diagnostics.

Configuration

Note The following information is extracted from the ToolboxST application and represents a sample of the configuration information for this board. Refer to the actual configuration file within the ToolboxST application for specific information.

Module Parameter	Description	Choices
BinReject	Defines the number of side bins that will be rejected when the search function is applied to the FFT results for channels 1 through 18. 0 = no bins rejected	0 to 6
Config_Mode	Defines the source of the currently active configuration. The Toolbox allows only mode Toolbox as a selection. The remote gateway configurator forces mode to tuning configurator without user control.	Toolbox only
FFT_Length	Defines the number of samples that will be used in the FFT calculation. Selections are: 1024, 2048, 4096, 8192, 16382, and 32768..	1024 to 32768
FFT_TF_SelA	Boolean that selects the internal test file as the input to all the acoustic monitoring channels instead of the actual analog input signals.	HW_Input to File
EventLstSel	Defines the sample site for the event capture list. Disable: list not used FFT_Out; fft output scaled in volts TC_Out: fft output after transducer compensation PSI_Out: fft outputs scaled in PSI Avg_Out: PSI_Out after averaging filter	Disable to Avg_Out
HiB_Limit	Defines the limit level for the maximum peak-peak amplitude signal in the high frequency band.	0 to 50 Psi
HiScrChBrkPt	Defines the frequency boundary between the high and screech frequency bands.	0 to 3200 Hz
LoLoB_Limit	Defines the limit level for the maximum amplitude signal in the low-low frequency band.	0 to 50 Psi
LowB_Limit	Defines the limit level for the maximum amplitude signal in the low frequency band.	0 to 50 Psi
LowLow_EndPt	Defines the ending frequency of the low-low frequency band.	0 to 3200 Hz
LowLowStrtPt	Defines the starting frequency of the low-low frequency band.	0 to 3200 Hz
LowMid_BrkPt	Defines the frequency boundary between the low and mid frequency bands.	0 to 3200 Hz
Low_StrtPt	Defines the starting frequency of the low band.	0 to 3200 Hz
MidB_Limit	Defines the limit level for the maximum amplitude signal in the mid frequency band	0 to 50 Psi
MidHi_BrkPt	Defines the frequency boundary between the mid and high frequency bands.	0 to 3200 Hz
NumEventScns	Defines the number of scans an event buffer will contain. *note if the sample location is set to Raw_Input the maximum scan allowed is 1.	1 to 32 Scans
OpLstSel	Defines the sample site for the spectrum on demand capture or diagnostic list. Selections are: Disable: list not used Raw_Input: input time domain data FFT_Out; fft output scaled in volts TC_Out: fft output after transducer compensation PSI_Out: fft outputs scaled in PSI Avg_Out: PSI_Out after averaging filter	Disable to Avg_Out Bool

Module Parameter	Description	Choices
PL_Fil_Freq	Defines the power line frequency that the notch filter will remove from the spectral content of the FFT output. Selections are 50 or 60 Hz.	50_Hz to 60_Hz
PL_Fil_Tol	Tolerance for power line filter signature calculated vs theoretical. Ten percent tolerance is 0.1.	0 to 1.0
PL_Fil_Width	Defines the bandwidth of the power line notch filter. The bandwidth will be $\pm$ value entered centered about the configured power line frequency.	0 to 100 Hz
SampleRate	Sample rate defines the FFT sample rate for all the acoustic monitoring channels 1–18. Selections are: 12,877 Hz only.	12,877 Hz only
ScanPrAvgFFT	Number of scans per average in the acoustic monitoring filtered FFT output. Selections are: integers 1–32	1 to 32 scans
ScanPrAvgRMS	Number of scans per average in the RMS calculation. Selections are: integers 1–32	1 to 32 scans
SearchInAvg(1) SearchInAvg(6)	Selects whether the sort function for the pk-pk amplitudes uses the present scan only or uses an averaged value	No average, Average
Session_Time	Scheduled time for temporary configuration mode. This time is forced to zero in the Toolbox. This value shall be set to the user-selected time in the temporary gateway remote configurator.	0 to 480 minutes
ScrchB_Limit	Defines the limit level for the maximum amplitude signal in the screech frequency band.	0 to 50 Psi
Scrch_EndPt	Defines the ending frequency of the screech frequency band.	0 to 3200 Hz
SysLimitDis	Enable all system limit checking.	Disable, Enable
T_FilWidth	Width ($\pm$ Hz) of the filter that excludes the transverse frequency fft coefficients and all fft coefficients designated by this filter from the screech band search.	0 to 100 Hz
TMC_Gain(1) – TMC_Gain(30)	Transducer mounting compensation gain values for 30 points to characterize the gain response.	0 to 10
TMC_Freq(1) – TMC_Freq(30)	Frequency corresponding to the gain value entered. Each of the 30 gain points has a corresponding frequency value.	0 to 3200 Hz
TrnsB_Limit	Defines the limit level for the maximum amplitude signal in the transverse frequency band.	0 to 50 Psi
Trns_Bnd_Enb	Enable calculations associated with the transverse band and excludes its FFT coefficients from the screech band.	Disable, Enable
Trns_EndPt	Defines the ending frequency of the transverse frequency band.	0 to 3200 Hz
Trns_StrtPt	Defines the starting frequency of the transverse frequency band.	0 to 3200 Hz
WindowSelect	Selects the windowing function to be used on the sampled data for both Channel A and B. Rectangular Hamming Hanning Triangular Blackman Blackman-Har(ris) Flat Top	Rectangular to Flat Top
ZoomCanSel	Selects one of the 18 acoustic monitoring cans to zoom in on. Selections are: None Can_1 through Can_18	0 to 18
ZoomFFTLngth	Defines the Zoom FFT Length of the input buffer.	1024, 2048, 4096, 8192, 16384, 32768

Module Parameter	Description	Choices
ZmEvtLstSel	Defines the sample site for the zoom event capture list. Selections are: Disable, FFT_Out, TC_Out, PSI_OUT, and Avg_Out	Disable to Avg_Out
ZmOpLstSel	Defines the sample site for the zoom operator capture list. Selections are: Disable: list not used Raw_Input: input time domain data FFT_Out: fft output scaled in volts TC_Out: fft output after transducer compensation PSI_Out: fft outputs scaled in PSI Avg_Out: PSI_Out after averaging filter	Disable to Avg_Out

Terminal Point Configuration

Module Parameter Sig1	Description First of 9 analog inputs - board point	Choices Point volts RMS
Gain	Analog Input resolution adjustment used to amplify signal before digital conversion. Gain factor * (maximum signal peak voltage) must be less than 10 volts to prevent saturation. Selections: 1, 2, 4, and 8	1,2,4, 8 Volts / Volt
BiasLevel	BiasLevel is a dc bias voltage subtracted from the analog signal inputted for the dc bias compensation and used by the TAMB dc bias select. Only used when InputUse is either custom or file.	-11.6 to + 11.6 V dc
Can_Id	Combustor can be wired to this terminal board signal. This normally corresponds to the signal number to avoid confusion; wire terminal board signal 1 to can 1.	1 to 18
CCSel	If constant current select is equal to 1 then the P24 voltage supply is configured as a constant current supply providing a 4 mA output. Only used when InputUse is set to custom.	False, True .
High_Input	Defines point 2 x-axis value in milli-volts for TAMB terminal point that is used in calculating the gain and offset for the conversion to engineering units.	0 to 9998.8 mV
High_Value	Defines point 2 Y-axis value in engineering units for TAMB terminal point that is used in calculating the gain and offset for the conversion from milli-volts to engineering units.	0 to 99999 PSI
InputUse	Selects the sensor type used on the signal. Selections are: Unused, Bently-Nevada, Vibro-meter, Vibro-mA(current), 4 CCSA, PCB, GE/RS (Reuter Stokes), Custom,– File(test data stored in VAMB)	Unused To File
Low_Input	Defines point 1 x-axis value in milli-volts for TAMB terminal point that is used in calculating the gain and offset for the conversion to engineering units.	0 to 9998.8 mV
Low_Value	Defines point 1 Y-axis value in engineering units for TAMB terminal point that is used in calculating the gain and offset for the conversion from milli-volts to engineering units.	0 to 99999 PSI
PL_Fil_En	Enables the power line notch filter.	Disable, Enable
DiagHighEnab	Enables high input sensor limit diagnostics.	Disable, Enable
DiagLowEnab	Enables low input sensor limit diagnostics.	Disable, Enable
OcBiasEnab	Enables bias for open circuits.	Disable, Enable
BiasNullEnab	Enables automatic dc bias nulling.	Disable, Enable
DiagOCChk	Enables open sensor error diagnostic test.	Disable, Enable
DiagBiasNull	Enables excessive dc bias diagnostic test.	Disable, Enable
DiagSigSat	Enables signal saturation diagnostic test.	Disable, Enable
SysLim1Enabl	Enables system limit 1 fault check.	Disable, Enable
SysLim1Latch	Selects whether a fault is latching.	NotLatch, Latch
SysLim1Type	Selects how the test values are compared.	<=, >=
SysLimit1	Value to use for system limit comparison.	-1000 to 1000 Psi

Module	Parameter Sig1	Description First of 9 analog inputs - board point	Choices Point volts RMS
SysLim2Enabl		Enables system limit 2 fault check.	Disable, Enable
SysLim2Latch		Selects whether a fault is latching.	Not Latch, Latch
SysLim2Type		Selects how the test values are compared.	<=, >=
SysLimit2		Value to use for system limit comparison.	-1000 to 1000 Psi

VAMB Board Points

Board Points (Signals)	Description – Point Edit(Enter Signal Connection)	Direction	Type
L3DIAG_VAMB1	Board Diagnostic	Input	BIT
L3DIAG_VAMB2	Board Diagnostic	Input	BIT
L3DIAG_VAMB3	Board Diagnostic	Input	BIT
Can1_Health	Combustor can 1 signal health	Input	BIT
:	:		
Can18_Health	Combustor can 18 signal health	Input	BIT
Sig1_SysLim1	Terminal board signal 1 outside of system limits 1	Input	BIT
:	:		
Sig18_SysLim1	Terminal board signal 18 outside of system limits 1	Input	BIT
Sig1_SysLim2	Terminal board signal 1 outside of system limits 2	Input	BIT
:	:		
Sig18_SysLim2	Terminal board signal 18 outside of system limits 2	Input	BIT
Test_Config	Card is temporarily remotely configured	Input	BIT
Test_Mode	Signals are from internal test sources, not from terminal board	Input	BIT
TripCapList	A capture list triggered by TripCapReq is available	Input	BIT
UserCapList	A capture list manually requested by a user is available	Input	BIT
VambBool_1	General Electric Proprietary Information	Input	BIT
:	:		
VambBool_6	General Electric Proprietary Information	Input	BIT
VambPt_0	General Electric Proprietary Information	Input	INTEGER
:	:		
VambPt_263	General Electric Proprietary Information	Input	INTEGER
Num_Of_Scans	Scan (block of FFT data) number of this data (1-32)	Input	INTEGER
Num_Avg_Scns	Number of scans (block of FFT data) averaged (1-32)	Input	INTEGER
Session_Tmr	Time remaining for remote tuning session	Input	INTEGER
Trip_Cap_Req	Request for trip capture buffer collection	Input	BIT

Alarms

I/O Board Diagnostic Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC Failure Override is Active	Board firmware programming error (board will not go online)
16	System Limit Checking is Disabled	System limit checking was disabled by configuration
18	Incorrect J3 Terminal Board ID	Cable to J3 connector not properly connected to a TAMB terminal board or terminal board defective.
19	Incorrect J4 Terminal Board ID	Cable to J4 connector not properly connected to a TAMB terminal board or terminal board defective.
20	Incorrect J6 Terminal Board ID	Cable to J6 connector not properly connected to a TAMB terminal board or terminal board defective.

Fault	Fault Description	Possible Cause
21	Incorrect J7 Terminal Board ID	Cable to J7 connector not properly connected to a TAMB terminal board or terminal board defective.
30	ConfigCompatCode Mismatch;Firmware:#.Tre:#.	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode Mismatch;Firmware:# Tre:#	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
38	Flashdisk error: Unable to revert to flash configuration after remote access	Permanent configuration data on card is corrupted. Download firmware to card or replace card.
39	JA1-JB1 TB IDs do no match: Check for cross-cabling	Terminal board cables are not properly connected. Check for cross-cabling.
40	VAMB A/Ds not calibrated, Run Self Test	Contact factory for instructions to run self test.
41-58	Sig x: Open Ckt Test Failed. Check Wires and Sensor.	Open circuit detected for terminal board signal Sig x, where x is the identified point. Check wiring and sensor.
61-78	Sig x: Bias Nulling Error. Check InputUse Config.	Dc bias designated for sensor type is outside of range detected for sensor. Check sensor type in configuration parameter InputUse, or check dc bias voltage on signal.
81-98	Sig x: Input Signal Saturated Check Gain Config	Peak input voltage is saturating input. Decrease configuration parameter Gain for designated signal, or check for sensor problem.
101- 118	Sig x: Sensor Limit Exceeded	Peak input voltage exceeds limit for selected sensor type. Check sensor type in configuration parameter InputUse, or check for sensor problem.

Notes

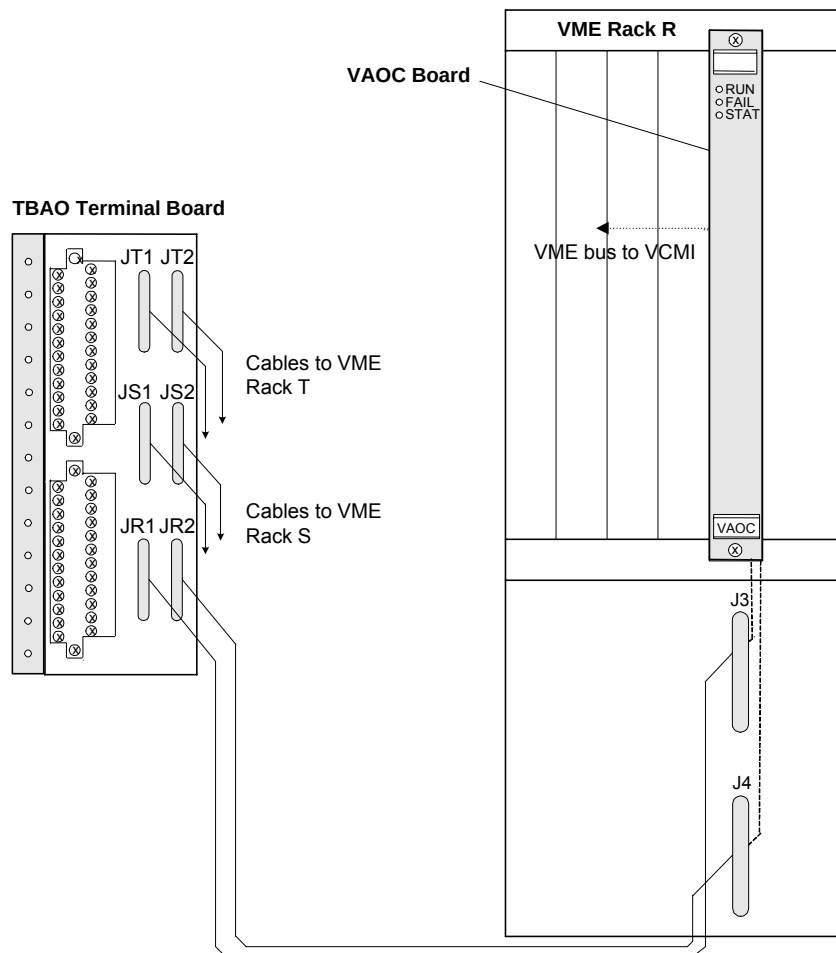
VAOC Analog Output

VAOC Analog Output

Functional Description

The Analog Output (VAOC) board controls 16 analog, 20 mA outputs. Outputs are wired to analog output terminal board(s) (TBAO or DTAO). Cables with molded plugs connect the terminal board to the VME rack where the VAOC processor board is located. VAOC receives digital values from the controller over the VME backplane from the VCMI, converts these to analog output currents, and sends them to the terminal board. The actual output current is measured on the terminal board and fed back to VAOC where it is controlled.

In triple modular redundant (TMR) applications, control signals are fanned to the same terminal board from three VME board racks R, S, and T, as shown in the following figure. Six cables are required to support all 16 outputs. Each final current output is the median selection of the three currents in the three VAOCs. This median select circuit is in each VAOC.



VAOC Board, TBAO Terminal Board, and Cabling

Compatibility

There are two generations of the VAOC board with corresponding terminal boards. The original VAOC includes all versions prior to and including VAOCH1B. When driving 20 mA outputs, these boards support up to a 500 Ω load resistance at the end of 1000 ft (304.8 m) of #18 wire. This generation requires terminal board TBAOH1B or earlier for proper operation, or any revision of DTAI.

The newest VAOC board, VAOCH1C, and any subsequent releases, support higher load resistance on the first eight output circuits. For 20 mA outputs, a drive voltage up to 18 V is available at the terminal board screw terminals. This permits operation with a 800 Ω load resistance with 1000 ft (304.8 m) of #18 wire with margin. The second set of eight output circuits retains the 500 Ω rating of the original VAOC. VAOCH1C requires TBAOH1C or later.

Installation

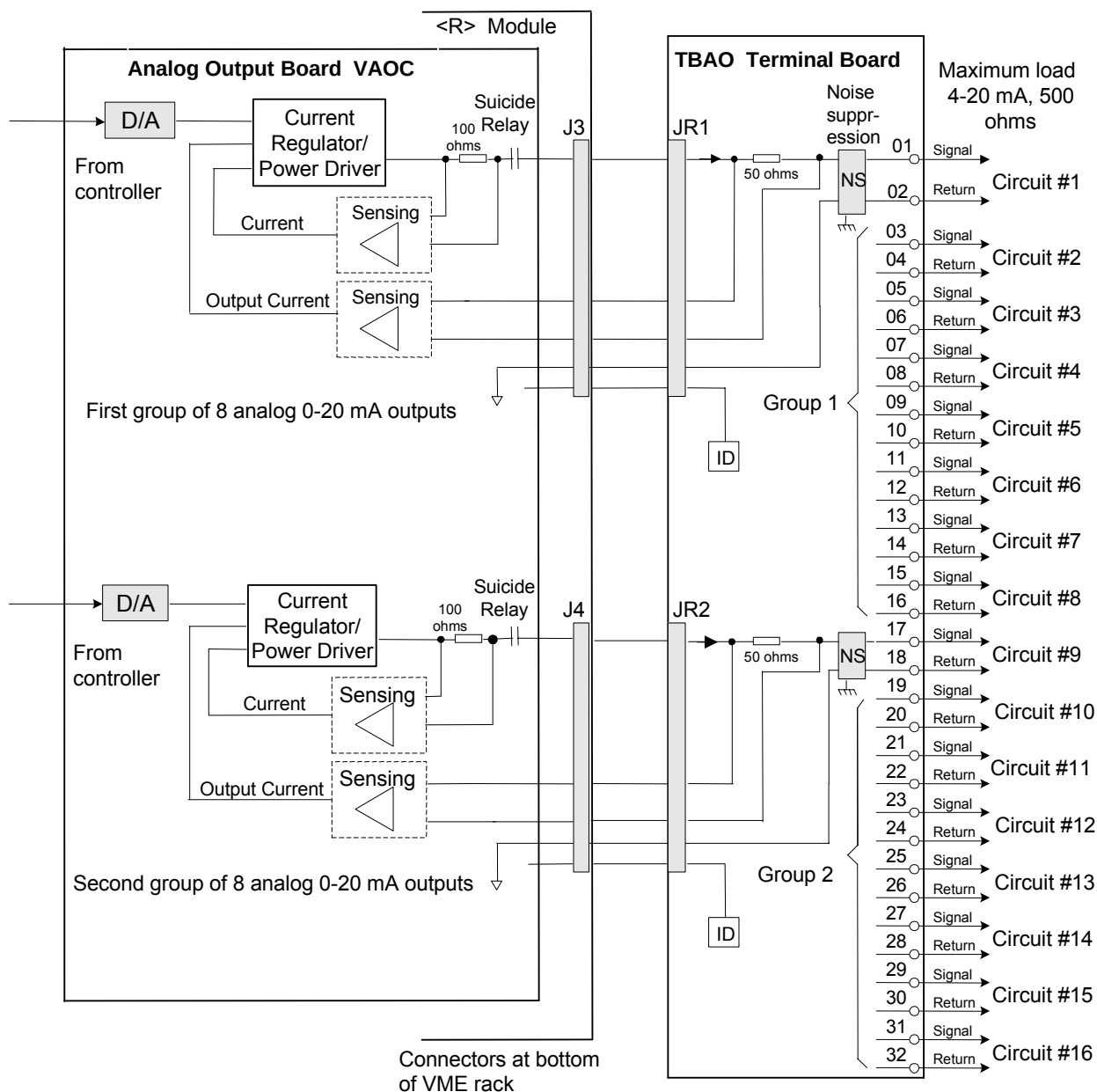
➤ To install the V-type board

- 1** Power down the VME I/O processor rack
- 2** Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3** Tighten the captive screws at the top and bottom of the front panel
- 4** Power up the VME rack and check the diagnostic lights at the top of the front panel

Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables.

Operation

VAOC supports 16 analog 0-20 mA outputs. The VAOC contains the D/A converter and driver that generates the controlled currents, as shown in the following figure. The output current is measured by the voltage drop across a resistor on the terminal board. Terminal board outputs have noise suppression circuitry to protect against surge and high frequency noise. The following figure shows VAOC circuitry in a simplex arrangement.



Analog Output Current Circuits, Simplex System

In a TMR system, each analog current output is fed by the sum of the currents from the three VAOCs. The total output current is measured with a series resistor that feeds a voltage back to each VAOC. The resulting output is the voted middle value (median) of the three currents. If one output fails, the other two pick up the current to the correct value. In the event of a circuit malfunction that cannot be cleared by a command from the processor, the circuit is disconnected by opening the shutdown relay contacts. This isolation function is only operational when configured for TMR operation.

Specifications

Item	Specification
Number of channels	16 current output channels, single ended (one side connected to common)
Analog outputs	0-20 mA, with up to 500 Ω burden Response better than 50 rad/sec
D/A converter resolution/accuracy	12 bit resolution with 0.5% accuracy
Frame rate	100 Hz on all 16 outputs
Fault detection	Output current out of limits Outer total (TMR) current D/A converter output Suicide relay operation Failed ID chip

Diagnostics

Three LEDs at the top of the I/O board front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED shows STATUS and is normally off but displays a steady orange if a diagnostic alarm condition exists in the board. The diagnostics include the following:

- Each output is monitored by diagnostics. Voltage drops across the local and outer loop current sense resistors, the D/A outputs, and at the shutdown relay contacts are sampled and digitized.
- Standard diagnostic information is available on the outputs, including high and low limit checks, and high and low system limit checks (configurable). If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG_XXXX, occurs. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O processor. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, and JT connector location. When the ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Note The following information is extracted from the toolbox and represents a sample of the configuration information for this board. Refer to the actual configuration file within the toolbox for specific information.

Parameter	Description	Choices	
VAOC Configuration			
Output Voting	Select type of output voting	Simplex, Simplex TMR	
J3:IS200TBAOH1A	Terminal board connected to VAOC through J3	Connected, not connected	
AnalogOut1	Analog output 1 board point (first set of 8 analog outputs)	Point edit (output FLOAT)	
Output_MA	Type of output current	Unused, 0-20 mA	
Low_MA	Output mA at low value	0 to 20 mA	
Low_Value	Output in engineering units at low mA	-3.4028e + 038 to 3.4028e + 038	
High_MA	Output mA at high value	0 to 20 mA	
High_Value	Output value in engineering units at high mA	-3.4028e + 038 to 3.4028e + 038	
TMR_Suicide	Enable suicide for faulty output current, TMR only	Enable, disable	
TMR_Diff Limit	Current difference in mA for suicide, TMR only	0 to 20 mA	
D/A_Err Limit	Difference between D/A reference and output, in % for suicide, TMR only	0 to 100 %	
J4:IS200TBAOH1A	Terminal board connected to VAOC though J4	Connected, not connected	
AnalogOut9	Analog output 9 - board point (second set of 8 analog outputs)	Point edit (output FLOAT)	
Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VAOC1	Board diagnostic	Input	BIT
L3DIAG_VAOC2	Board diagnostic	Input	BIT
L3DIAG_VAOC3	Status of suicide relay for output 1	Input	BIT
OutSuicide1		Input	BIT
:	:	Input	BIT
OutSuicide16	Status of suicide relay for output 16	Input	BIT
Out1MA	Measure total output current in mA	Input	Float
:	:	Input	Float
Out16MA	Measure total output current in mA	Input	Float

Alarms

Fault	Fault Description	Possible Cause
2	Flash memory CRC failure	Board firmware programming error (board will not go online)
3	CRC failure override is active	Board firmware programming error (board is allowed to go online)
16	System limit checking is disabled	System checking was disabled by configuration
17	Board ID failure	Failed ID chip on the VME I/O board
18	J3 ID failure	Failed ID chip on connector J3, or cable problem
19	J4 ID failure	Failed ID chip on connector J4, or cable problem
24	Firmware/hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: []; Tre: []The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory
31	IOCompatCode mismatch; Firmware: []; Tre: []The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory
82-97	Output [] Total current too high relative to total current. An individual current is N mA more than half the total current, where N is the configurable TMR_Diff Limit	Board failure
98-113	Output [] Total current varies from reference current. Total current is N mA different than the reference current, where N is the configurable TMR_Diff Limit	Board failure or open circuit
114-129	Output [] Reference Current Error. The difference between the output reference and the input feedback of the output reference is greater than the configured DA_Err Limit measured in percent	Board failure (D/A converter)
130-145	Output [] Individual Current Unhealthy. Simplex mode alarm indicating current is too high or too low	Board failure
146-161	Output [] Suicide Relay Non-Functional. The suicide relay is not responding to commands	Board failure (relay or driver)
162-177	Output [] Suicide Active. One output of three has suicided, the other two boards have picked up the current	Board failure

TBAO Analog Output

Functional Description

The Analog Output (TBAO) terminal board supports 16 analog outputs with a current range of 0-20 mA. Current outputs are generated by the I/O processor, which can be local (Mark* VIe control) or remote (Mark VI control). The outputs have noise suppression circuitry to protect against surge and high-frequency noise. TBAO has two barrier-type terminal blocks for customer wiring and six D-type cable connectors.

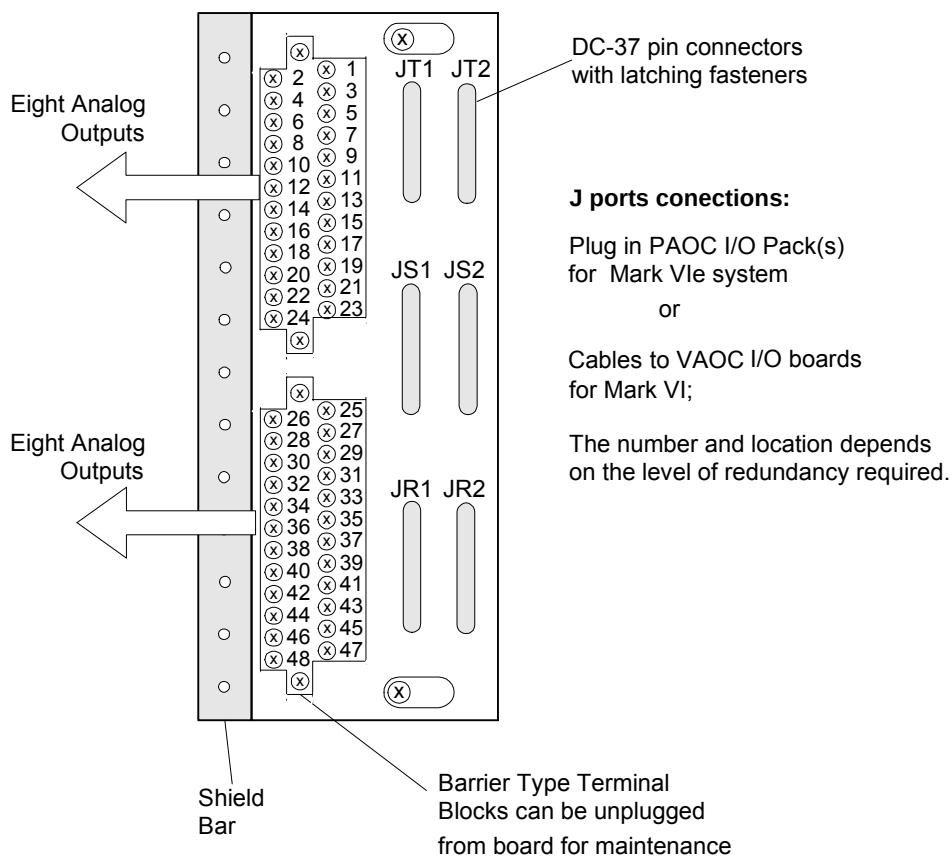
Mark VI Systems

In Mark VI systems, TBAO works with VAOC processor and supports simplex and TMR applications. Cables with molded plugs connect TBAO to the VME rack where the VAOC board is located. In TMR systems, TBAO is cabled to three VOAC boards.

Mark VIe Systems

In Mark VIe systems, TBAO works with the PAOC I/O pack and supports simplex applications only. The I/O packs plug into the D-type connectors and communicate over Ethernet with the controller.

Refer to *GEI-100577 Mark VIe Analog Input* for board compatibility.



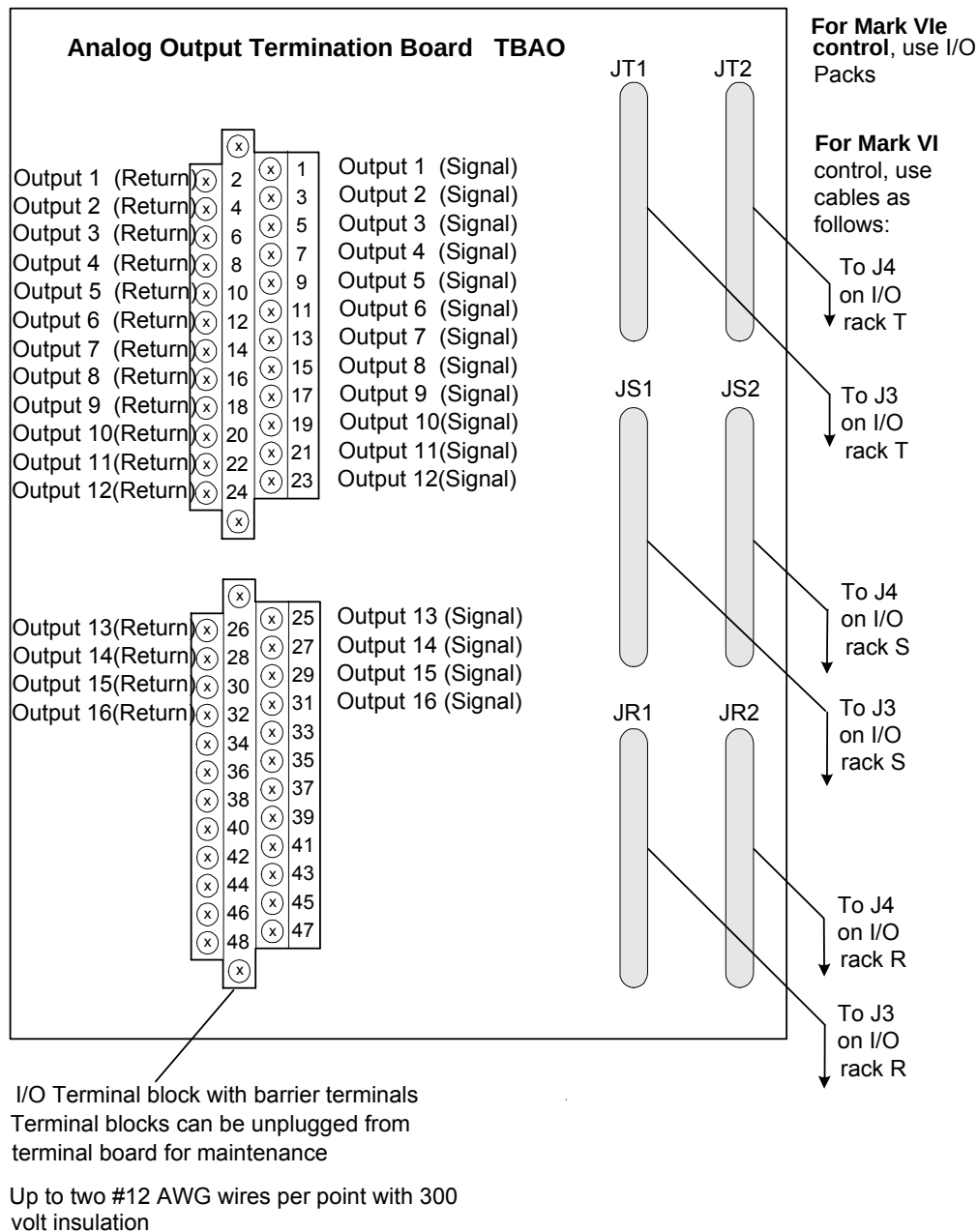
TBAO Analog Output Terminal Board

Installation

Attach TBAO to a vertical mounting plate. Connect the wires for the 16 analog outputs directly to the two I/O terminal blocks mounted on the left of the board. Each point can accept two 3.0 mm (#12AWG) wires with 300 V insulation per point using spade or ring type lugs. Each block is held down with two screws and has 24 terminals. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. Make cable connections to TBAO follows:

- In Mark VI systems, connect cables with molded plugs to the D-type connectors on the TBAO and to the VME rack where the VAOC processor is located. Use two cables for simplex or six cables for TMR.
- In Mark VIe systems, plug the PAOC I/O packs directly into selected D-type connectors. Special side mounting brackets support the packs.

The following figure shows details of TBAO wiring and cabling.

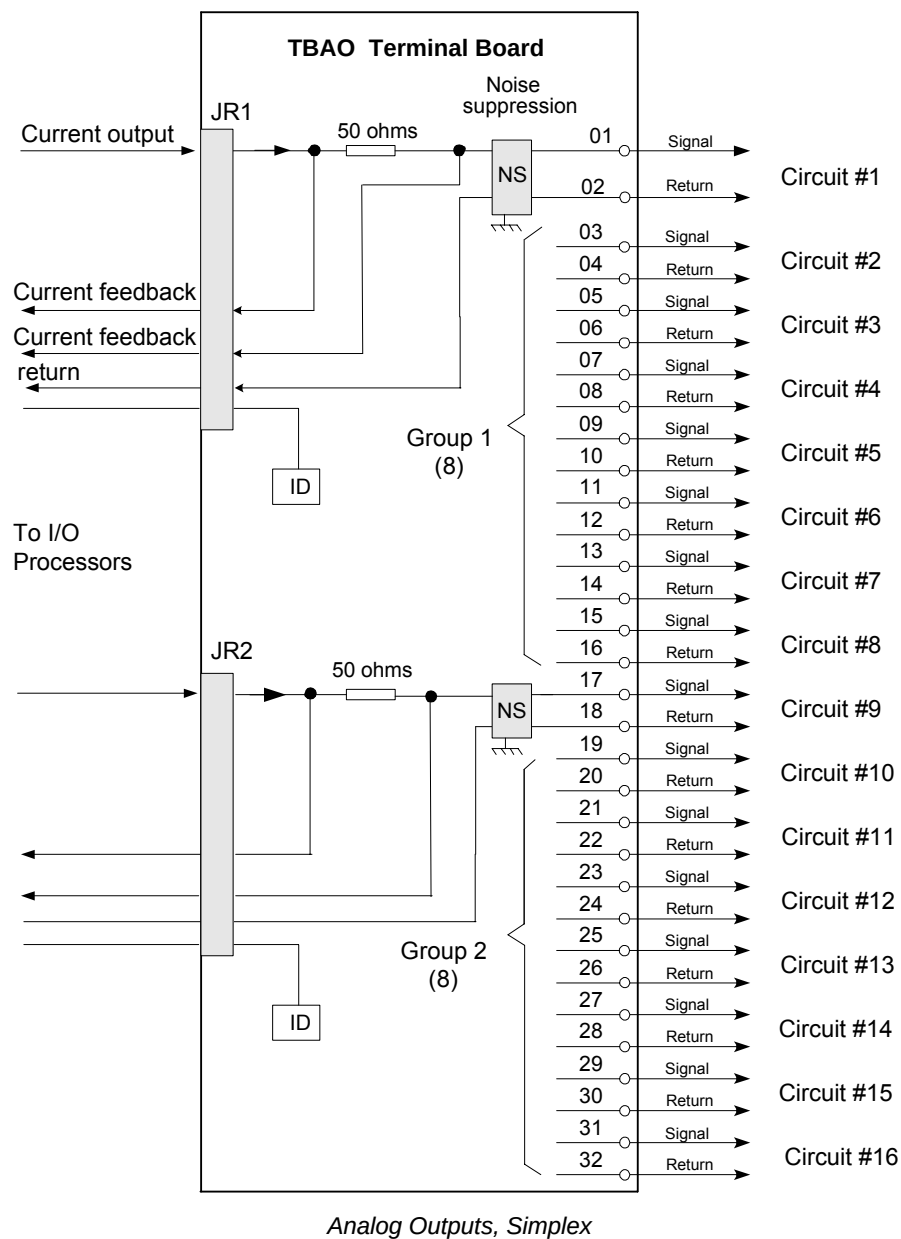


TBAO Terminal Board Wiring

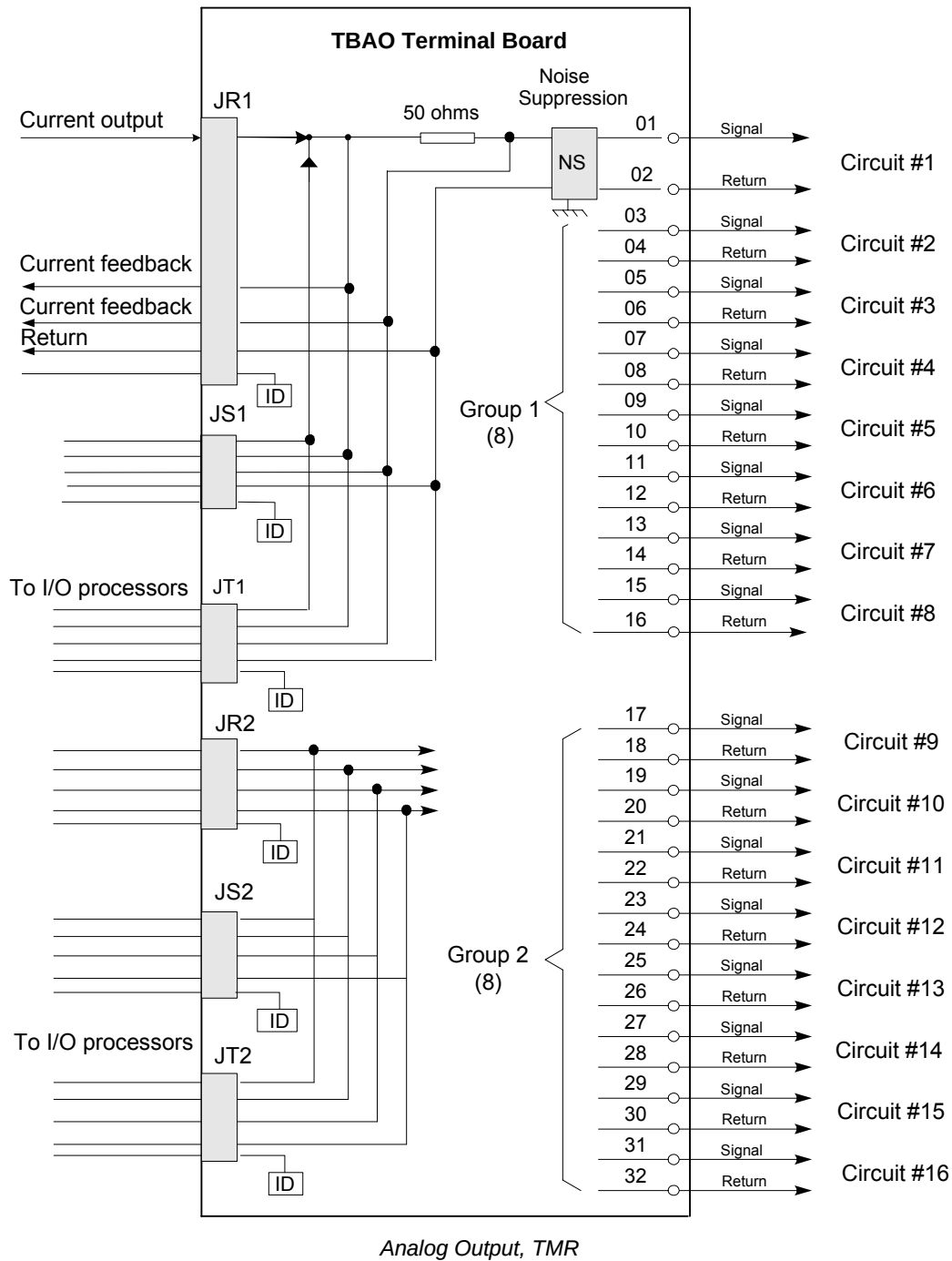
Operation

TBAO supports 16 analog control outputs. Driven devices should not exceed a resistance of 500 Ω (900 Ω if using I/O packs) and can be located up to 300 m (984 ft) from the turbine control cabinet. The VAOC or PAOC contains the D/A converter and drivers that generate the controlled currents. The output current is measured by the voltage drop across a resistor on the terminal board.

Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. The following figure shows TBAO in a simplex system.



In a TMR system, each analog current output is fed by the sum of the currents from the three I/O processors, as shown in the drawing below. The total output current is measured with a series resistor that feeds a voltage back to each I/O processor. The resulting output is the voted middle value (median) of the three currents.



Specifications

Item	Specification
Number of channels	16 current output channels, single-ended (one side connected to common)
Analog output current	0-20 mA
Customer load resistance	Up to 500 Ω burden with VOACH1B and TBAOH1B and 900 Ω burden (18 V compliance) with PAOC and TBAOH1C
Physical	
Size	10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)
Temperature	-30 to +65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

DTAO Simplex Analog Output

Functional Description

The Simplex Analog Output (DTAO) terminal board is a compact analog output terminal board designed for DIN-rail mounting. DTAO has eight analog outputs driven by the VAOC I/O board over a single cable. This board is designed for simplex-only applications and only works with the VAOC. A single cable with 37-pin D-type connector connects DTAO to the VAOC rack. This cable is identical to those used on the larger TBAO terminal board. Two DTAO boards can be connected to the VAOC for a total of 16 analog outputs.

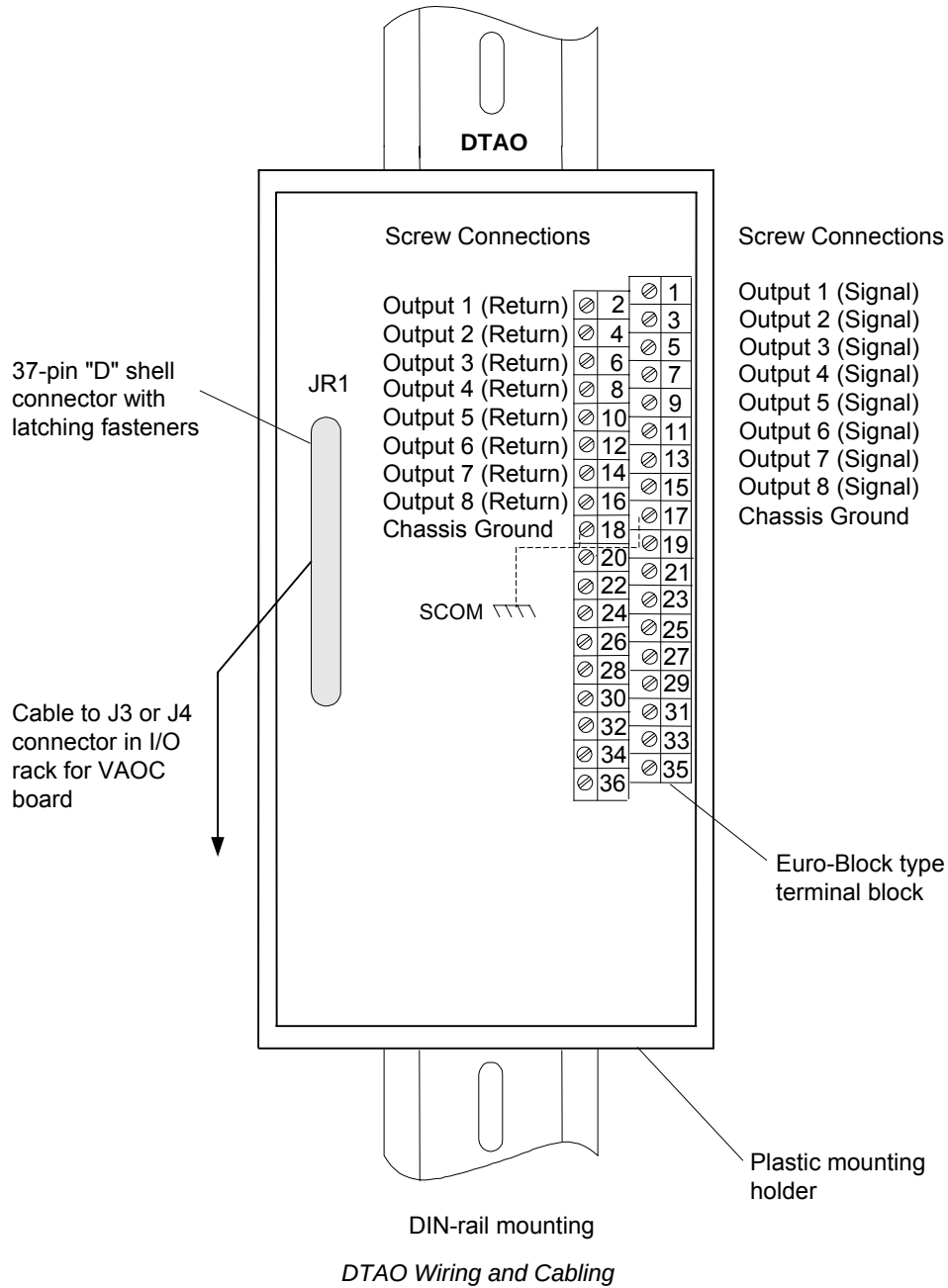
Note The DTAO board does not work with the PAOC I/O pack.

The on-board circuits and noise suppression are the same as those on TBAO. High-density Euro-block type terminal blocks are permanently mounted to the board, with two screw connections for the ground connection (SCOM). An on-board ID chip identifies the board to the VAOC for system diagnostic purposes.

Installation

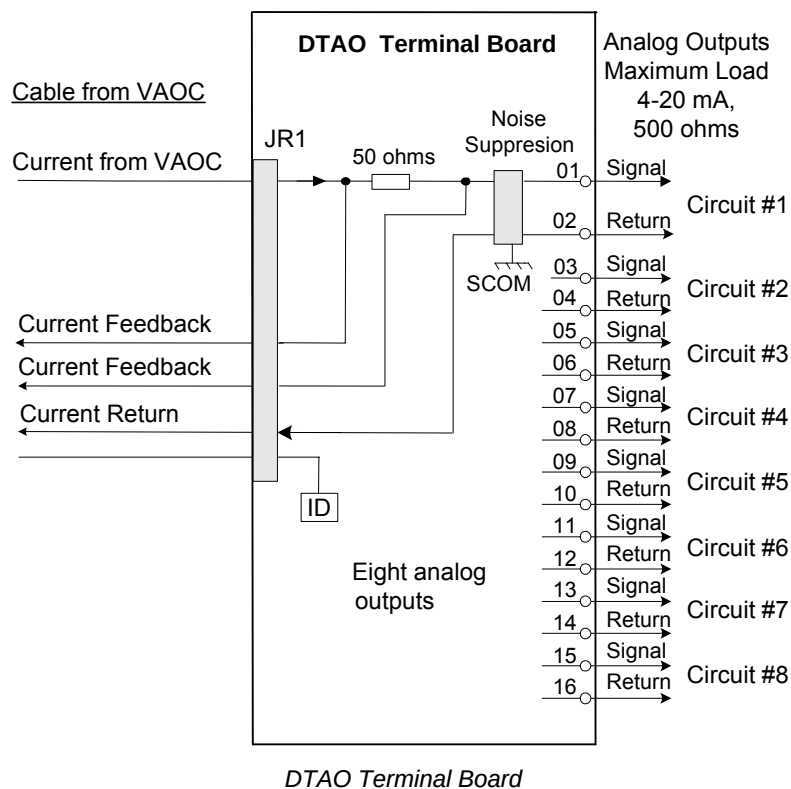
Mount the plastic holder on the DIN-rail and slide the DTAO board into place. Connect the wires for the eight analog outputs directly to the terminal block as shown in the following figure. Driven devices should not exceed a resistance of 500 Ω and can be located up to 300 m (984 ft) from the turbine control cabinet. The Euro-block type terminal block has 36 terminals and is permanently mounted on the terminal board. Typically #18 AWG wires (shielded twisted pair) are used. Two screws, 17 and 18, are provided for the SCOM (ground) connection, which should be as short a distance as possible. DIN-type terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space.

Note There is no shield terminal strip on DTAO.



Operation

DTAO supports eight analog control outputs. On each output the voltage drop across the local loop current sense resistor is measured and the signal is fed back to the VAOC processor, which controls the current. Filters reduce high-frequency noise and suppress surge on each output near the point of signal exit. VAOC contains the D/A converter and drivers that generate the controlled currents.



Specifications

Item	Specification
Number of channels	8 current output channels, single ended (one side connected to common)
Analog output current	0-20 mA
Customer load resistance	Up to 500 Ω burden
Physical	
Size	8.6 cm wide x 16.2 cm high (3.4 in x 6.37 in)
Temperature	0 to 60°C (32 to 149 °F)

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- The board provides the voltage drop across a series resistor to indicate the output current. The I/O processor creates a diagnostic alarm (fault) if any one of the two outputs goes unhealthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, JT connector location. When this chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

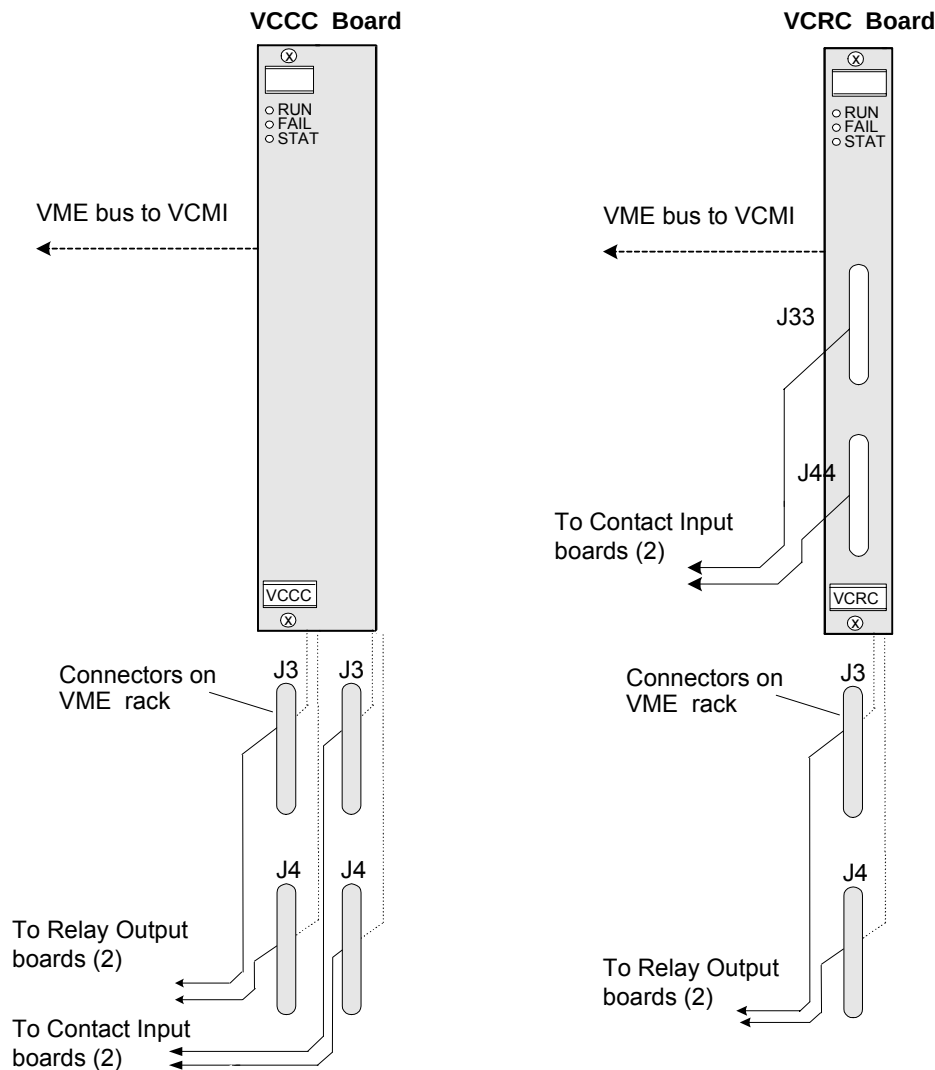
VCCC/VCRC Discrete Input/Output

VCCC/VCRC Discrete Input/Output

Functional Description

Note VCRC is a single slot version of VCCC with the same functionality, but contact input cables plug into the front of the board.

The Discrete Input/Output (VCCC) board with its associated daughterboard accepts 48 discrete inputs and controls 24 relay outputs from four terminal boards. VCCC is a double width module and mounts in the VME I/O rack. This rack has two sets of J3/J4 plugs for cables to the TBCI and TRLY terminal boards. VCRC is a narrower, single slot board and can be used instead of the VCCC.



VCCC and VCRC Boards and Cable Connections

VCRC Option

The VCRC board has the same functionality as the VCCC board but takes up only one VME slot because no daughter board is required. Two front panel connectors, J33 and J44, accept the contact inputs from the TBCI terminal boards. Relay outputs on TRL Y use the J3 and J4 ports on the VME rack, the same as for VCCC. If locating cables on the front panel is undesirable, VCCC can be used instead.

Note VCRC does not support the TICI contact voltage sensing board.

Installation

➤ To install the V-type board

- 1** Power down the VME I/O processor rack
- 2** Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3** Tighten the captive screws at the top and bottom of the front panel
- 4** Power up the VME rack and check the diagnostic lights at the top of the front panel

Cable connections to the terminal boards are made at the J3 and J4 connectors (right hand set) on the lower portion of the VME rack. These are latching type connectors to secure the cables. Cable connections to the TRL Y terminal boards are made to the left hand set of J3 and J4 connectors.

Note With the VCRC, both TBCI cables connect to J33 and J44 on the front panel, not to connectors under the rack.

Operation

VCCC passes the input voltages through optical isolators and samples the signals at the frame rate for control functions, and at 1 ms for sequence of events (SOE) reporting. VCCC transfers the signals over the VME backplane to the VCMI, which sends them to the controller. The contact input processing is shown in the figure, *VCCC and I/O Terminal Boards, Simplex System*.

Contact Inputs

The first 24 dry contact inputs are wired to a contact input terminal board. A second terminal board is required for inputs 25 - 48. Dc power is provided for the contacts. Cables with molded plugs connect the terminal board to the VME rack where the VCCC processor board is located.

High speed scanning and recording at 1 ms rate is available for inputs monitoring important turbine variables. The SOE recorder reports all contact openings and closures with a time resolution of 1 ms. Contact chatter and pulse widths down to 6 ms are reported.

The dry-contact inputs are powered from a floating 125 V dc (100 - 145 V dc) supply (TBCIH1) or from a floating 24 V dc (18.5 - 32 V dc) supply (TBCIH2). Filters reduce high frequency noise and suppress surge on each input near the point of signal exit. Noise and contact bounce is filtered with a 4 ms filter. Ac voltage rejection (50/60 Hz) is 60 V rms with 125 V dc excitation.

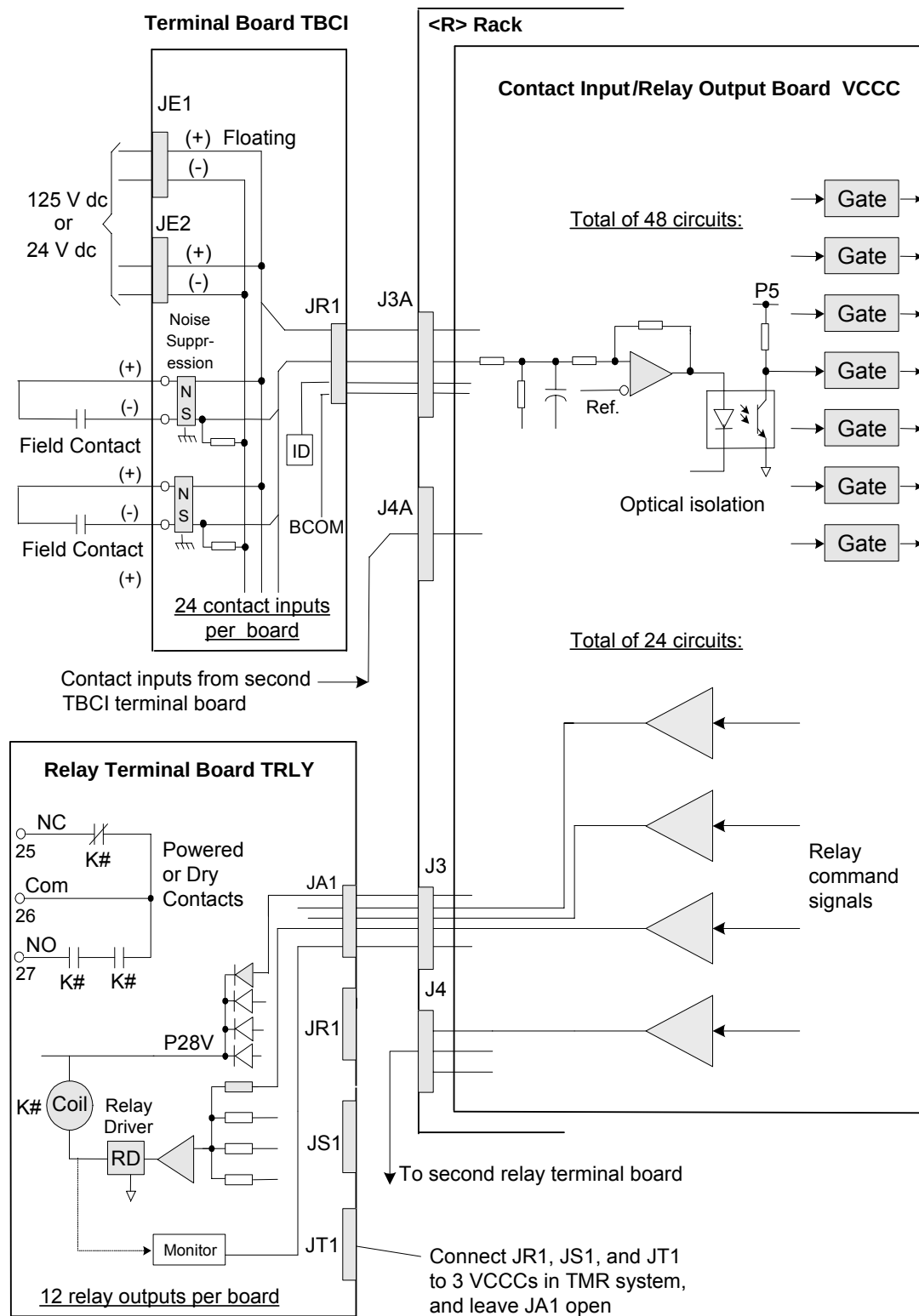
For triple modular redundant (TMR) applications, contact input voltages are fanned out to three VME board racks R, S, and T through plugs JR1, JS1, and JT1. The signals are processed by the three VCCCs and the results voted by the VCMI board in each controller rack.

Relay Outputs

TRL YH1B holds 12 plug-in magnetic relays. The first six relay circuits can be jumpers configured for either dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115 V ac source, or an optional 24 V dc source, with individual jumper selectable fuses and on-board suppression can be provided for field solenoid power. The next five relays (7-11) are un-powered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications such as ignition transformers.

Cables carry relay control signals and monitor feedback voltages between VCCC and TRL Y. Relay drivers, fuses, and jumpers are mounted on the relay board. Several types of relay boards can be driven, including TRL Y, DRL Y, and SRL Y.

The relay outputs have failsafe features so that when a cable is unplugged, the inputs vote to de-energize the corresponding relays. Similarly, if communication with the associated VME board is lost, the relays de-energize.



VCCC and I/O Terminal Boards, Simplex System

Specifications

Item	Specification
Number of channels	48 dry contact voltage input channels (24 per terminal board) 24 relay output channels (12 relays per terminal board)
Input contact excitation voltage	H1 – nominal 125 V dc, floating, ranging from 100 to 145 V dc H2 – nominal 24 V dc, floating, ranging from 18.5 to 32 V dc
Input isolation	Optical isolation to 1500 V on all inputs
Input filter	Hardware filter, 4 ms
Ac voltage rejection	60 V rms @ 50/60 Hz at 125 V dc excitation
Input frame rate	System dependent scan rate for control purposes 1,000 Hz scan rate for SOE monitoring
Rated voltage on relays	a: Nominal 125 V dc or 24 V dc b: Nominal 120 V ac or 240 V ac
Max relay load current	a: 0.6 A for 125 V dc operation b: 3.0 A for 24 V dc operation c: 3.0 A for 120/240 V ac, 50/60 Hz operation
Max response time on	25 ms
Max response time off	25 ms
Relay contact material	Silver cad-oxide
Relay contact life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault detection	Loss of contact input excitation voltage Non-responding contact input in test mode Loss of user solenoid power (blown fuse) Coil current disagreement with command Relay contact voltage monitoring indicates problem Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost Failed ID chip
Physical	
Size - VCRC	26.04 cm high x 1.99 cm wide x 18.73 cm deep (10.25 in x 0.782 in x 7.375 in)
Size - VCCC	26.04 cm high x 3.98 cm wide x 18.73 cm deep (10.25 in x 1.564 in x 7.375 in)
Temperature	0 to 60°C (32 to 140 °F)

Diagnostics

Three LEDs at the top of the I/O board front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED shows STATUS and is normally off but displays a steady orange if a diagnostic alarm condition exists in the board. The diagnostics include the following:

- Each output is monitored by diagnostics. Voltage drops across the local and outer loop current sense resistors, the D/A outputs, and at the shutdown relay contacts are sampled and digitized.
- Standard diagnostic information is available on the outputs, including high and low limit checks, and high and low system limit checks (configurable). If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG_xxxx, occurs. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O processor. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the JR, JS, and JT connector location. When the ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Note The following information is extracted from the toolbox and represents a sample of the configuration information for this board. Refer to the actual configuration file within the toolbox for specific information.

Parameter	Description	Choices
Configuration		
System Limits	Enable all system limit checking	Enable, disable
J3:IC200TRLYH1B	Terminal board 1 connected to VCCC through J3	Connected, not connected
Relay01	First relay output (from first set of 12 relays) - card point	Point edit (Output BIT)
Relay Output	Select relay output	Used, unused
FuseDiag	Enable fuse diagnostic	Enable, disable
Relay01Fdbk	Relay 01 contact voltage (first set of 12 relays) - card point	Point edit (Input BIT)
ContactInput	Configurable Item:slot#	Used, unused
SignalInvert	Inversion makes signal true if contact is open	Normal, invert
SignalFilter	Contact Input filter in msec	0, 10, 20, 50
J4:IC200TRLYH1B	Terminal board 2 connected to VCCC through J4	Connected, not connected
Relay01	Relay output 1 (second set of 12 relays) - card point	Point edit (Output BIT)
Relay01Fdbk	Relay 1 contact voltage (second set of 12 relays) - card point	Point edit (Input BIT)
J3A:IS200TBCIH1A	Terminal board connected to VCCC from J3	Connected, not connected
Contact01	First contact of 24 on first terminal board - board point	Point edit (input BIT)
Contact input	Select contact input	Used, unused
Signal invert	Inversion makes signal true if contact open	Normal, invert
Sequence of events	Select input for sequence of events scanning	Enable, disable
Signal filter	Contact input filter in milliseconds	0, 10, 20, 50
J4A:IS200TBCIH1A	Terminal board connected to VCCC from J4	Connected, not connected

Parameter	Description	Choices	
Contact01	First contact of 24 on second terminal board - board point	Point edit	(input BIT)

Board point Signals	Description-Enter Signal Connection Name	Direction	Type
L3DIAG_VCCC1	Board diagnostic	Input	BIT
L3DIAG_VCCC2	Board diagnostic	Input	BIT
L3DIAG_VCCC3	Board diagnostic	Input	BIT

Alarms

Fault	Fault Description	Possible Cause
1	SOE Overrun. Sequence of events data overrun	Communication problem on IONet
2	Flash memory CRC failure	Board firmware programming error (board will not go online)
3	CRC failure override is active	Board firmware programming error (board is allowed to go online)
16	System limit checking is disabled. System limit checking has been disabled	System checking was disabled by configuration
17	Board ID failure	Failed ID chip on the VME I/O board
18	J3 ID failure	Failed ID chip on connector J3, or cable problem
19	J4 ID failure	Failed ID chip on connector J4, or cable problem
22	J33/J3A ID failure	Failed ID chip on connector J33 or J3A, or cable problem
23	J44/J4A ID failure	Failed ID chip on connector J44 or J4A, or cable problem
24	Firmware/hardware incompatibility. The firmware on this board cannot handle the terminal board it is connected to	Invalid terminal board connected to VME I/O board. Check the connections and call the factory.
30	ConfigCompatCode mismatch; Firmware: [] ; Tre: [] The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: []; Tre: [] The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
33-56/ 65-88	TBCI J33/J3A/J44/J4A contact input [] not responding to Test Mode. A single contact or group of contacts could not be forced high or low during VCCC self-check	Normally a VCCC problem, or the battery reference voltage is missing to the TBCI terminal board, or a bad cable.
129-140/ 145-156	TRLY J3/J4 relay output coil [] does not match requested state. A relay coil monitor shows that current is flowing or not flowing in the relay coil, so the relay is not responding to VCCC commands	The relay terminal board may not exist, or there may be a problem with this relay, or, if TMR, one VCCC may have been out-voted by the other two VCCC boards.
161-172/ 177-188	TRLY J3/J4 relay driver [] does not match requested state. The relay is not responding to VCCC commands	The relay terminal board may not exist and the relay is still configured as used, or there may be a problem with this relay driver.
97-102/ 113-118	TRLY J3/J4 fuse [] blown. The fuse monitor requires the jumpers to be set and to drive a load, or it will not respond correctly	The relay terminal board may not exist, or the jumpers are not set and there is no load, or the fuse is blown.
240/241	TBCI J3/J4 excitation voltage not valid, TBCI J33/J3A/J44/J4A contact inputs not valid. The VCCC monitors the excitation on all TBCI and DTCL boards, and the contact input requires this voltage to operate properly	The contact input terminal board may not exist, or the contact excitation may not be on, or be unplugged, or the excitation may be below the 125 V level.
256-415	Logic signal voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TBCI Contact Input with Group Isolation

Functional Description

The Contact Input with Group Isolation (TBCI) terminal board accepts 24 dry contact inputs wired to two barrier-type terminal blocks. Dc power is wired to TBCI for contact excitation. The contact inputs have noise suppression circuitry to protect against surge and high-frequency noise.

Mark VI Systems

In the Mark* VI system, TBCI works with VTCC/VCRC and supports simplex and TMR applications. Cables with molded plugs connect TBCI to VME rack where the VCCC or VCRC processor board is located. Both board versions TBCIH_B and TBCIH_C work correctly with Mark VI and are functionally identical.

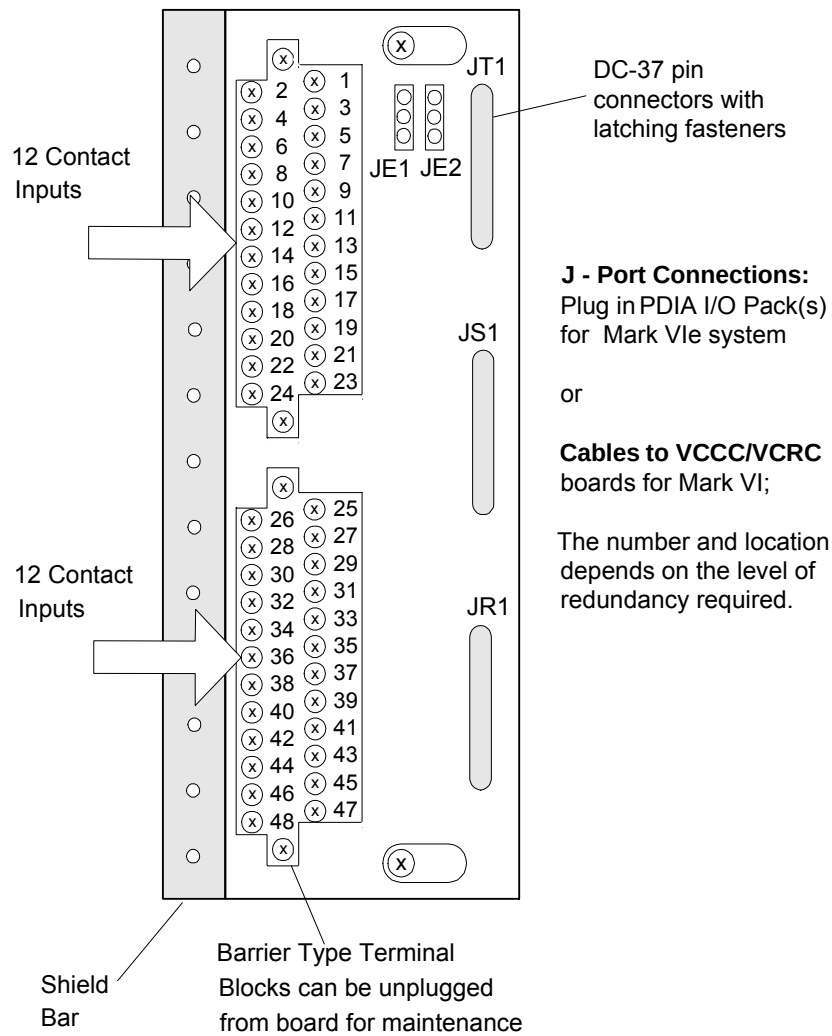
Mark VIe Systems

In the Mark VIe system, the TBCI works with the PDIA I/O pack and supports simplex, dual, and TMR applications. One, two, or three PDIA's can be plugged directly into the TBCI. Mark VIe requires the C version of this board for correct mechanical alignment of connector JT1 with I/O pack mechanical support.

Board Versions

Three versions of TBCI are available as follows:

Terminal Board	Contact Inputs	Excitation Voltage
TBCIH1C	24	Nominal 125 V dc, floating, ranging from 100 to 145 V dc
TBCIH2C	24	Nominal 24 V dc, floating, ranging from 16 to 32 V dc
TBCIH3C	24	Nominal 48 V dc, floating, ranging from 32 to 64 V dc



TBCI Contact Input Terminal Board

Installation

Wiring

Connect the wires for the 24 dry contact inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

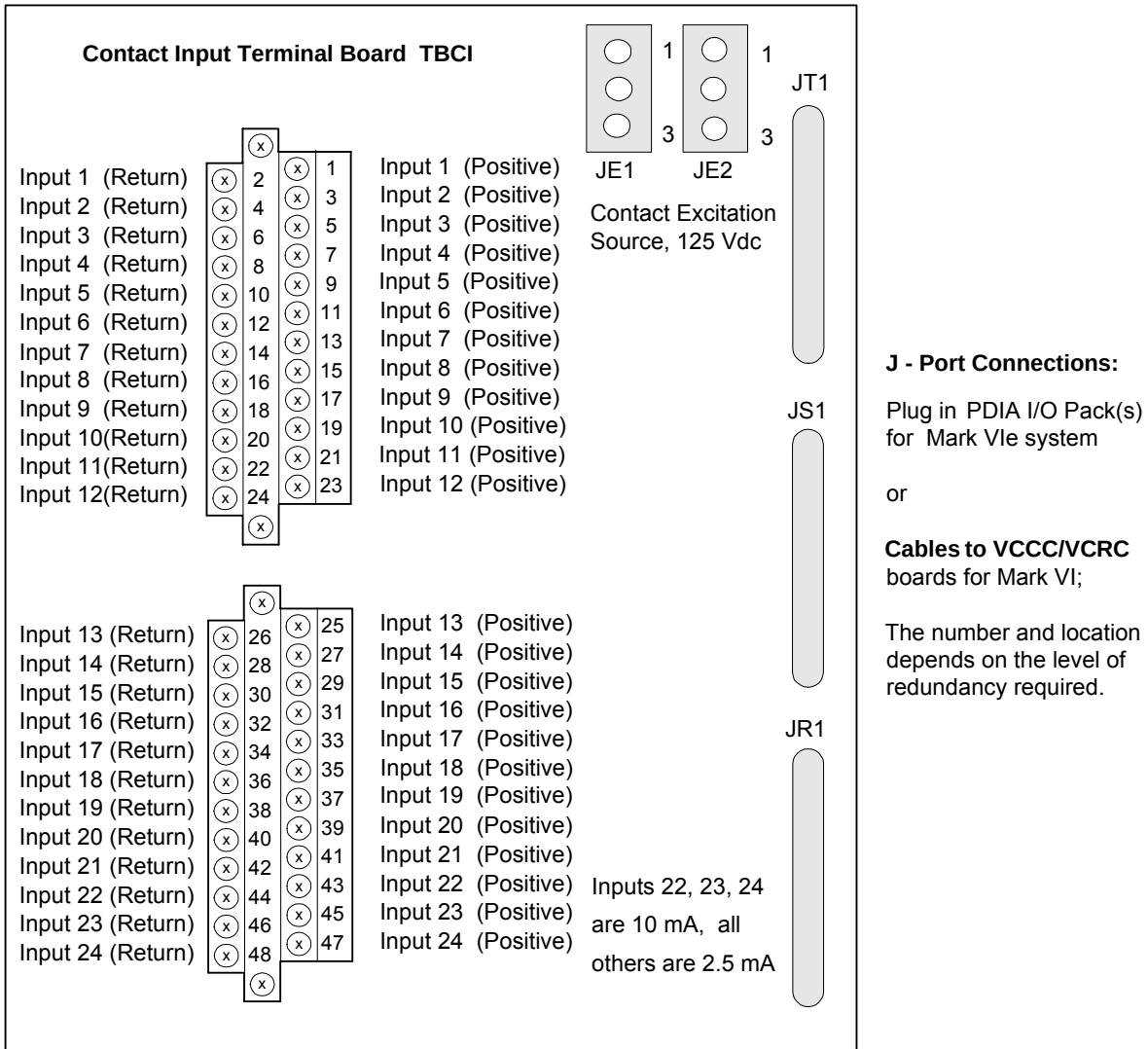
Power Connection

Connect TBCI to the contact excitation voltage source using plugs JE1 and JE2, as shown in following figure.

Cabling Connections

In a simplex system, connect TBCI to the I/O processor using connector JR1. In a TMR system, connect TBCI to the I/O processors using connectors JR1, JS1, and JT1. Cables or I/O packs are plugged in depending on the type of Mark VI or Mark VIe system, and the level of redundancy.

Note For a Mark VIe system, the I/O packs plug into TBCI and attach to side-mounting brackets. One or two Ethernet cables plug into the pack. Firmware may need to be downloaded. Refer to *GEH-6700, ToolboxST for Mark VIe Control*.



Terminal Blocks can be unplugged from terminal board for maintenance

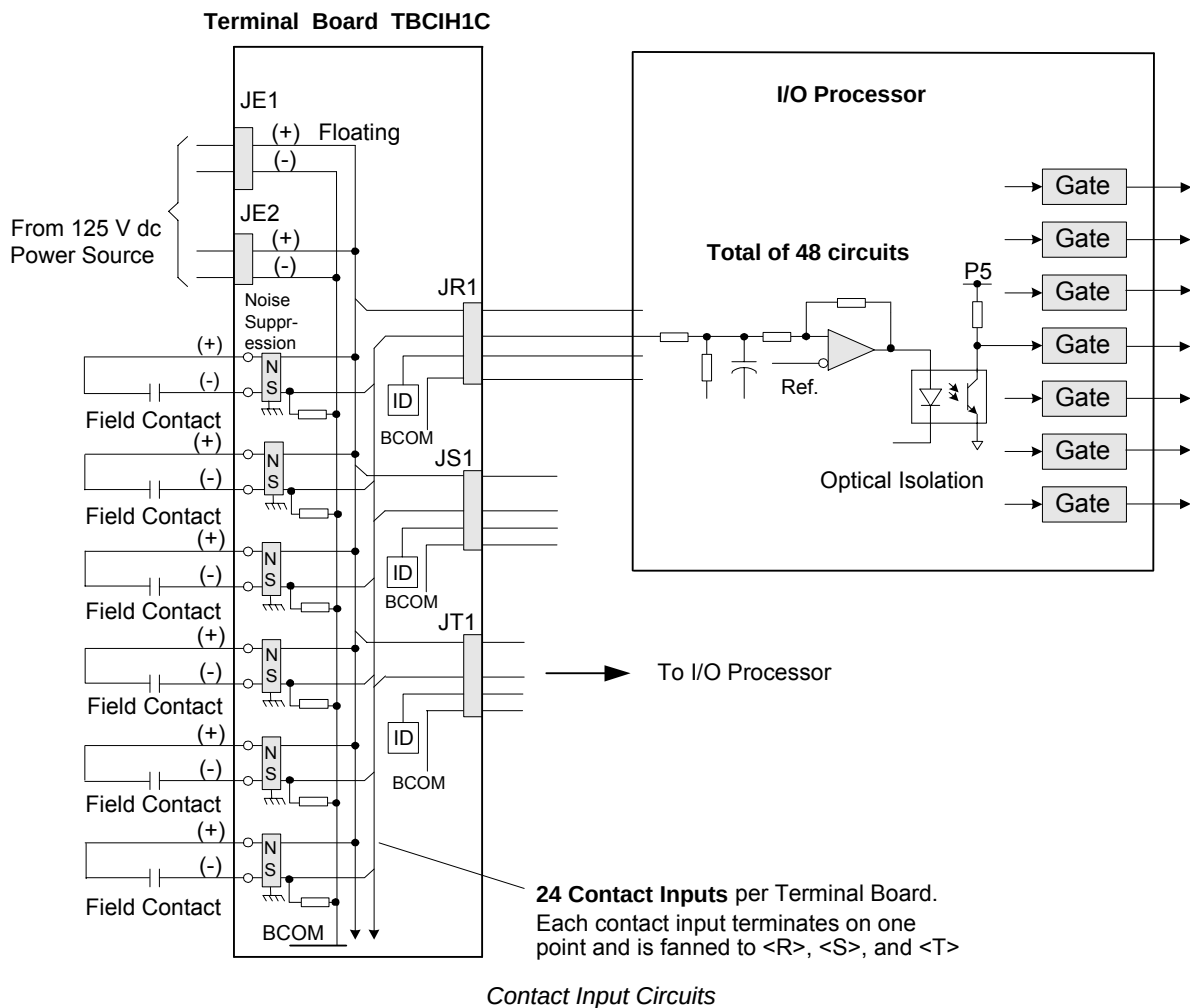
Up to two #12 AWG wires per point with 300 volt insulation

TBCI1C Terminal Board Wiring and Cabling

Operation

Filters reduce high-frequency noise and suppress surge on each input near the point of signal entry. The dry contact inputs on H1 are powered from a floating 125 V dc (100-145 V dc) supply from the turbine control. The 125 V dc bus is current limited in the power distribution module prior to feeding each contact input. H2 and H3 versions use lower voltages as shown in the specification table.

The discrete input voltage signals pass to the I/O processor, which sends them through optical isolators providing group isolation and transfers the signals to the system controller. The reference voltage in the isolation circuits sets a transition threshold that is equal to 50% of the applied floating power supply voltage. The tracking is clamped to go no less than 13% of the nominal rated supply voltage to force all contacts to indicate open when voltage dips below this level.



A pair of terminal points is provided for each input, with one point (screw) providing the positive dc source and the second point providing the return (input) to the board. The current loading is 2.5 mA per point for the first 21 inputs on each terminal board. The last three have a 10 mA load to support interface with remote solid-state output electronics. Contact input circuitry is designed for NEMA Class G creepage and clearance.

Specifications

Item	Specification
Number of channels	24 contact voltage input channels
Excitation voltage	H1: Nominal 125 V dc, floating, ranging from 100 to 145 V dc H2: Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc H3: Nominal 48 V dc, floating, ranging from 32 to 64 V dc
Input current	H1: For 125 V dc applications: First 21 circuits draw 2.5 mA (50 k Ω) Last three circuits draw 10 mA (12.5 k Ω) H2: For 24 V dc applications: First 21 circuits draw 2.5 mA (10 k Ω) Last three circuits draw 9.9 mA (2.42 k Ω) H3: For 48 V dc applications: First 21 circuits draw 2.5 mA Last three circuits draw 10 mA
Input filter	Hardware filter, 4 ms
Power consumption	20.6 W on the terminal board
Temperature rating	0 to 60°C (32 to 140 °F)
Fault detection	Loss of contact input excitation voltage Non-responding contact input in test mode Unplugged cable
Physical	
Size	33.02 cm high x 10.16 cm wide (13.0 in. x 4.0 in)
Temperature	Operating: -30 to 65°C (-22 to 149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack/board.
- As a test, all inputs associated with this terminal board are forced to the open contact (fail safe) state. Any input that fails the diagnostic test is forced to the failsafe state and a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

TICI Contact Input with Point Isolation

Functional Description

The Contact Input with Point Isolation (TICI) terminal board provides 24 point isolated voltage detection circuits to sense a range of voltages across relay contacts, fuses, and switches.

Mark VI Systems

In the Mark* VI system, the TICI is controlled by the VCCC board and supports simplex and TMR applications. Cables with molded plugs connect TICI to the VME rack where the I/O boards are mounted.

Note The VCRC J3 and J4 front connectors do not support TICI.

Mark VIe Systems

In the Mark VIe system, the TICI works with the PDIA I/O pack and supports simplex, dual, and TMR applications. One, two, or three PDIA's plug into the TICI to support a variety of system configurations.

Installation

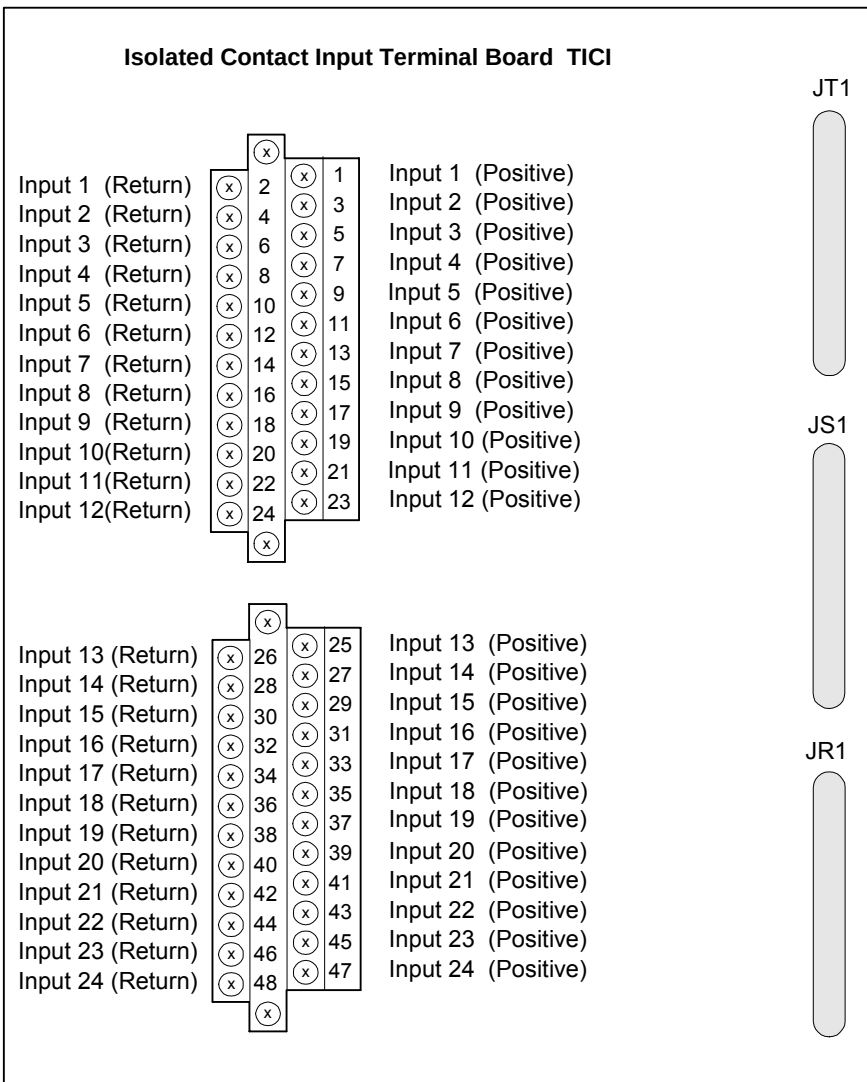
Wiring

Connect the wires for the 24 isolated digital inputs directly to two I/O terminal blocks on the terminal board. These blocks are held down with two screws and can be unplugged from the board for maintenance. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Cabling Connections

In a simplex system, connect TICI to the I/O processor using connector JR1. In a TMR system, connect TICI to the I/O processors using connectors JR1, JS1, and JT1. Cables or I/O packs are plugged in depending on the type of Mark VI or Mark VIe system, and the level of redundancy.

Note For a Mark VIe system, the I/O packs plug into TICI and attach to side-mounting brackets. One or two Ethernet cables plug into the pack. Firmware may need to be downloaded.



J - Port Connections:

Plug in PDIA I/O Pack(s)
for Mark VIe system

or

Cables to VCCC boards
for Mark VI;

The number and location
depends on the level of
redundancy required.

Terminal Blocks can be unplugged
from terminal board for maintenance

Up to two #12 AWG wires per
point with 300 volt insulation

TICI Terminal Board Wiring and Cabling

Operation

The TICI is similar to TBCI, except for the following items:

- No contact excitation is provided on the terminal board.
- Each input is electrically isolated from all others and from the active electronics.

There are two groups of the TICI with different nominal voltage thresholds. TICIH1 has the following input voltage ranges:

- 70-145 V dc, nominal 125 V dc, with a detection of 39 to 61 V dc
- 200-250 V dc, nominal 250 V dc, with a detection of 39 to 61 V dc
- 90-132 V rms, nominal 115 V rms, 47-63 Hz, with a detection of 35 to 76 V ac
- 190-264 V rms, nominal 230 V rms, 47-63 Hz, with a detection of 35 to 76 V ac

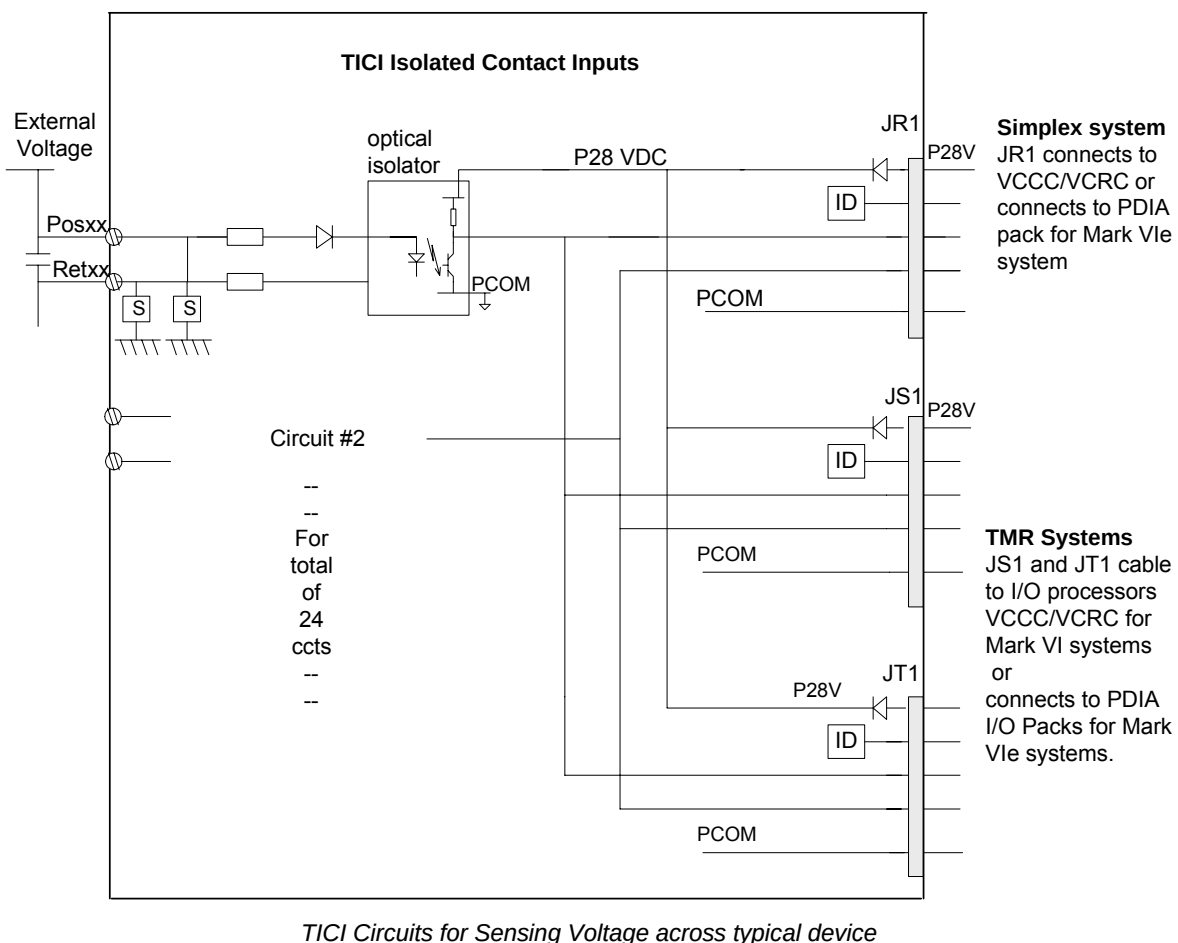
TICIH2 has the following input voltage range:

- 16-32 V dc, nominal 24 V dc, with a detection threshold of 9.5 to 15 V dc

TICI provides input hardware filtering with time delays of 15 ms, nominal:

- For dc applications the time delay is 15 $\pm$ 8 ms
- For ac applications the time delay is 15 $\pm$ 13 ms

In addition to hardware filters, the contact input state is software-filtered, using configurable time delays selected from 0, 10, 20, 50, and 100 ms. For ac inputs, a filter of at least 10 ms is recommended.



The following restrictions should be noted regarding creepage and clearance on the 230 V rms application:

- For NEMA requirements: 230 V single-phase
- For CE Certification: 230 V single or 3-phase

Refer to VCCC or PDIO documentation for information on monitoring contact inputs.

Specifications

Item	Specification
Number of channels	24 input channels for isolated voltage sensing
Input voltage	TICIH2: 16-32 V dc, nominal 24 V dc, with a detection threshold of 9.5 to 15 V dc TICIH1: 70 -145 V dc, nominal 125 V dc, with a detection threshold of 39 to 61 V dc 200 -250 V dc, nominal 250 V dc, with a detection threshold of 39 to 61 V dc 90 -132 V rms, nominal 115 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac 190-264 V rms, nominal 230 V rms, 47-63 Hz, with a detection threshold of 35 to 76 V ac
Fault detection in I/O board	Non-responding contact input in test mode Unplugged cable or failed ID chip
Physical	
Size	17.8 cm high x 33.02 cm wide (7.0 in. x 13.0 in.)
Temperature	Operating -30 to +65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack/board.
- As a test, all inputs associated with this terminal board are forced to the open contact (fail safe) state. Any input that fails the diagnostic test is forced to the failsafe state and a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

DTCI Simplex Contact Input with Group Isolation

Functional Description

The Simplex Contact Input with Group Isolation (DTCI) terminal board is a compact terminal board designed for DIN-rail mounting. The DTCI board has 24 contact inputs with a nominal excitation of 24 V dc, and connects to the VCCC (or VCRC) processor board with a single cable. Two DTCI boards can be connected to the VCCC or VCRC for a total of 48 contact inputs. The terminal boards can be stacked vertically on a DIN-rail to conserve cabinet space. Only a simplex version of this board is available.

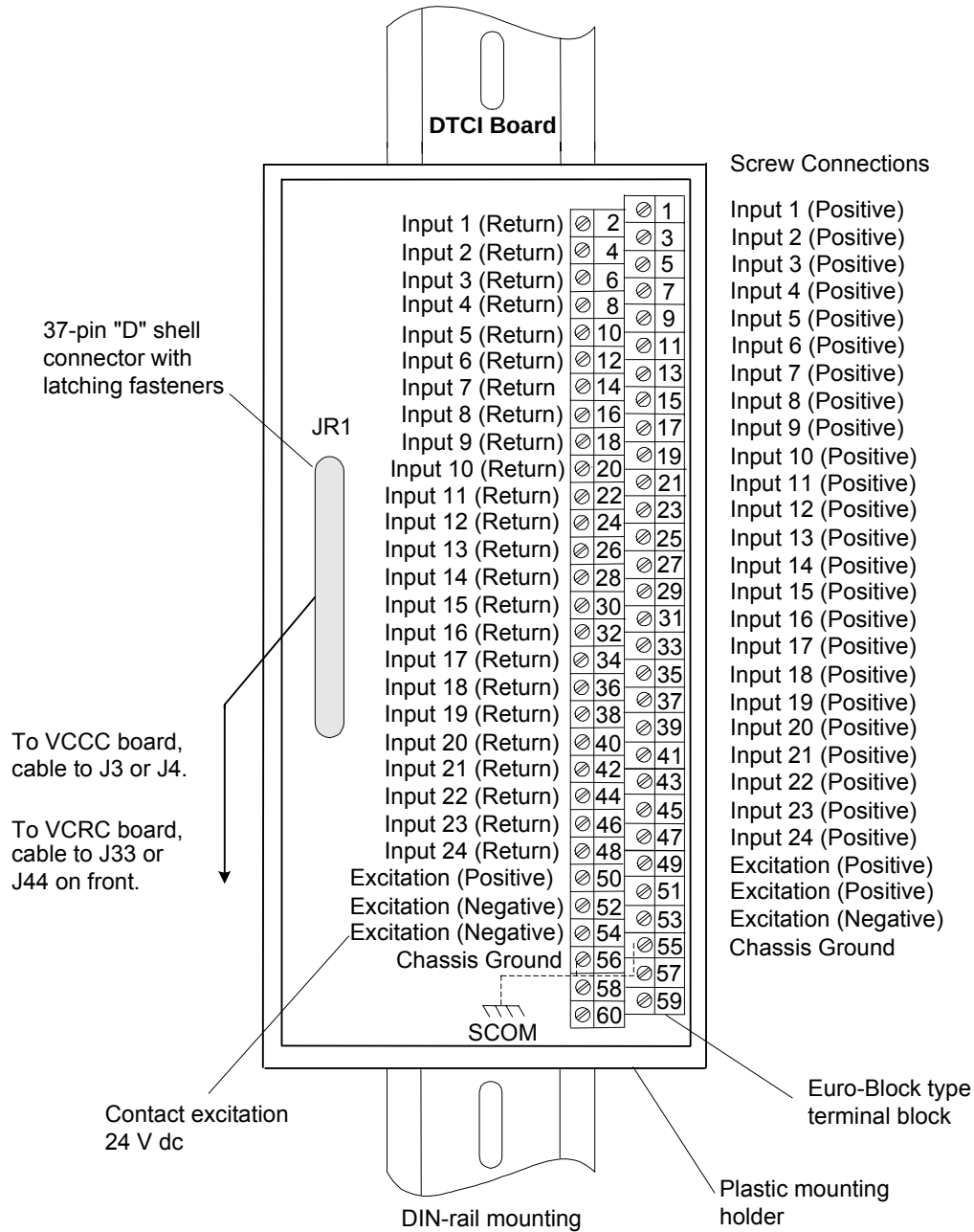
Note DTCI does not work with the PDIA I/O Pack.

Installation

Note There is no shield terminal strip with this design.

Mount the plastic holder on the DIN-rail and slide the DTCI board into place. Connect the wires for the contact inputs directly to the terminal block. The Euro-Block type terminal block has 60 terminals and is permanently mounted on the terminal board. Typically #18 AWG wires are used. Two screws, 55 and 56, are provided for the SCOM (ground) connection, which should be as short a distance as possible. Six screws are provided for the 24 V dc excitation power.

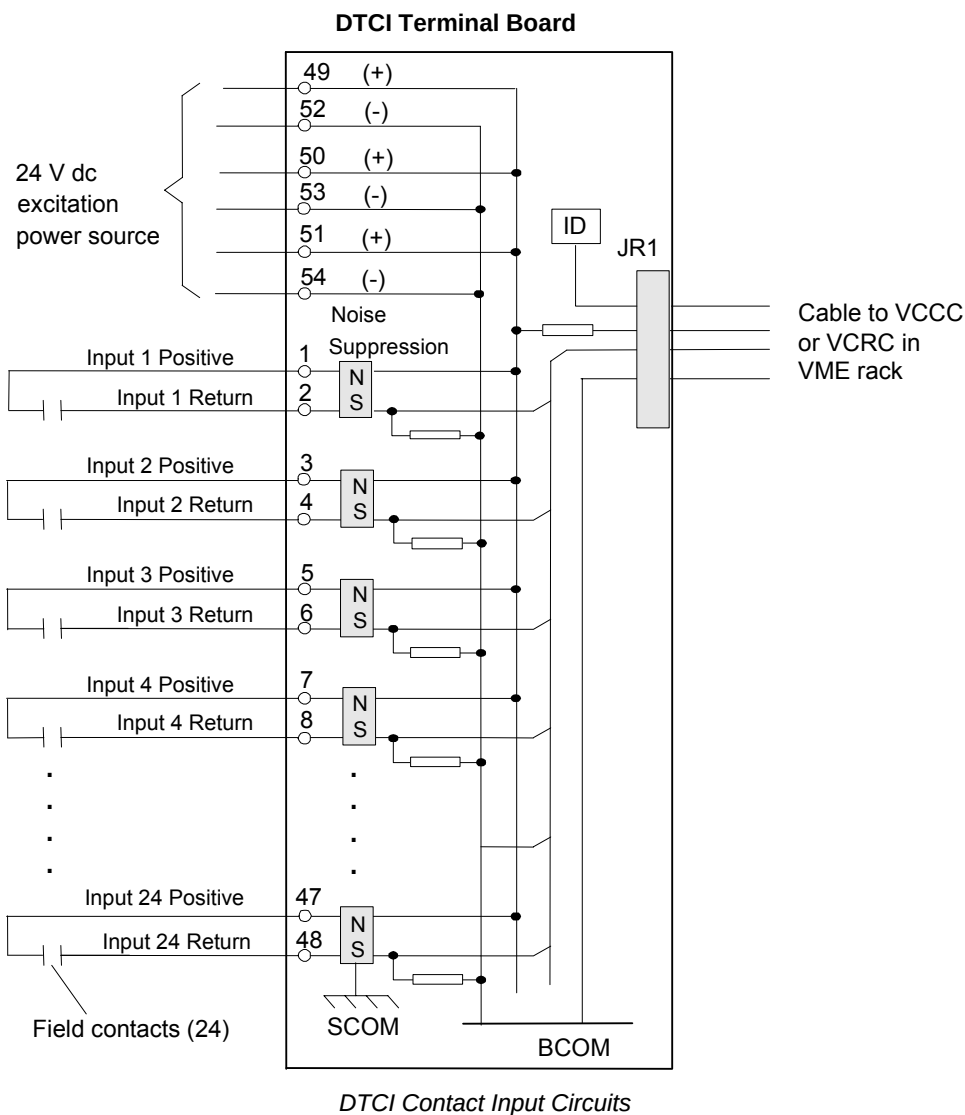
Note SCOM must be connected to ground.



Operation

DTCI has the same functionality and on-board signal conditioning as TBCI, except they are scaled for 24 V dc. The input excitation ranges from 18 to 32 V dc, and the threshold voltage is 50% of the excitation voltage. The ac voltage rejection is 12 V rms. Contact inputs take 2.5 mA nominal current on the first 21 circuits, and 10 mA on circuits 22 through 24.

Filters reduce high frequency noise and suppress surge on each input near the point of signal entry. The discrete input voltage signals are cabled to the VCCC board (or VCRC), which passes them through optical isolators and transfers the signals over the VME backplane to the VCM1. The VCM1 then sends them to the controller.



Specifications

Item	Specification
Number of channels	24 dry contact voltage input channels
Excitation voltage	Nominal 24 V dc, floating, ranging from 18 to 32 V dc
Input current	First 21 circuits each draw 2.5 mA (50 k Ω) Last three circuits each draw 10 mA (12.5 k Ω)
Input filter	Hardware filter, 4 ms
Temperature rating	0 to 60°C (32 to 140 °F)
Fault detection in I/O board	Loss of contact input excitation voltage Non-responding contact input in test mode Unplugged cable
Physical	
Size, with support plate	8.6 cm wide x 16.2 cm high (3.4 in x 6.37 in)
Temperature	0 to 60°C (32 to 140 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The excitation voltage is monitored. If the excitation drops to below 40% of the nominal voltage, a diagnostic alarm is set and latched by the I/O pack/board.
- As a test, all inputs associated with this terminal board are forced to the open contact (fail safe) state. Any input that fails the diagnostic test is forced to the failsafe state and a fault is created.
- If the input from this board does not match the TMR voted value from all three boards, a fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

TRLYH1B Relay Output with Coil Sensing

Functional Description

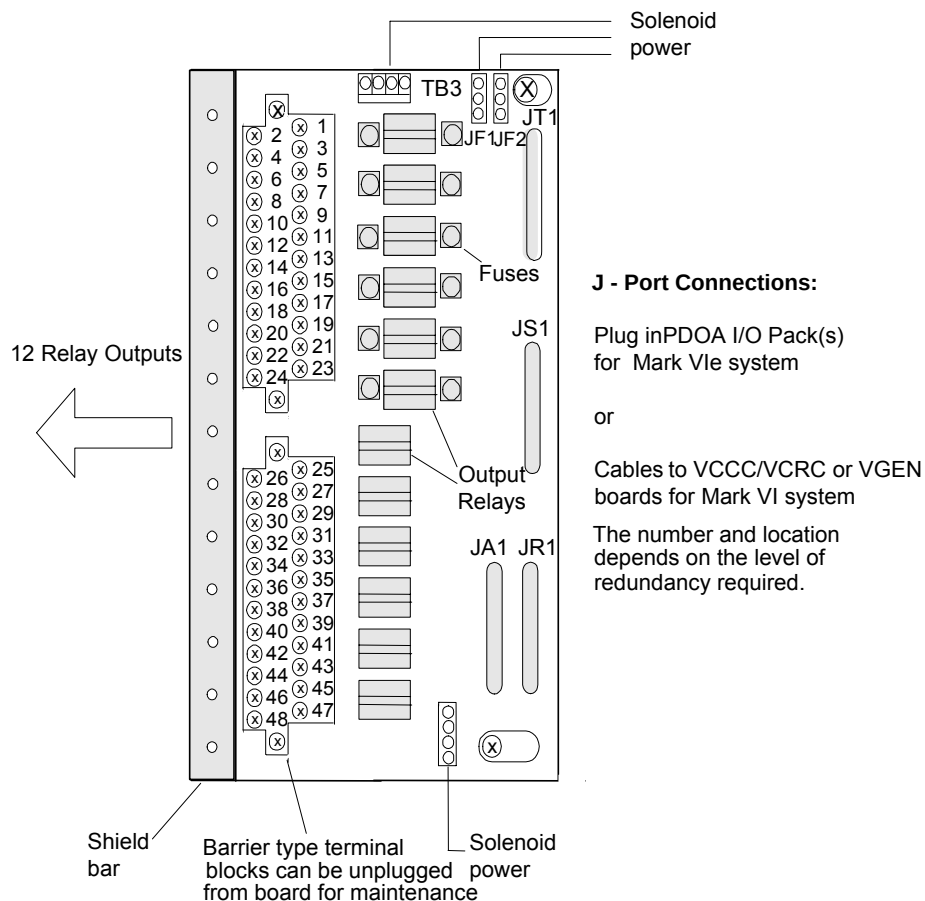
The Relay Output with coil sensing (TRLYH1B) terminal board holds 12 plug-in magnetic relays. The first six relay circuits configured by jumpers for either dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115/230 V ac source, or an optional 24 V dc source with individual jumper selectable fuses and on-board suppression, can be provided for field solenoid power. The next five relays (7-11) are unpowered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications such as ignition transformers.

Mark VI Systems

In Mark* VI systems, TRLY is controlled by the VCCC, VCRC, or VGEN board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Mark VIe Systems

In the Mark VIe system, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



TRLYH1B Relay Output Terminal Board

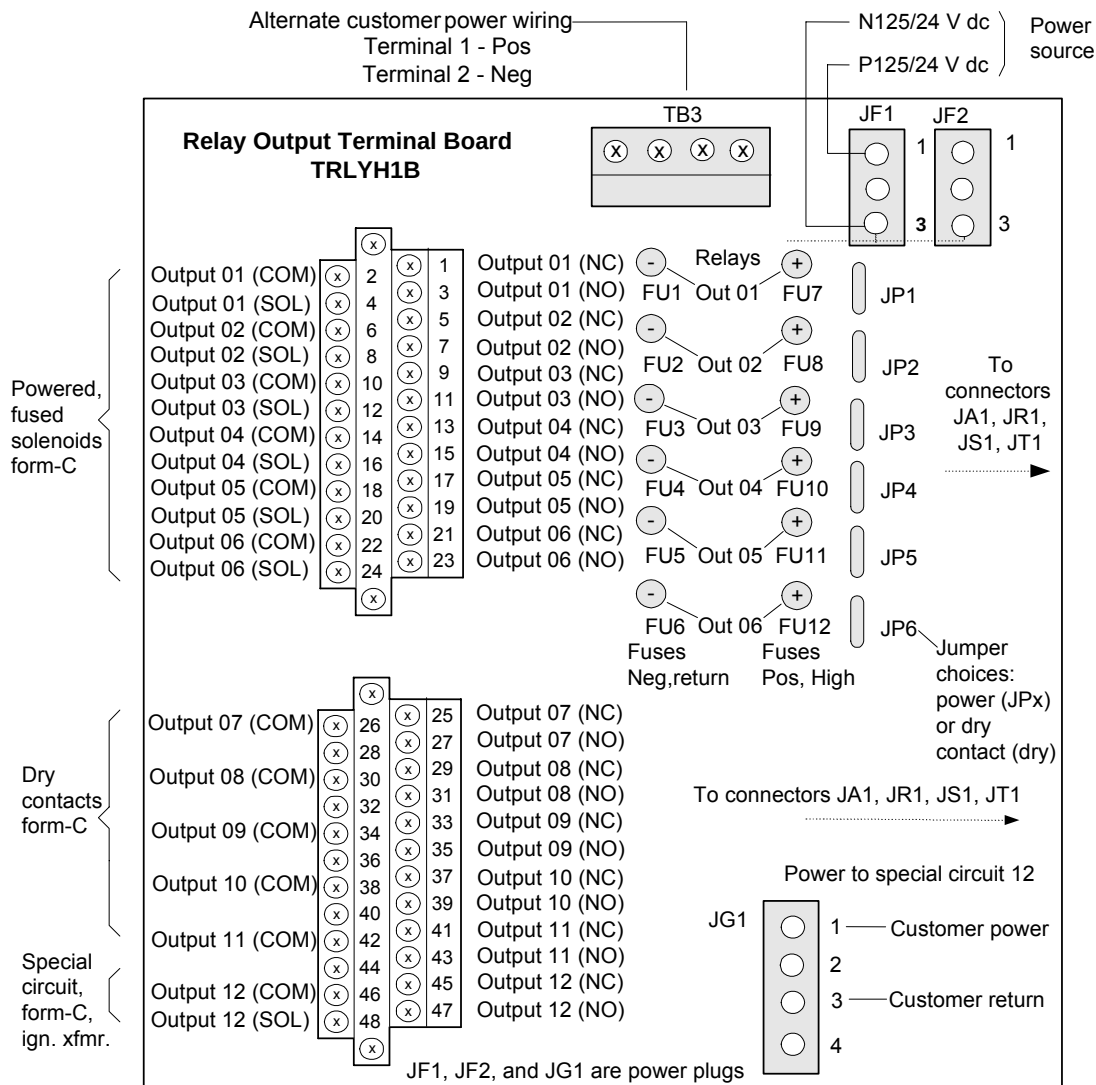
Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as shown in the figure, *TRLYH1B Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on to the left side of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-JP6 are removed in the factory and shipped in a plastic bag. Re-install the appropriate jumper if power to a field solenoid is required. Conduct individual loop energization checks as per standard practices and install the jumpers as required. For isolated contact applications, remove the fuses to ensure that suppression leakage is removed from the power bus.

Note These jumpers are also for isolation of the monitor circuit when used on isolated contact applications.

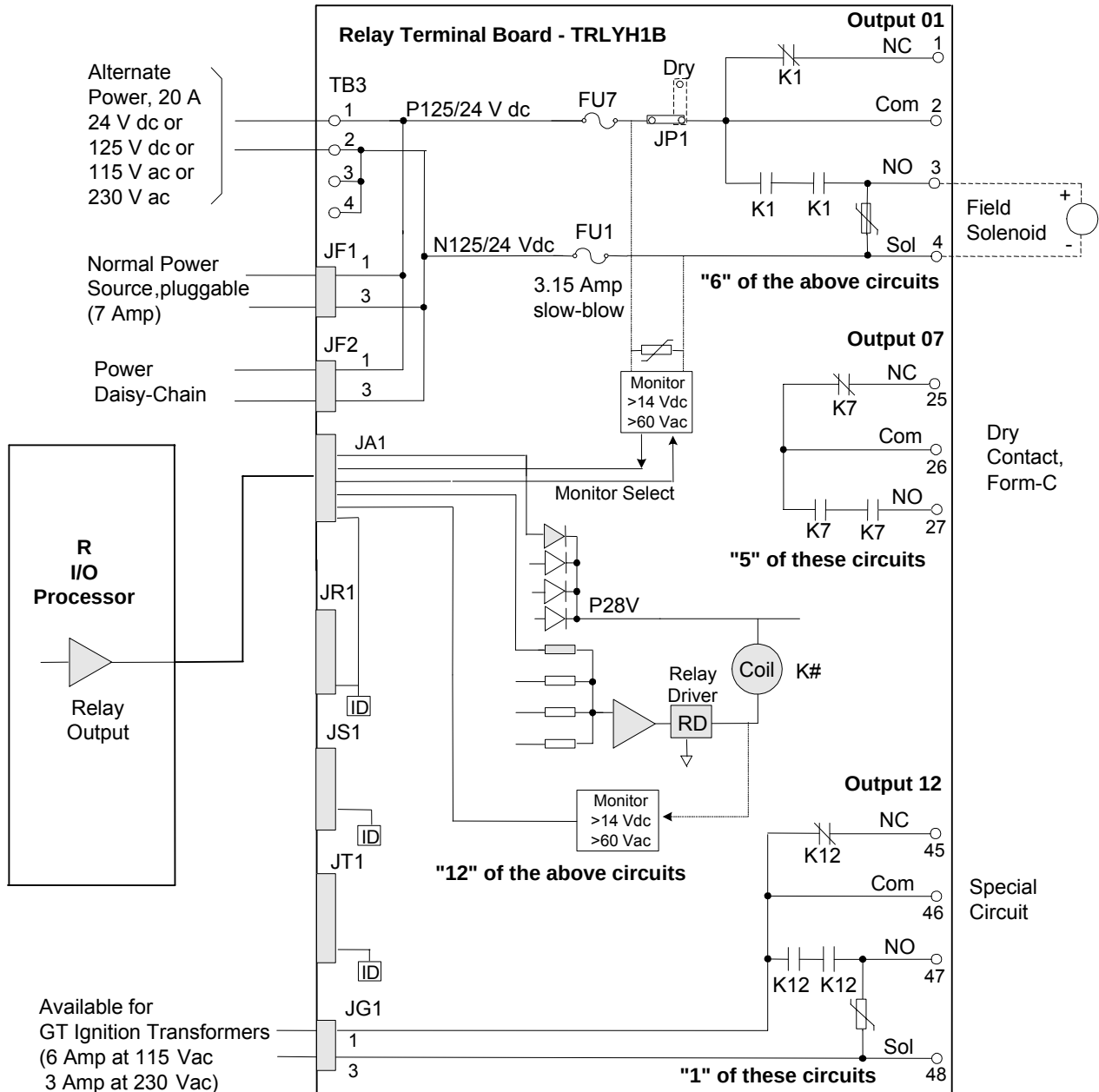


TRLYH1B Terminal Board Wiring

Operation

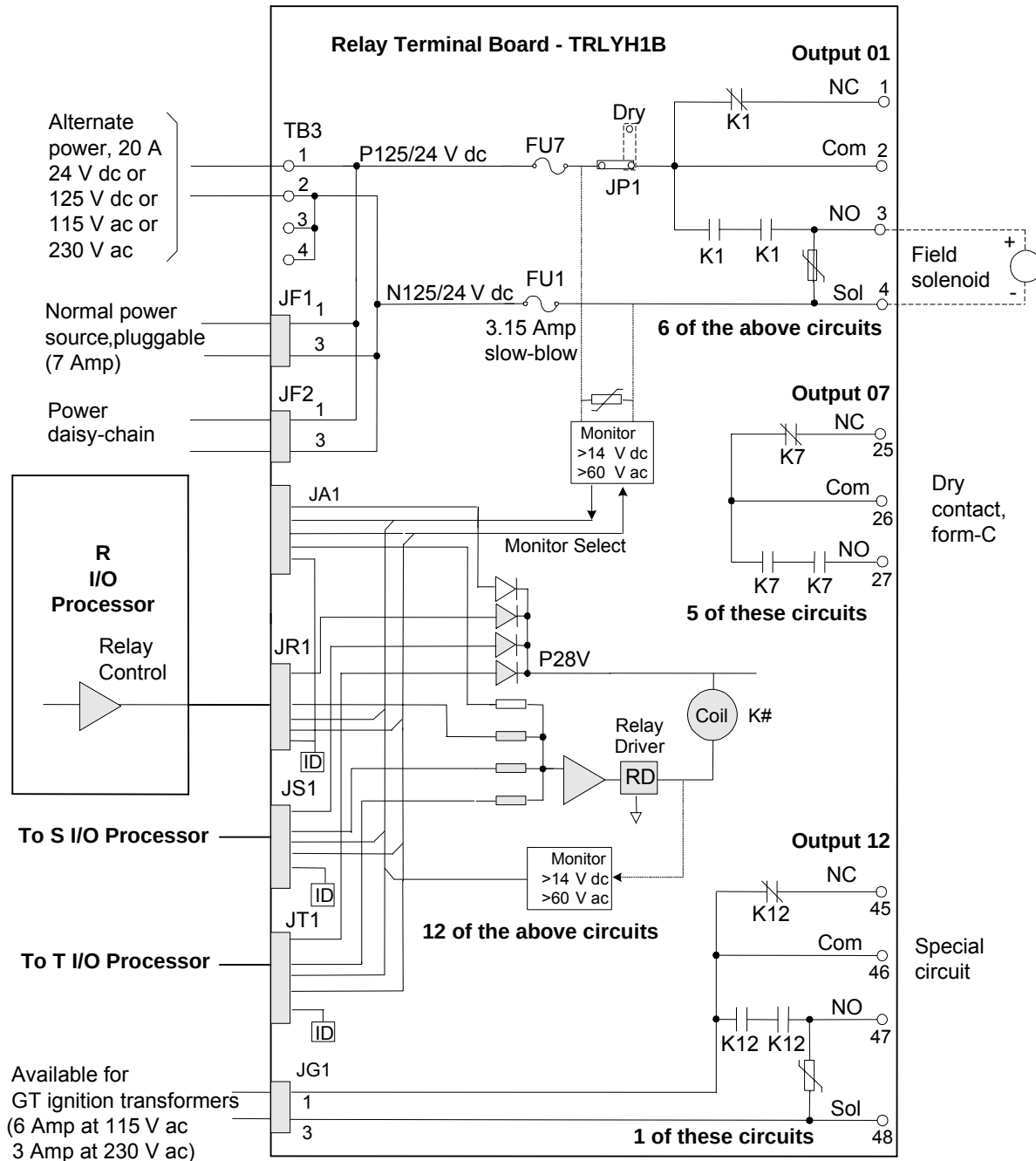
Relay drivers, fuses, and jumpers are mounted on the TRLYH1B. For simplex operation, D-type connectors carry control signals and monitor feedback voltages between the I/O processors and TRLY through JA1.

Relays are driven at the frame rate and have a 3.0 A rating. The rated contact-to-contact voltage is 500 V ac for one minute. The rated coil to contact voltage is 1,500 V ac for one minute. The typical time to operate is 10 ms. Relays 1-6 have a 250 V metal oxide varistor (MOV) for transient suppression between normally open (NO) and the power return terminals. The relay outputs have a failsafe feature that vote to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O processor is lost.



TRLYH1B Circuits, Simplex System

For TMR applications, relay control signals are fanned into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes from all three I/O processors and is diode-shared. The following figure shows a TRLYH1B in a TMR system.



TRLYH1B Circuits, TMR System

Specifications

Item	Specifications
Number of relay channels on one TRLY board	12: 6 relays with optional solenoid driver voltages 5 relays with dry contacts only 1 relay with 7 A rating
Rated voltage on relays	a: Nominal 125 V dc or 24 V dc b: Nominal 115/230 V ac
Max load current	a: 0.6 A for 125 V dc operation b: 3.0 A for 24 V dc operation c: 3.0 A for 115/230 V ac, 50/60 Hz operation
Max response time on	25 ms typical
Max response time off	25 ms typical
Maximum inrush current	10 A
Contact material	Silver cad-oxide
Contact life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault detection	Loss of relay solenoid excitation current Coil current disagreement with command Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost.
Physical	
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_XXXX occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1. Refer to terminal board wiring diagram for more information.

TRLYH1C Relay Output with Contact Sensing

Functional Description

The Relay Output with contact sensing (TRLYH1C) terminal board holds 12 plug-in magnetic relays. The first six relay circuits are Form-C contact outputs to drive external solenoids. A standard 125 V dc or 115 V ac source with fuses and on-board suppression is provided for field solenoid power. TRLYH2C holds 12 plug-in magnetic relays. The first six relay circuits are Form-C contact outputs to drive external solenoids. A standard 24 V dc source with fuses and on-board suppression is provided for field solenoid power.

The next five relays (7-11) are unpowered, isolated Form-C contacts. Output 12 is an isolated Form-C contact with non-fused power supply, used for ignition transformers. For example, 12 NO contacts have jumpers to apply or remove the feedback voltage sensing.

TRLYH1C and H2C are the same as the standard TRLYH1B board except for the following:

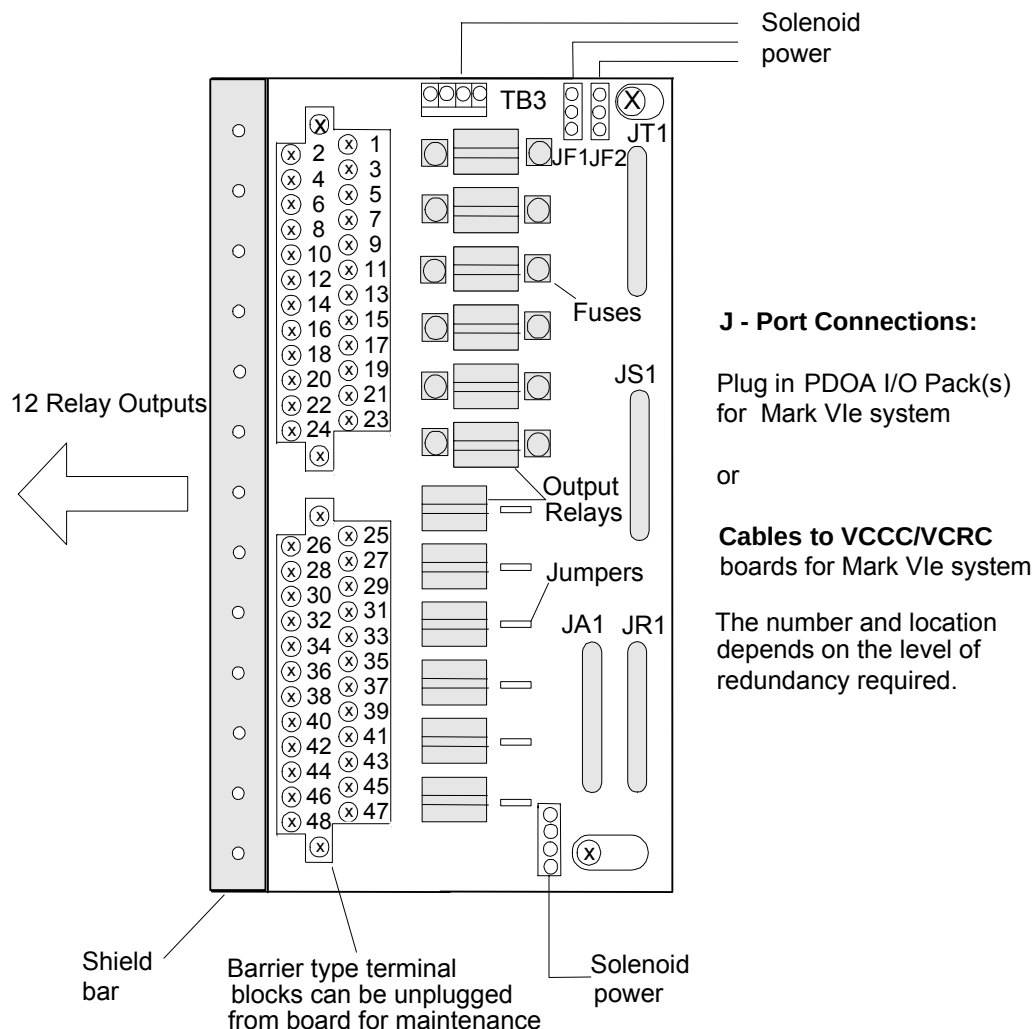
- Six jumpers for converting the solenoid outputs to dry contact type are removed. These jumpers were associated with the fuse monitoring.
- Input relay coil monitoring is removed from the 12 relays.
- Relay contact voltage monitoring is added to the 12 relays. Individual monitoring circuits have voltage suppression and can be isolated by removing their associated jumper.
- High-frequency snubbers are installed across the NO and SOL terminals on the six solenoid driver circuits and on the special circuit, output 12.

Mark VI Systems

In the Mark* VI system, the TRLY is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Mark VIe Systems

In the Mark VIe system, TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



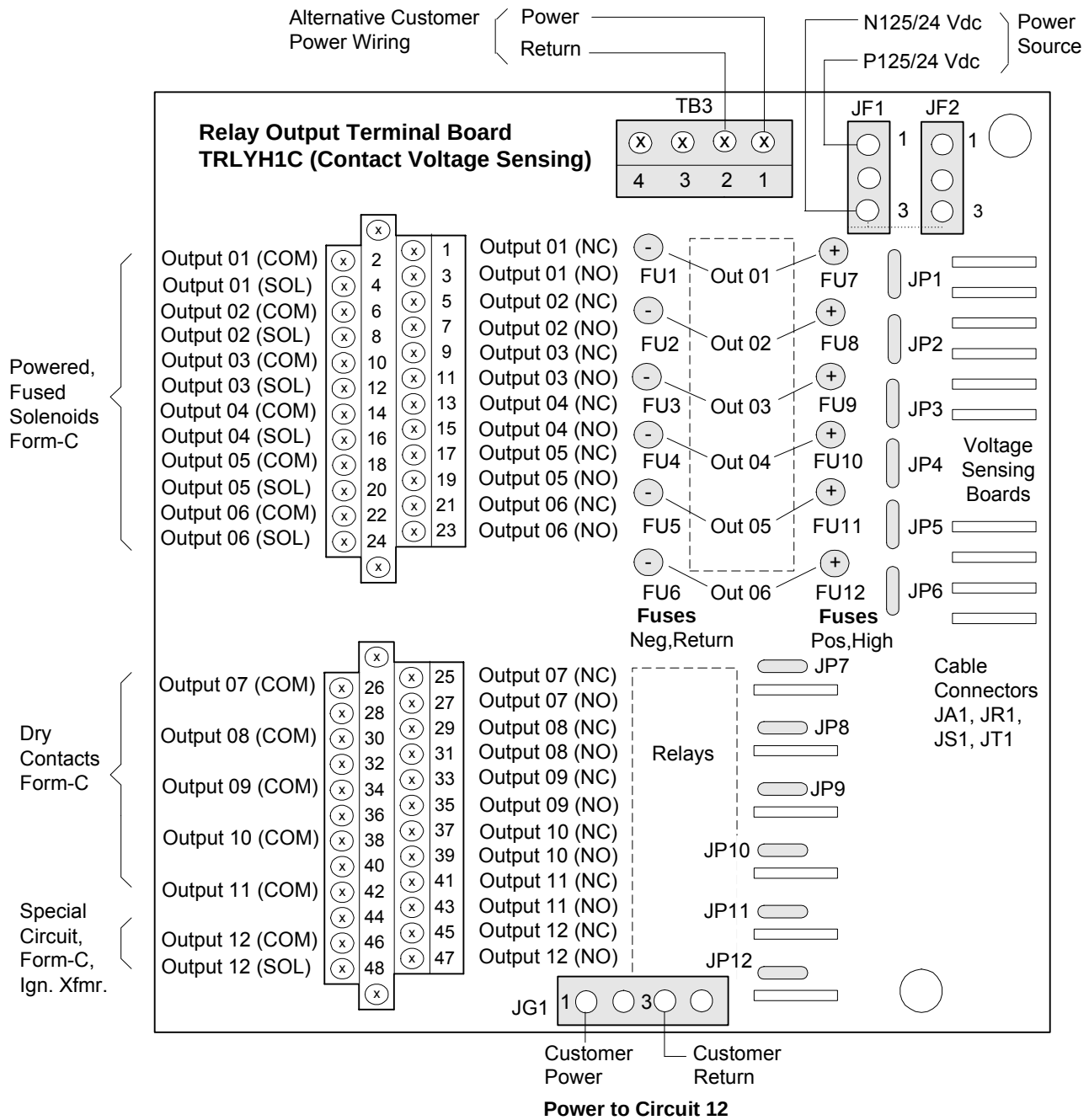
TRLYH1C Relay Output Terminal Board With Voltage Sensing

Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as shown in the figure, *TRLYH1C Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1 normally. JF2 can be used to daisy-chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-12 remove the voltage monitoring from selected outputs.



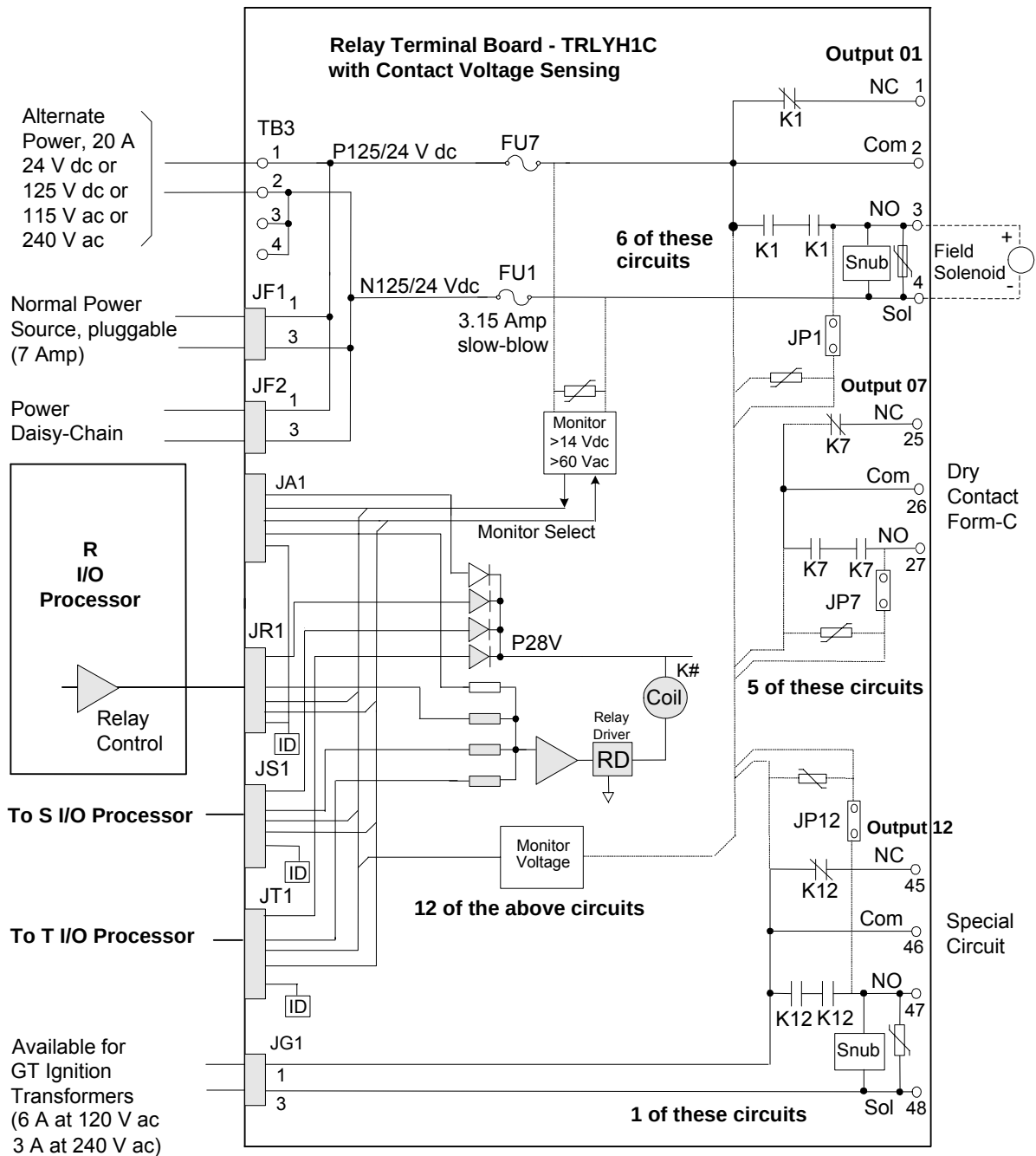
TRLYH1C Terminal Board Wiring

Operation

Relay drivers, fuses, and jumpers are mounted on the TRLYH1C. Relays 1-6 have a 250 V MOV for transient suppression between the NO and power return terminals.

Relays are driven at the frame rate and have a 3.0 A rating. The rated contact-to-contact voltage is 500 V ac for one minute. The rated coil to contact voltage is 1,500 V ac for one minute. The typical time to operate is 10 ms. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board is lost.

For simplex operation, a cable carries control signals and monitor feedback voltages between the I/O board and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O boards R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. The 28 V power for the relay coils comes in from all three I/O boards and is diode-shared. The following figure shows a TRLYH1C in a TMR system.



TRLYH1C Circuits

Specifications

Item	Specifications
Number of relay channels on one TRLY board	12: Six relays with solenoid driver voltages Five relays with dry contacts only One relay with 7 A rating
Rated voltage on relays	a: Nominal 125 V dc or 24 V dc b: Nominal 120 V ac or 240 V ac
Max load current	a: 0.6 A for 125 V dc operation b: 3.0 A for 24 V dc operation c: 3.0 A for 115/230 V ac, 50/60 Hz operation
Max response time on	25 ms typical
Max response time off	25 ms typical
H1C contact feedback threshold	70-145 V dc, nominal 125 V dc, threshold 45 to 65 V dc 90-132 V rms, nominal 115 V rms, 47-63 Hz, threshold 45 to 72 V ac 190-264 V rms, nominal 230 V rms, 47-63 Hz, threshold 45 to 72 V ac
H2C contact feedback threshold	16-32 V dc, nominal 24 V dc, threshold 10 to 16 V dc
Max response time off	25 ms typical
Contact material	Silver cad-oxide
Contact life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault detection	Loss of relay excitation current NO contact voltage disagreement with command Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost
Physical	
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to 149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1. Refer to terminal board wiring diagram for more information.

TRL YH1D Relay Output with Servo Integrity Sensing

Functional Description

The Relay Output with Solenoid Integrity Sensing (TRL YH1D) terminal board holds six plug-in magnetic relays. The six relay circuits are Form-C contact outputs, powered and fused to drive external solenoids. A standard 24 V dc or 125 V dc source can be used. The board provides special feedback on each relay circuit to detect a bad external solenoid. Sensing is applied between the NO output terminal and the SOL output terminal.

TRL YH1D is similar to the standard TRL YH1B board except for the following:

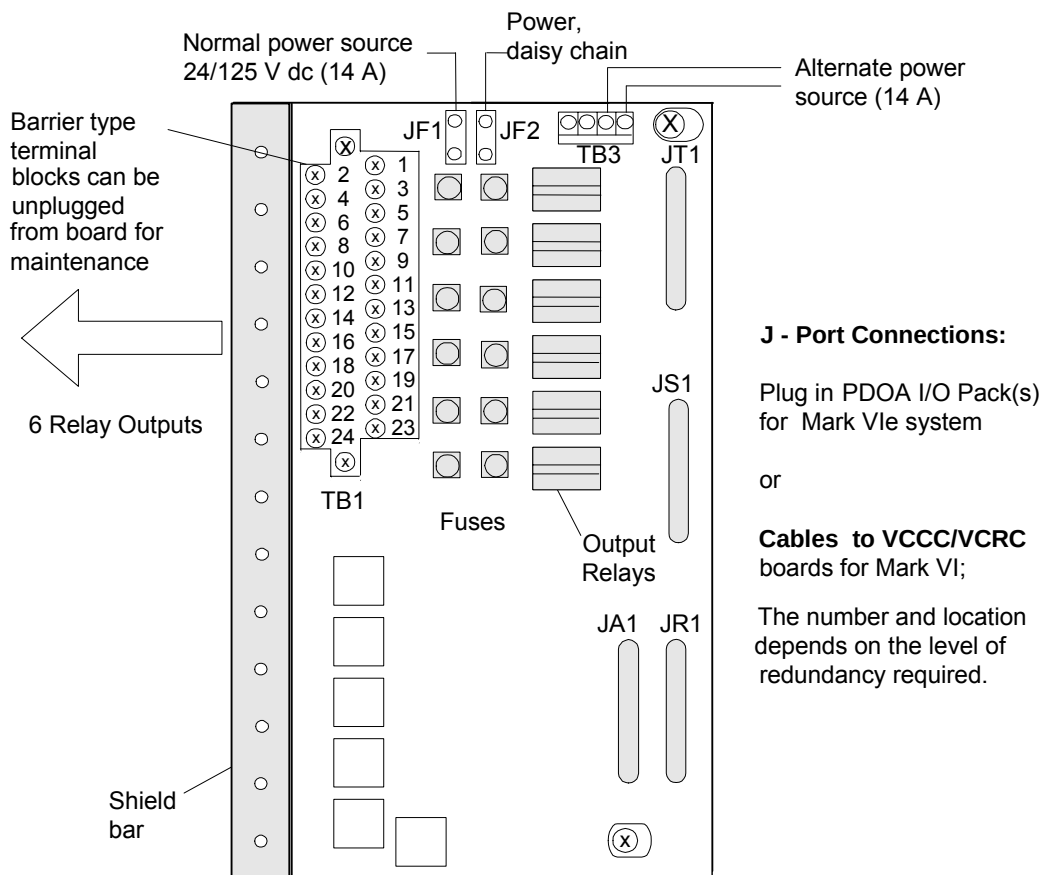
- There are only six relays.
- The board is designed for 24/125 V dc applications only.
- Relay circuits have a NO contact in the return side as well as the source side.
- The relays cannot be configured for dry contact use.
- Input relay coil monitoring is removed.
- The terminal board provides monitoring of field solenoid integrity.
- There is no special-use relay for driving an ignition transformer.

Mark VI Systems

In the Mark* VI systems, the TRL Y is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Mark VIe Systems

In the Mark VIe systems, the TRL Y works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

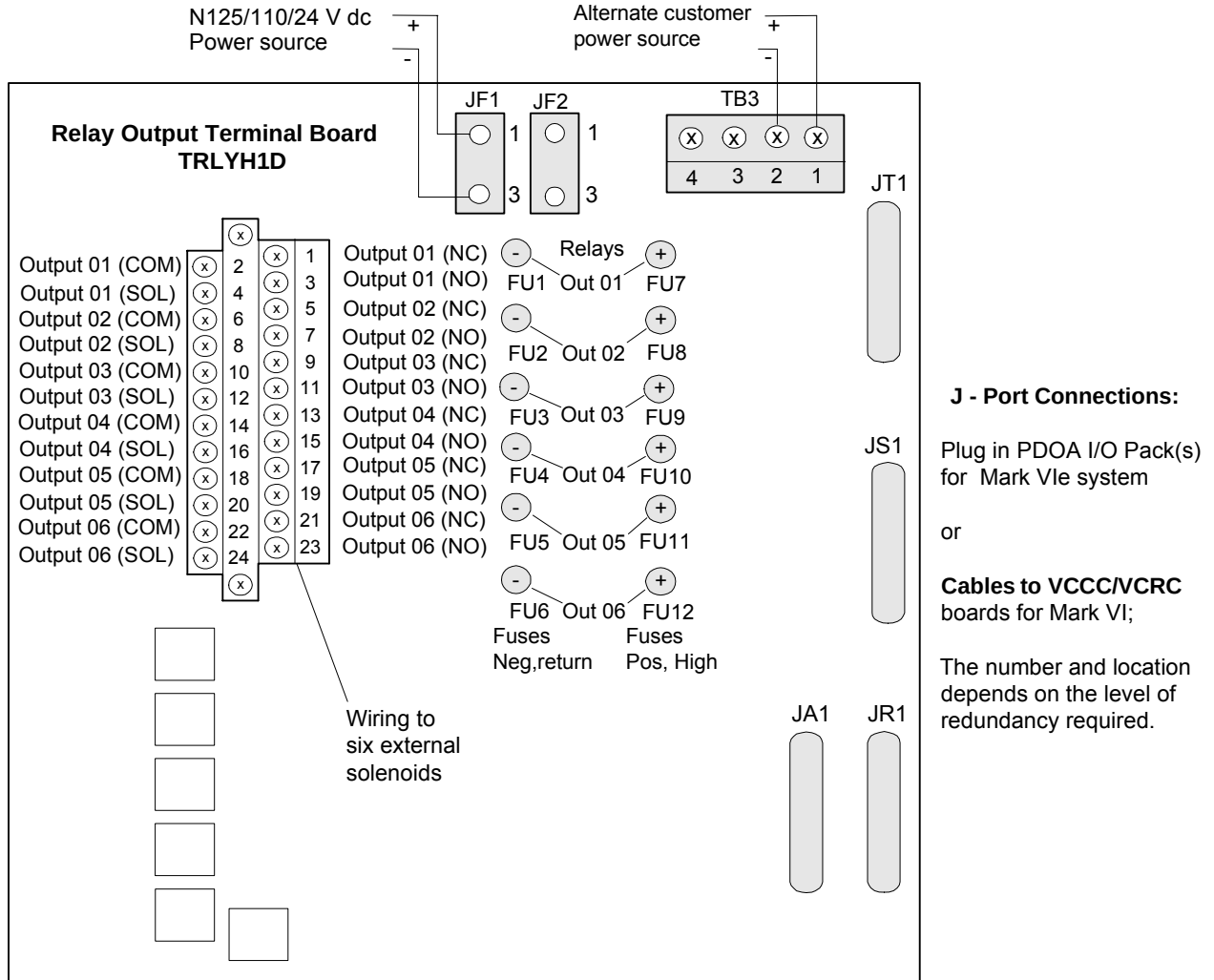


TRLYH1D Relay Output Terminal Board

Installation

Connect the wires for the six relay outputs directly to the TB1 terminal block on the terminal board as shown in the figure, TRLYH1D Terminal Board Wiring. The block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip, attached to chassis ground, is located immediately to the left of the terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy-chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used.

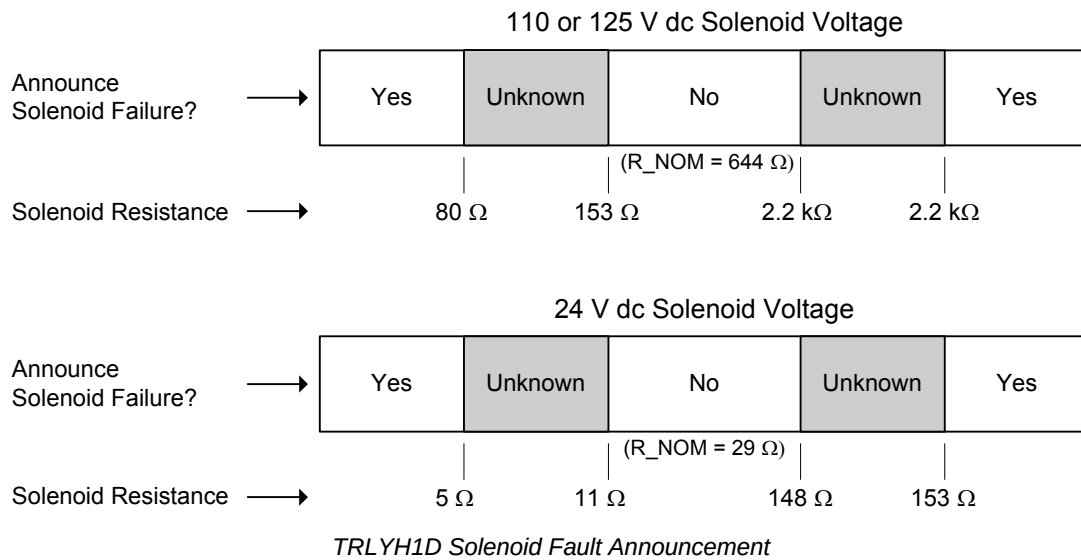


TRLYH1D Terminal Board Wiring

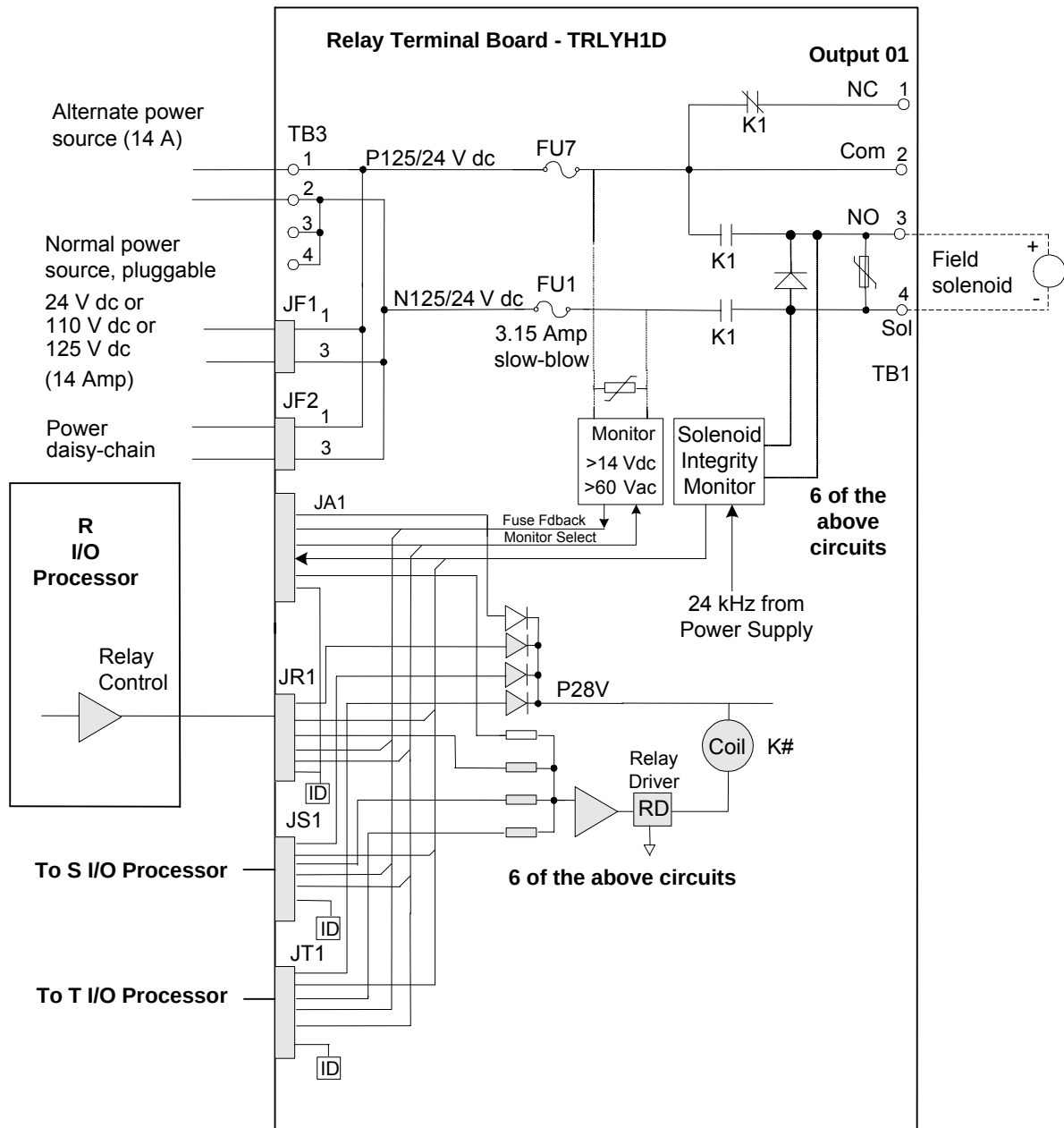
Operation

The six relays have a MOV and clamp diode for transient suppression between the NO and power return terminals. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board is lost.

TRL YH1D monitors each solenoid between the NO and SOL output terminals. When the relay is de-energized, the circuit applies a bias of less than 8% nominal voltage to determine if the load impedance is within an allowable band. If the impedance is too low or high for consecutive scans, an alarm feedback is generated. The contacts must be open for at least 1.3 seconds to get a valid reading.



For simplex operation, cables carry control signals and solenoid monitoring feedback voltages between the I/O board and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O processor boards R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes in from all three I/O boards and is diode-shared. The following figure shows TRLYH1D in a TMR system.



TRLYH1D Circuits, TMR System

Specifications

Item	Specification
Number of relay channels	Six relays with special customer solenoid monitoring
Rated voltage on relays	Nominal 125 V dc or 24 V dc
Relay contact rating for 24 V dc voltage	Current rating 10 A, resistive Current rating 2 A, L/R = 7 ms, without suppression
Relay contact rating for 125 V dc voltage	Current rating 0.5 A, resistive Current rating 0.2 A, L/R = 7 ms, without suppression Current rating 0.65 A, L/R = 150 ms, with suppression (MOV) across the load
Maximum response time on	25 ms typical
Maximum response time off	25 ms typical
Contact life	Electrical operations: 100,000
Board size	17.8 cm by 33.0 cm (7 in by 13 in)
Fault detection	Loss of solenoid voltage supply (fuse monitor) Solenoid resistance measured to detect open and short circuits Unplugged cable or loss of communication with I/O board (relays de-energize if communication with associated I/O board is lost)
Physical	
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Temperature	-30 to +65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

There are no jumpers or hardware settings on the board.

TRLYH1E Solid-State Relay Output

Functional Description

The solid-state Relay Output (TRLYH1E) terminal board is a 12-output relay board using solid-state relays for the outputs and featuring isolated output voltage feedback on all 12 circuits. The solid-state relays allow the board to be certified for Class 1 Division 2 applications. The use of solid-state relays requires three different board types:

- TRLYH1E for 115 V ac applications
- TRLYH2E for 24 V dc applications
- TRLYH3E for 125 V dc applications

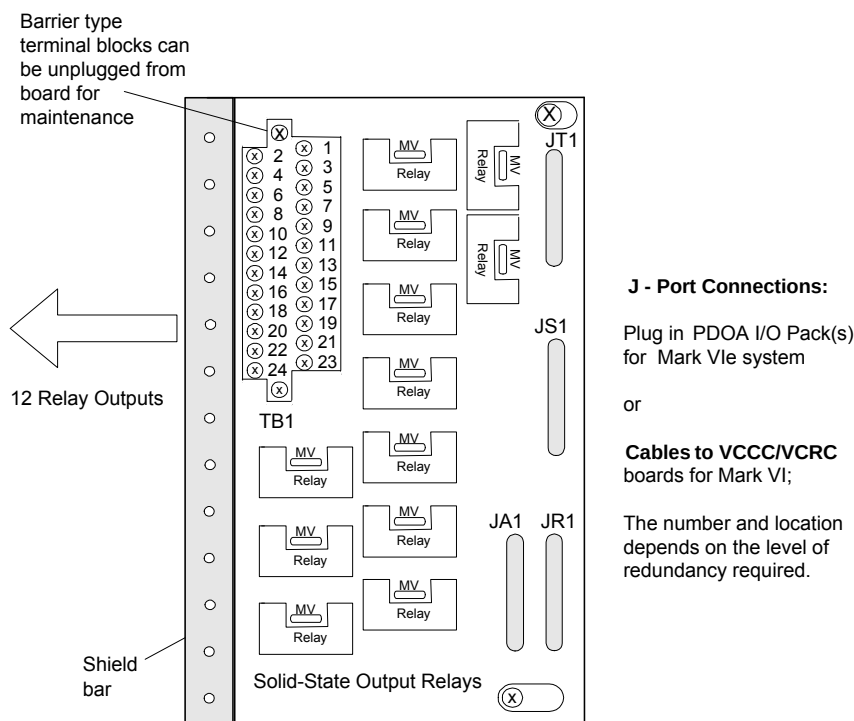
Unlike the form-C contacts provided on the mechanical relay boards, all 12 outputs on TRLYH1E are single, NO, contacts. There is no user solenoid power distribution on the board.

Mark VI Systems

In the Mark* VI system, the TRLY is controlled by the VCCC or VCRC board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Mark VIe Systems

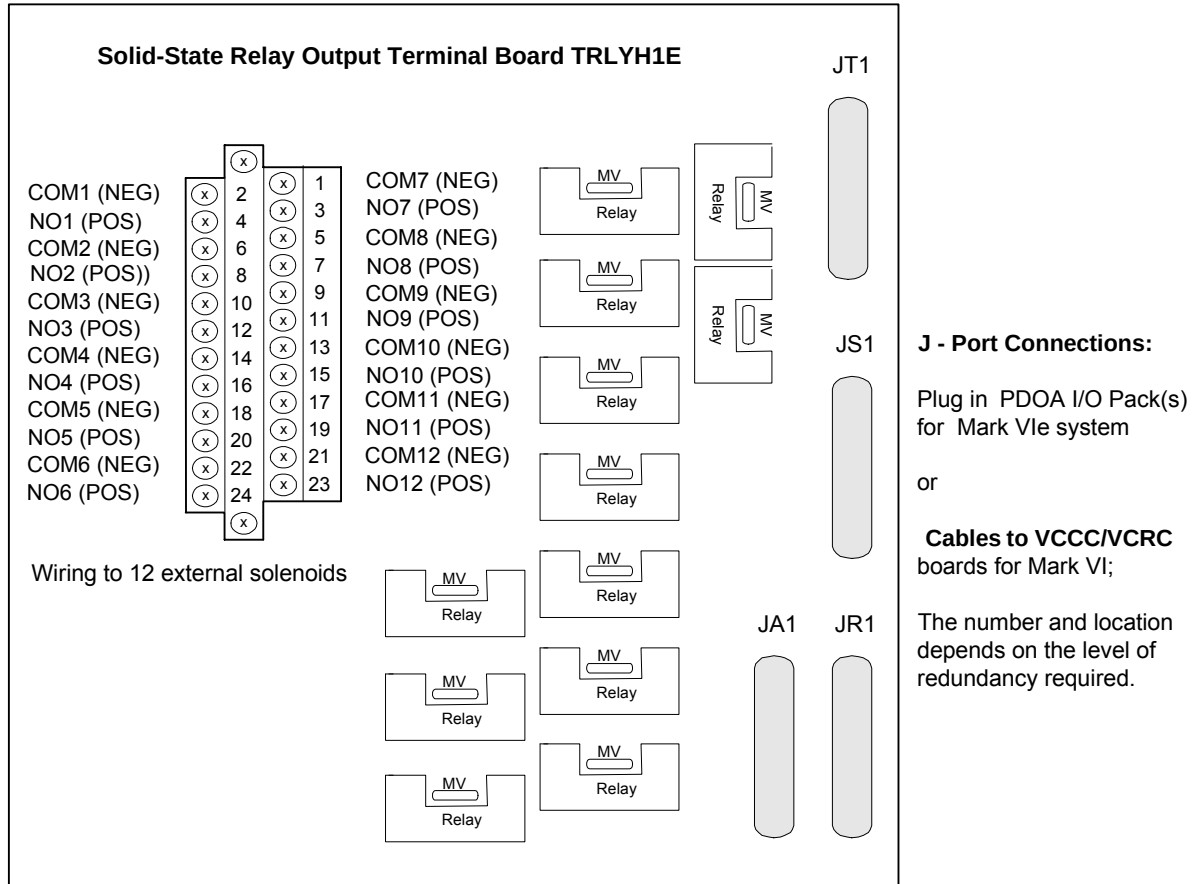
In the Mark VIe system, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



TRLYH1E Solid-State Relay Output Terminal Board

Installation

Connect the wires for the 12 solenoids directly to the I/O terminal block on the terminal board as shown in the figure, *TRLYH1E Terminal Board Wiring*. The terminal block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. The dc relays are unidirectional, so care should be taken about polarity when connecting load to these relays. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block. The solenoids must be powered externally by the customer.

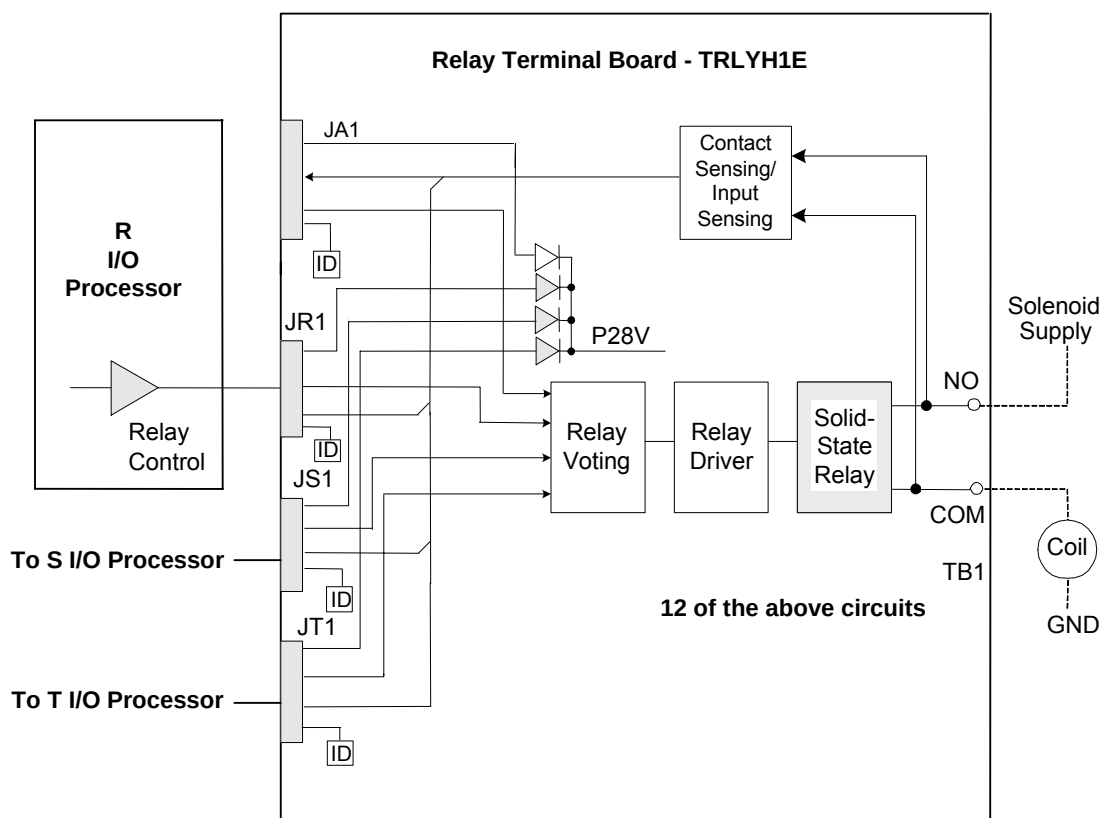


TRLYH1E Terminal Board Wiring

Operation

NO solid-state relays, relay drivers, and output monitoring are mounted on TRLYH1E. During power up, relays stay de-energized while connected to any control. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O processor is lost.

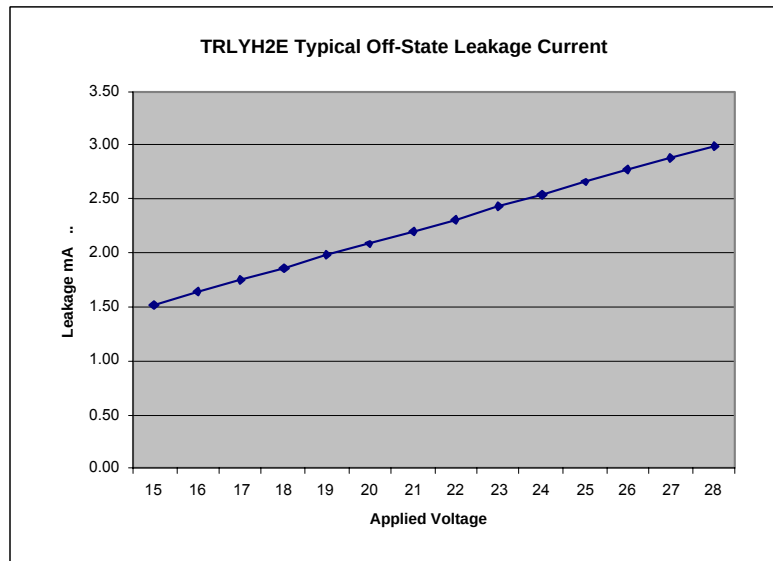
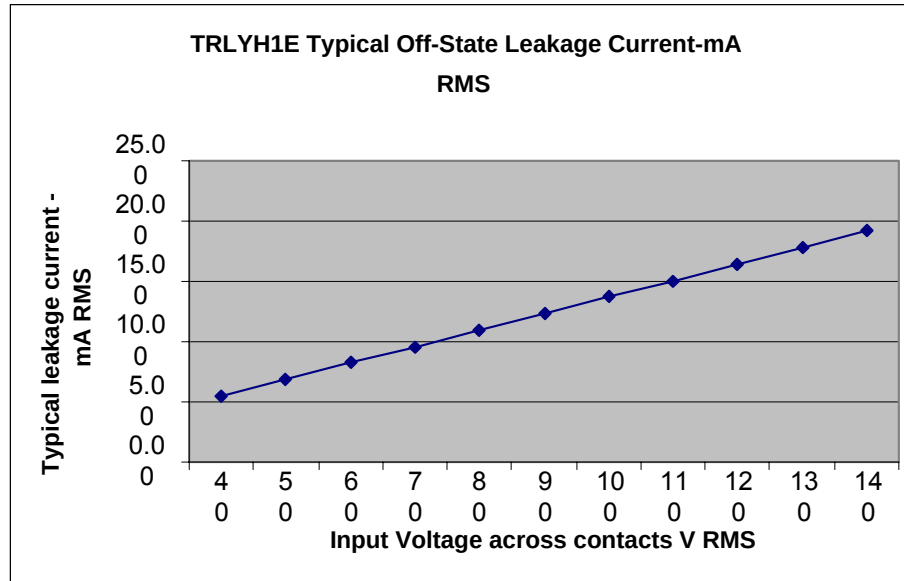
For simplex operation, control signals and relay output voltage feedback signals pass between the I/O processor and TRLY through JA1. For TMR applications, relay control signals are fanned into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay drivers comes in from all three I/O processors and is diode-shared. The following figure shows TRLYH1E in a TMR system.

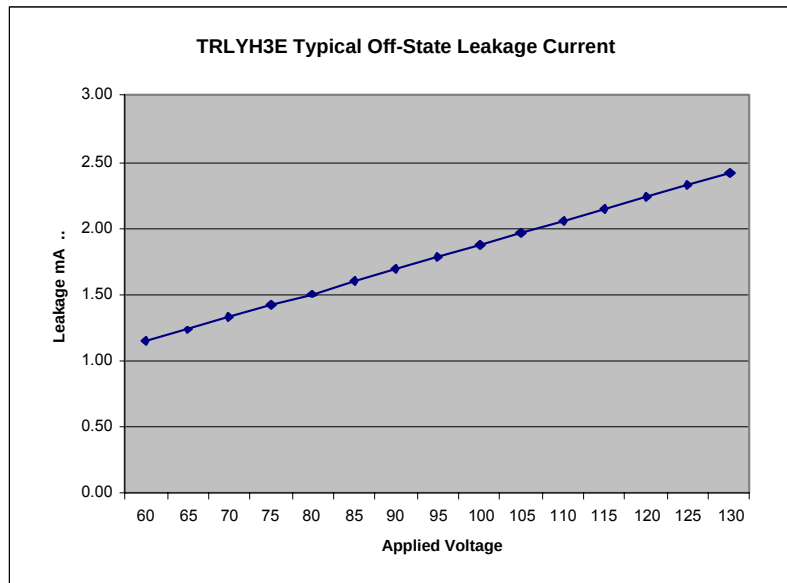


TRLYH1E Circuits, TMR System

Contact Voltage Feedback

In TRLYH1E, isolated feedback of voltage sensing is connected to the relay outputs. This allows the control to observe the voltage across the relay outputs without a galvanic connection. One contact sensing circuit is provided with each relay. This feature is similar to the voltage sensing on TRLYH1C but with simpler hardware. The voltage sensing circuit allows a small leakage current to pass to power the isolated circuit. The typical leakage current is the sum of the leakage through the turned off solid-state relay and the current through the voltage sensing circuit. The following charts indicate the typical leakage current as a function of the applied voltage for the three board types.





Due to the permitted leakage current, the board may give false indications if used in series with a low input current load, including common contact input circuits such as those found on TBCI or STCI. To ensure correct operation, the maximum load resistances for the three board types are as follows:

- TRL YH1E: Maximum load resistance at nominal 115 V ac is 2.5 k Ω .
- TRL YH2E: Maximum load resistance at nominal 24 V dc is 4.5 k Ω .
- TRL YH3E: Maximum load resistance at nominal 125 V dc is 25 k Ω .

Load resistance may be decreased by applying a resistor in parallel with the load so the parallel combination satisfies the maximum resistance requirement.

Contact Voltage Rating

Solid-state relays have a finite transient voltage capability and require coordinated voltage protection. TRL YH1E for ac applications uses a load control device that turns off on a current zero crossing. This turn-off characteristic ensures that no inductive energy is present in the load at turn-off time. Basic protection of the ac relay is provided on TRL YH1E using a MOV with clamp voltage coordinated with relay voltage rating. In addition, there is an R-C snubber circuit on the relay output using a 56 Ω resistor in series with a 0.25 μ F capacitor.

Both the TRL YH2E (for 24 V dc applications) and the TRL YH3E (for 125 V dc applications) can interrupt currents in large inductive loads. Because a wide range of loads may be encountered, an appropriate R-C or diode snubber circuit must be selected for each application. The snubber should be applied at the load device using common engineering practices. If the applied snubber does not fully control inductive switching voltage transients, both board versions contain an active voltage clamp circuit. This circuit activates at approximately 50-55 V dc for the H2E and at approximately 164-170 V dc for the H3E (both values below the rating of the relay). While the clamp circuit has a finite ability to absorb energy, it can handle the wiring inductance of a resistive load.

Specifications

Item	Specification
Number of relay channels on one TRLY board	12 relays: 115 V ac operation with TRLYH1E 24 V dc operation with TRLYH2E 125 V dc operation with TRLYH3E
Maximum operating voltage and maximum load current with free convection air flow	1E: 250 V rms at 47-63 Hz. 10 A @25°C (77 °F) maximum de-rate current linearly to 6 A @ 65°C (149 °F) maximum 2E: 28 V dc 10 A dc @40°C (104 °F) maximum de-rate current linearly to 7 A dc @65°C (149 °F) maximum 3E: 140 V dc 3 A dc@40°C (104 °F)maximum de-rate current linearly to 2 A dc @65°C (149 °F)maximum
Maximum off state leakage (see charts of leakage vs. applied voltage)	1E: 3 mA rms 2E: 3 mA A dc at 55 V 3E: 2.5 mA A dc
Max response time on	1 ms for dc relays; ½ cycle for ac relay
Max response time off	300 micro seconds for dc relays; ½ cycle for ac relay
Relay MTBF	1E: 50 years 2E: 37 years 3E: 47 years
Relay contact voltage sensing threshold	1E: 115 V ac 70 V ±10% ac rms 2E: 24 V dc 15 V ±2 V dc 3E: 125 V dc 79 V ±10% dc
Operating temperature range	-30 to 65°C (-22 to +149 °F)
Operating humidity	5 to 95% non-condensing
Fault detection	Relay current disagreement with command Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost
Physical	
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

There are no jumpers or hardware settings on the board.

TRLYH1F Relay Output with TMR Contact Voting

Functional Description

The Relay Output with TMR contact voting (TRLYH1F) terminal board provides 12 contact-voted relay outputs. The board holds 12 sealed relays in each TMR section, for a total of 36 relays. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied.

Note TRLYH1F and H2F do not support simplex arrangements

TRLYH1F does not have power distribution. However, an optional power distribution board, IS200WPDFH1A, can be added so that a standard 125 V dc or 115 V ac source, or an optional 24 V dc source with individual fuses, can be provided for field solenoid power.

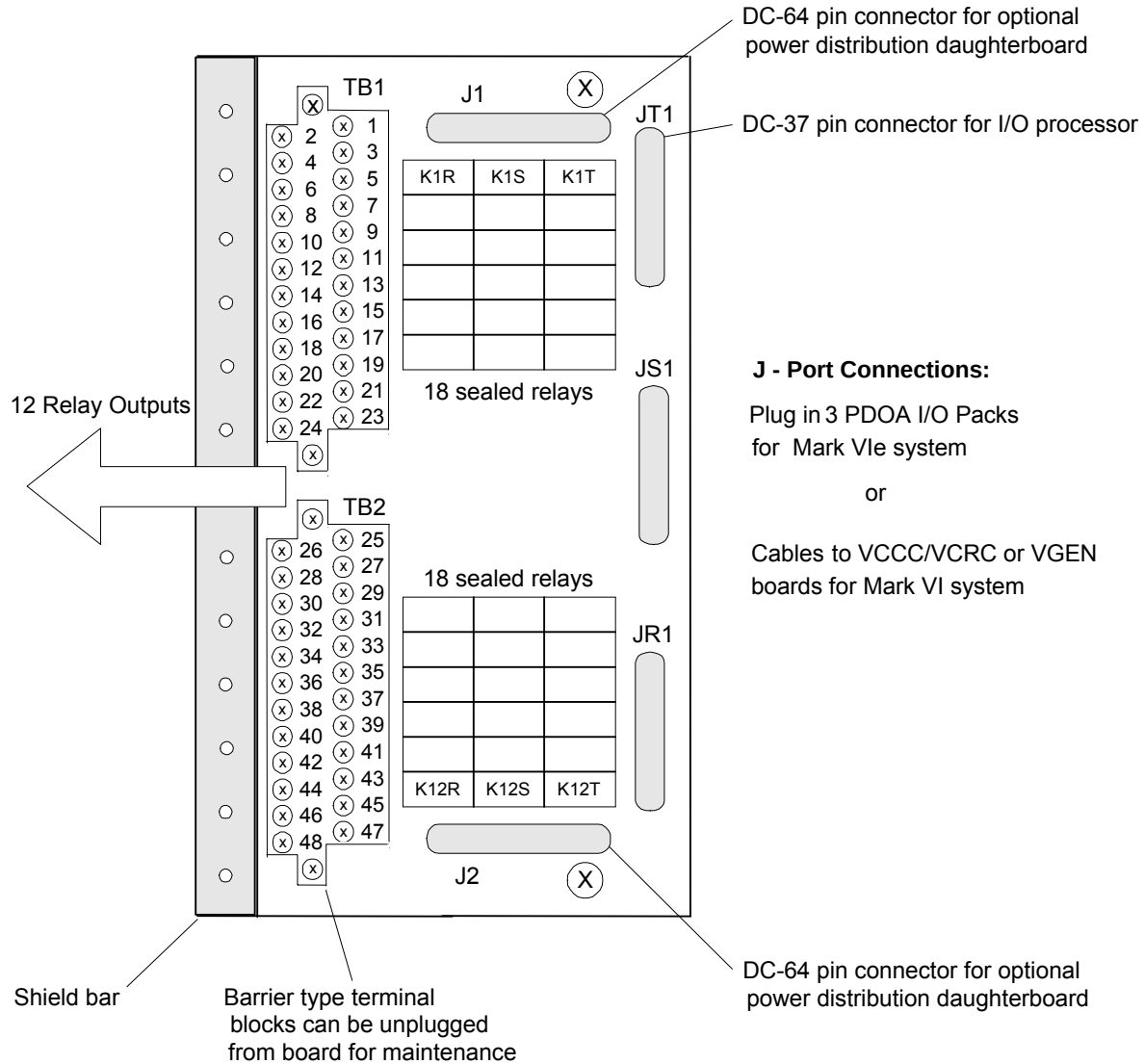
TRLYH2F is same as TRLYH1F except that the voted contacts form a Form B (NC) output. Both boards can be used in Class 1 Division 2 applications.

Mark VI Systems

In the Mark* VI system, the TRLY is controlled by the VCCC, VCRC, or VGEN board and only supports TMR applications. Cables with molded plugs connect JR1, JS1, and JT1 to the VME rack where the I/O boards are mounted.

Mark VIe Systems

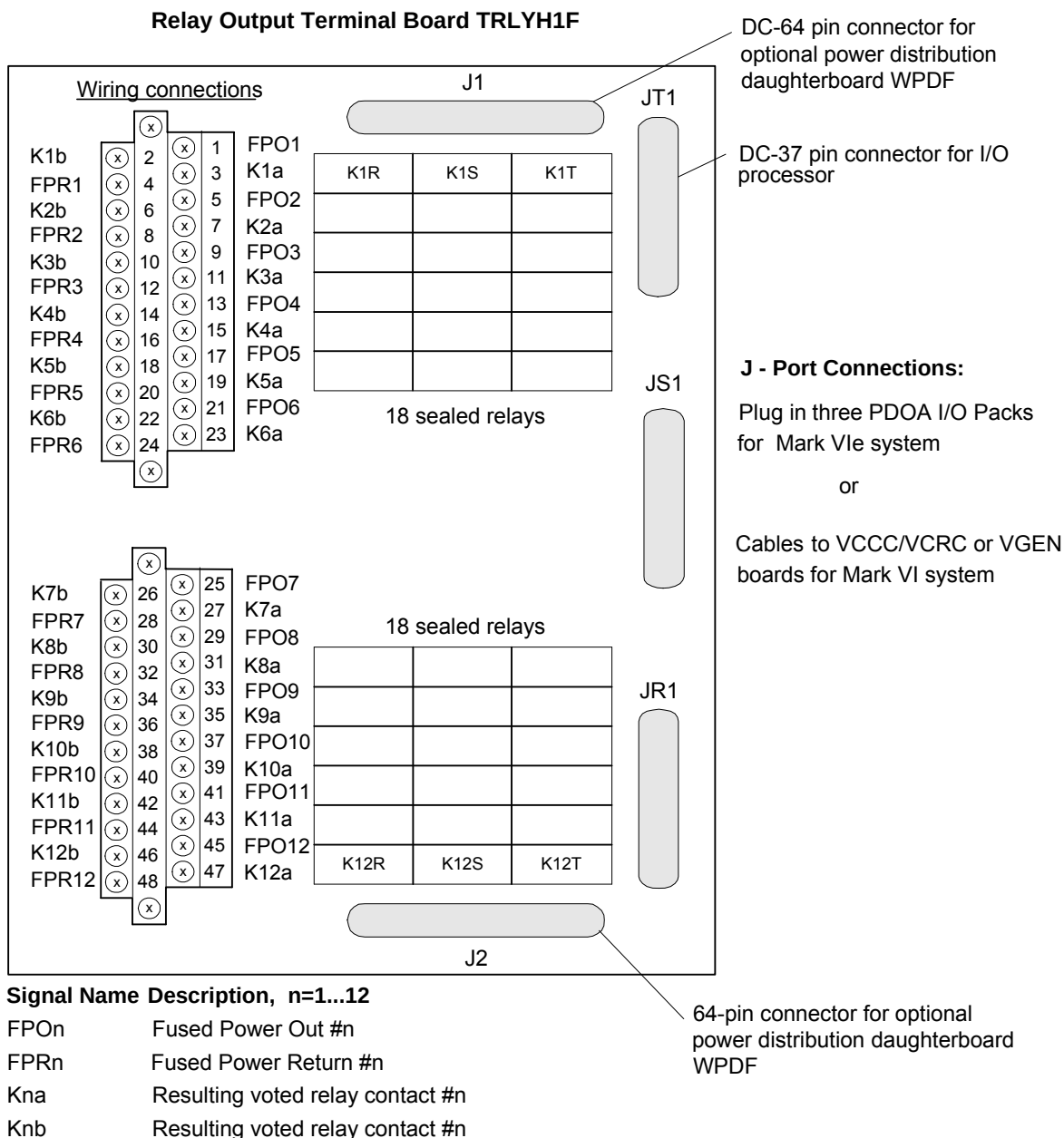
In the Mark VIe system, the TRLY works with PDOA I/O pack and only supports TMR applications. Three TMR PDOA packs plug into the JR1, JS1, and JT1 37-pin D-type connectors on the terminal board.



TRLYH1F Relay Output Terminal Board

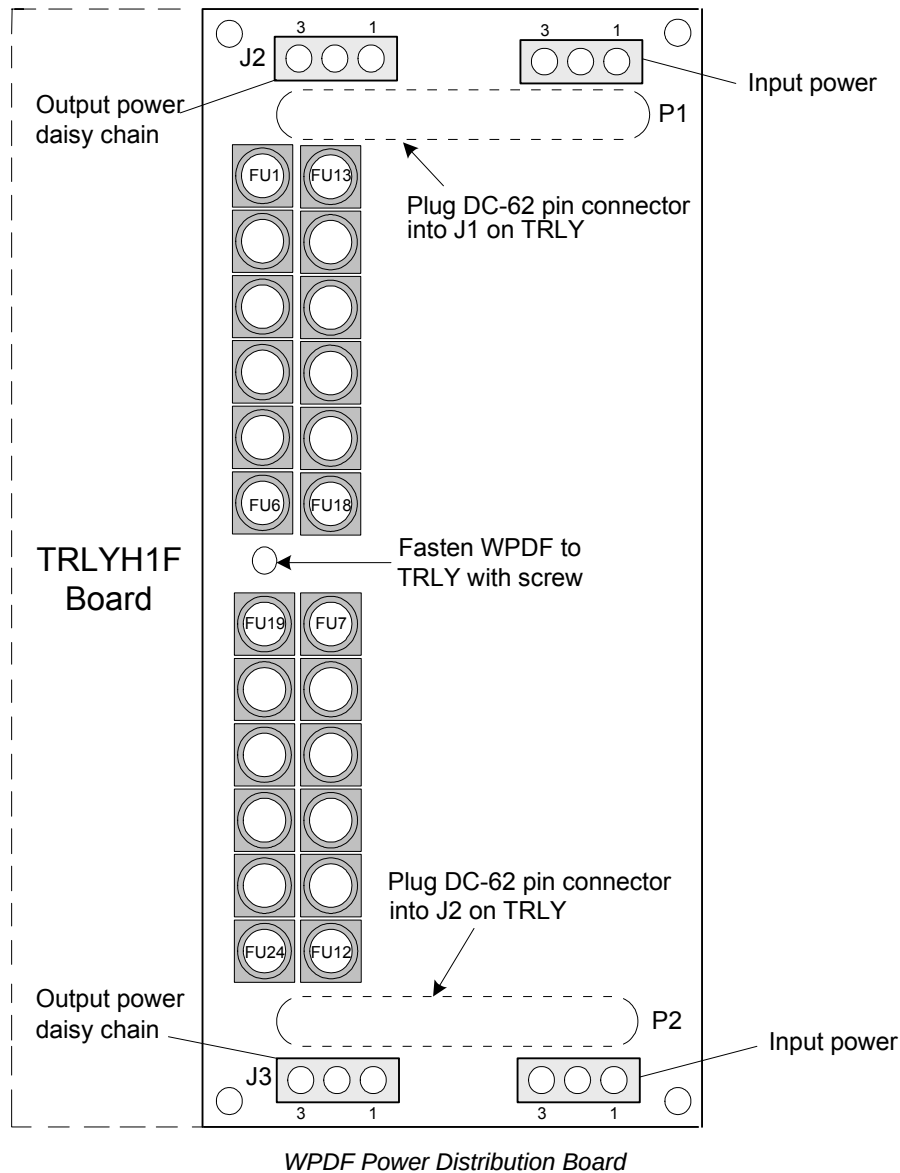
Installation

Connect the wires for the 12 solenoids directly to two I/O terminal blocks on the terminal board as shown in the following figure, *TRLYH1F Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left side of each terminal block. Solenoid power for outputs 1-12 is available if the WPDF daughterboard is used. Alternatively, power can be wired directly to the terminal block.

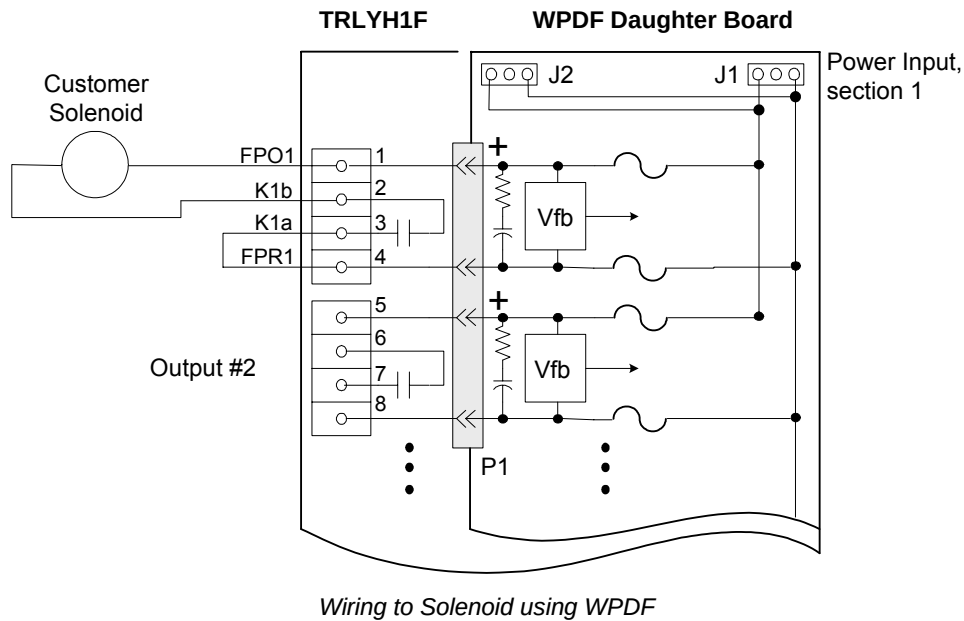


Power Distribution Board

If using the optional WPDF power distribution board, mount it on top of TRLY on the J1 and J2 connectors. Secure WPDF to TRLY by fastening a screw in the hole located at the center of WPDF. Connect the power for the two sections of the board on the three-pin connectors J1 and J4. Power can be daisy-chained out through the adjacent plugs, J2 and J3.



The solenoids must be wired as shown in the following figure. If WPDF is not used, the customer must supply power to the solenoids.



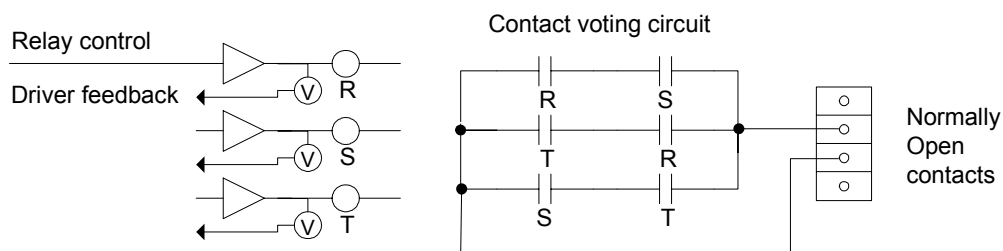
Operation

The 28 V dc power for the terminal board relay coils and logic comes from the three I/O processors connected at JR1, JS1, and JT1. The same relays are used for ac voltages and dc voltages, as specified in the *Specifications* section. H1F and H2F use the same relays with differing circuits.

Relay drivers are mounted on the TRLYH1F and drive the relays at the frame rate. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board or I/O pack is lost.

This board only supports TMR applications. The relay control signals are routed into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals directly control the corresponding relay driver for each TMR section R, S, and T. Power for each section's relay coils comes in from its own I/O processor and is not shared with the other sections.

TRLYH1F features TMR contact voting. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied. TRLYH2F is the same except that the voted contacts form a Form B (NC) output. The following figure shows TMR voting contact circuit.

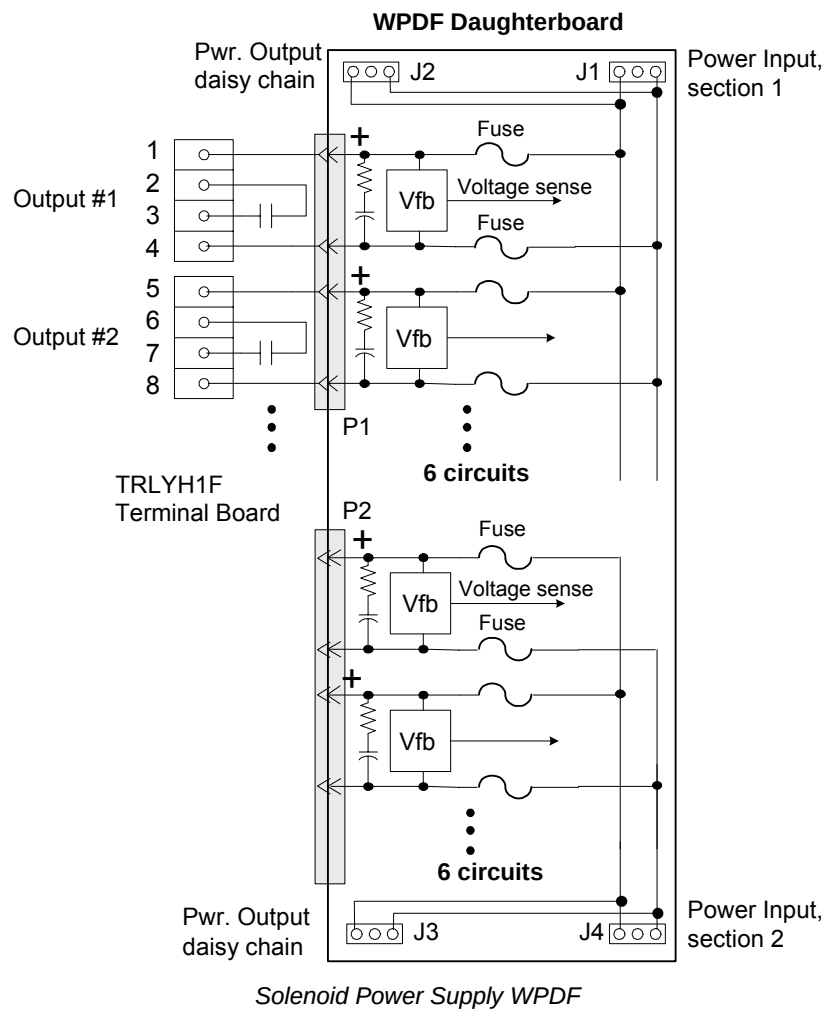


TRLYH1F Contact Arrangement for TMR Voting

Field Solenoid Power Option

The WPDFH1A daughterboard supplies power to TRLYH#F to power solenoids. WPDF holds two power distribution circuits, which can be independently used for standard 125 V dc, 115 V ac, or 24 V dc sources. Each section consists of six fused branches that provide power to TRLYH#F. Each branch has its own voltage monitor across its secondary fuse pair. Each voltage detector is fanned to three independent open-collector drivers for feedback to each of the I/O processors R, S, and T.

WPDF should not be used without TRLYH#F. Fused power flows through this board down to the TRLY terminal board points. TRLY controls the fuse power feedback. The following figure shows TRLYH1F/WPDF solenoid power circuit.



Specifications

Item	Specification
Number of output relay channels	12
Board types	H1F: NO contacts H2F: NC contacts
Rated voltage on relays	a: Nominal 100/125 V dc or 24 V dc b: Nominal 115 V ac
Maximum load current	a: 0.5/0.3 A resistive for 100/125 V dc operation b: 5.0 A resistive for 24 V dc operation c: 5.0 A resistive for 115 V ac
Maximum response time on Contact life	25 ms Electrical operations: 100,000
Fault detection	Coil Voltage disagreement with command Blown fuse indication (with WPDF power daughterboard). Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost.
WPDF Solenoid Power Distribution Board	
Number of Power Distribution Circuits (PDC)	2: Each rated 10 A, nominal 115 V ac or 125 V dc.
Number of Fused Branches	12: 6 for each PDC
Fuse rating	3.15 A at 25°C (77 °F) 2.36 A – recommended maximum usage at 65°C (149 °F)
Voltage monitor, maximum response delay	60 ms typical
Voltage monitor, minimum detection voltage	16 V dc 72 V ac
Voltage monitor, max current (leakage)	3 mA
Physical	
Size - TRLY	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Size - WPDF	10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to +149 °F)
Technology	Surface-mount

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The voltage to each relay coil is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The voltage across each solenoid power supply is monitored and if it goes below 16 V ac/dc, an alarm is created.
- If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location.

Details of the individual diagnostics are available from the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

There are no jumpers or hardware settings on the board.

DRLY Simplex Relay Output

Functional Description

The Simplex Relay Output (DRLY) terminal board is a compact relay output terminal board designed for wall mounting (not DIN-rail mounting). The board has 12 form-C dry contact output relays and connects to the VCCC, VCRC, or VTUR processor board with a single cable. The 37-pin cable connector is identical to those used on the larger TRLY terminal board. Two DRLY boards can be connected to VCCC, VCRC, or VTUR for a total of 24 contact outputs. Only a simplex version of this board is available.

There are two versions of the DRLY terminal board:

- H1A has higher powered relay contacts than H1B.
- H1B is suitable for use in UL listing for Class I, Division 2 Hazardous (classified) locations.

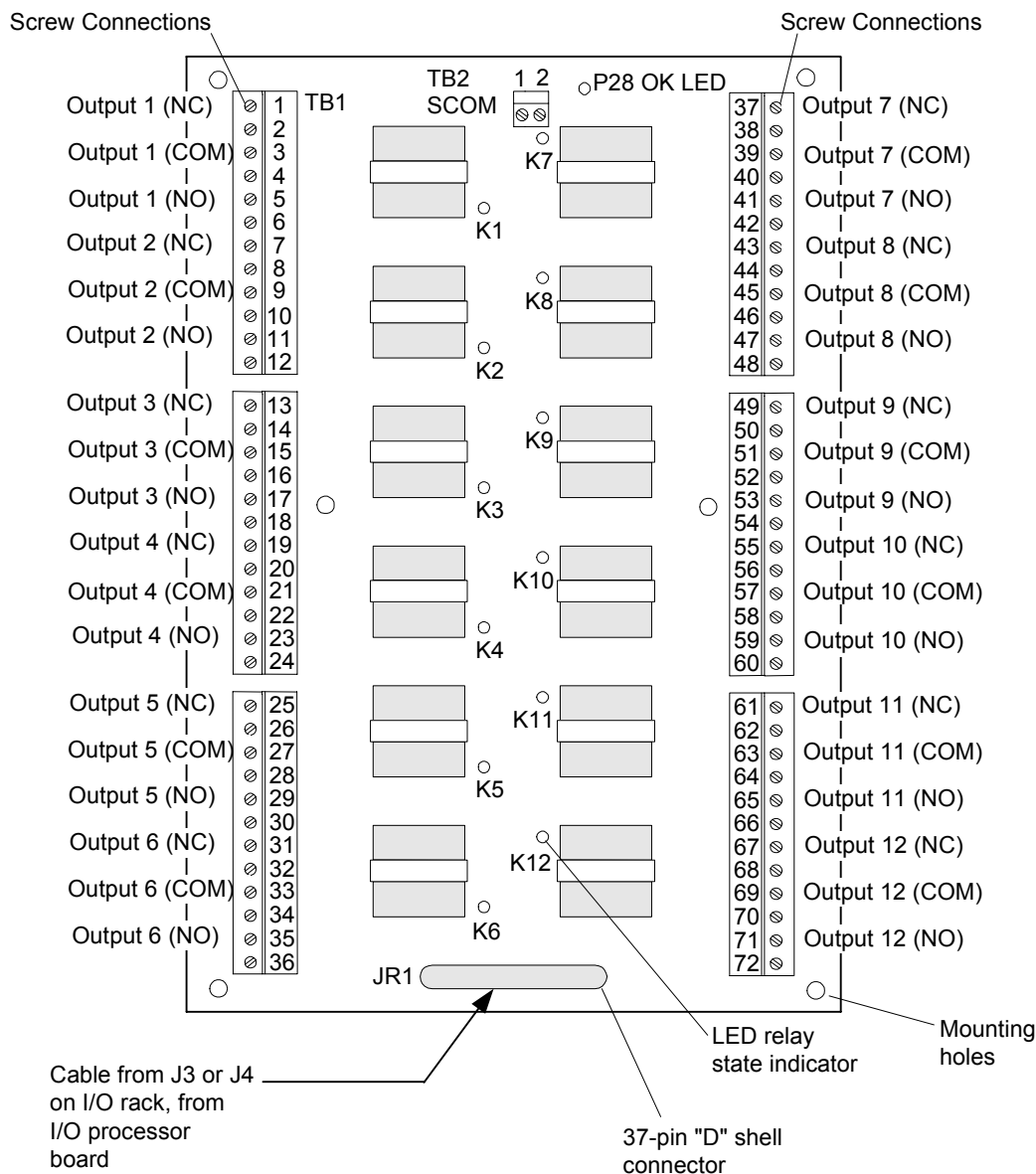
Note DRLY does not work with the PDOA I/O Pack.

Installation

Note DLRV does not have a shield terminal strip.

Mount the DRLV board by fastening screws to wall through the four mounting holes in the corners of metal support plate. Connect the wires for the 12 relay outputs directly to the odd-numbered screws on the terminal blocks. The high-density Euro-Block type terminal blocks plug into the numbered receptacles on the board. The two screws on TB2 are provided for the SCOM (chassis ground) connection, which should be as short a distance as possible.

Note SCOM, TB2, must be connected to chassis ground.

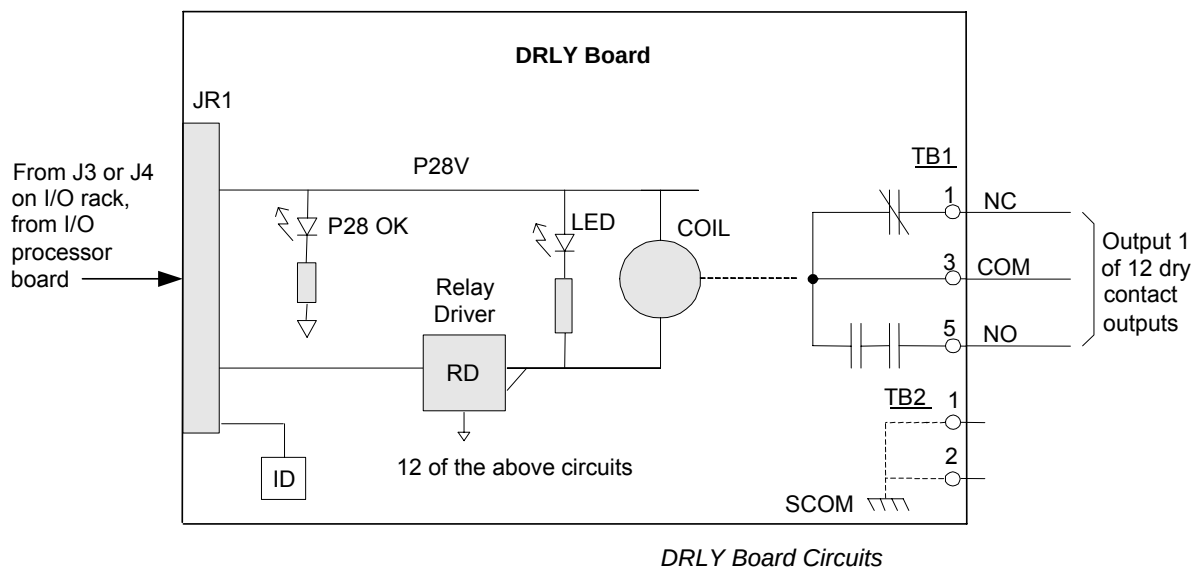


DRLV Wiring and Cabling

Operation

DRLY does not include solenoid source power. There is one set of dry contacts per relay, with two NO contacts in series. Unlike TRLY, there is no on-board suppression, and no relay state monitoring. The I/O board (VCCC, VCRC, or VTUR) provides the 28 V dc power for the relay coils, which is indicated with a green LED. DRLY has a yellow LED for each relay that indicates voltage across the coil. With an unconnected control cable, the relays default to a de-energized state.

Note Three relays on DRLY can be controlled by VTUR using the DTRT transition board. Six relays can be controlled if two DTURs are used.



DRLYH1A Specifications

Item	Specification
Number of relay outputs and type	12 relays, nominal 24 V dc coil. Two-pole double throw with Form C contacts containing two NO and 2 NC contacts
Relay contact rating	Resistive: Inductive: 28 V dc: 10 A 28 V dc: 2 A, L/R = 7 ms, without suppression 120 V ac: 10 A 120 V ac: 2 A, PF= 0.4, 10 A inrush, no suppression Motor load 1/3 Hp. 240 V ac: 3 A 240 V ac: 2 A, PF= 0.4, 10 A inrush, no suppression Motor load 1/2 Hp. 125 V dc: 0.5 A 125 V dc: 0.2 A, L/R = 7 ms without suppression 125 V dc: 0.65 A, L/R = 150 ms, MOV suppression by others (with two contacts in series on the same relay)
Suppression	External suppression will be supplied by customer
Relay response time	Operate: 15 ms typical Release: 10 ms typical
Fault detection in I/O board	The state of the P28 V dc is monitored using a green LED at the top of the board. Voltage across each relay coil is indicated with a yellow LED. There is no relay state monitoring in the VCCC or VCRC
Physical	
Size	21.59 cm long x 20.57 cm wide (8.5 in x 8.1 in wide)
Temperature	0 to 60°C (32 to 140 °F)

DRLYH1B Specifications

Item	Specification
Number of relay outputs	12 relays, nominal 24 V dc coil
Relay type	Two-pole double throw with Form C contacts containing two NO and 2 NC contacts. UL listed, CSA certified, sealed to UL 1604
Relay contact rating (resistive load)	28 V dc: 2 A Max operating voltage: 250 V rms, 220 V dc 125 V dc: 0.5 A Max operating current: 2 A dc, 1 A rms 120 V ac: 1 A Max switching capacity: 125 VA, 60 W 240 V ac: 0.5 A
Suppression	External suppression will be supplied by customer
Relay response time	Operate: 3 ms typical Release: 2 ms typical
Fault detection in I/O board	The state of the P28 V dc is monitored using a green LED at the top of the board Voltage across each relay coil is indicated with a yellow LED There is no relay state monitoring in the I/O board
Agency requirements	UL listed Class I, Division. 2 applications, CSA, and CE, also approvals listed in table above for TRLYH1A
Physical	
Size	21.59 cm long x 20.57 cm wide, (8.5 in x 8.1 in)
Temperature	0 to 75°C (32 to 167 °F)

Diagnostics

The board contains the following diagnostics; there is no relay state monitoring.

- The terminal board connector has an ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. When this chip is read by VCCC/VCRC or VTUR and a mismatch is encountered, a hardware incompatibility fault is created.
- The voltage across each relay coil is indicated with a yellow LED.
- The 28 V supply to the board is indicated with a green LED.

Configuration

There are no jumpers or hardware settings on the board.

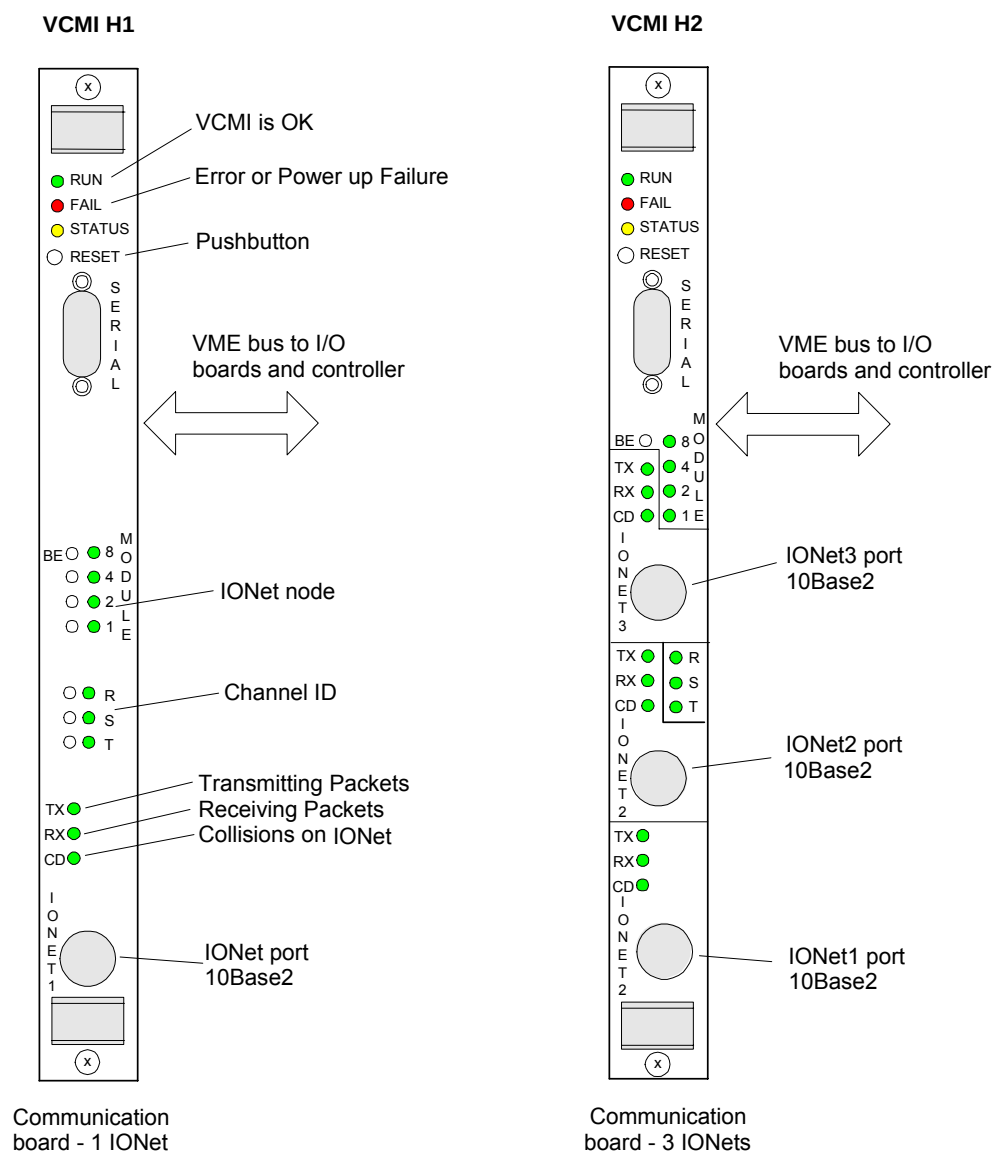
Notes

VCMI Bus Master Controller

VCMI Bus Master Controller

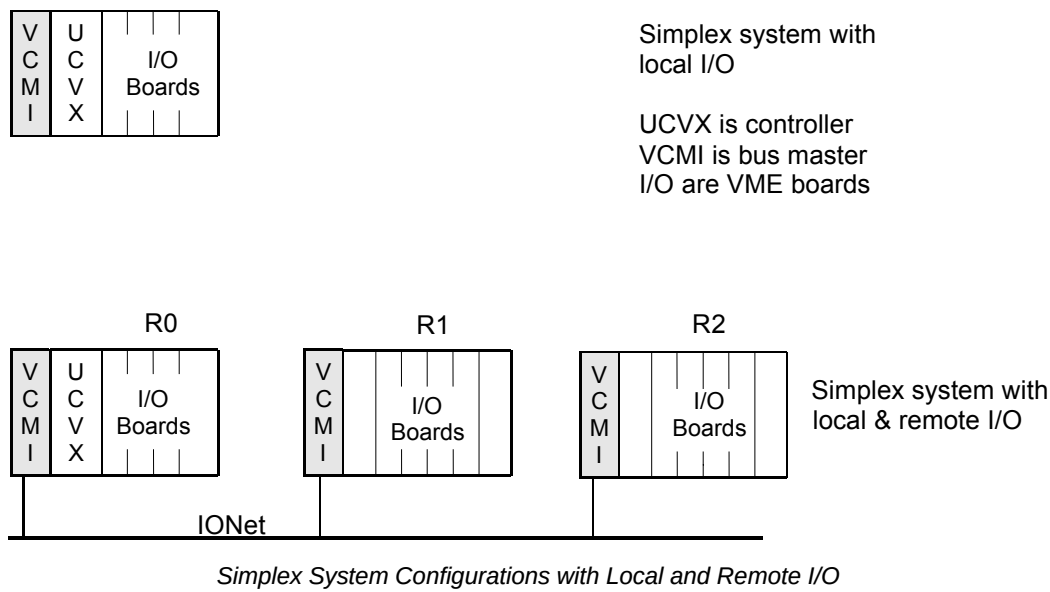
Functional Description

The VME Bus Master Controller (VCMI) board is the communication interface between the controller and the I/O boards, and the communication interface to the system control network, known as IONet. VCMI is also the VME bus master in the control and I/O racks, and manages the IDs for all the boards in the rack and their associated terminal boards. The two versions of the VCMI are shown in the following figure:



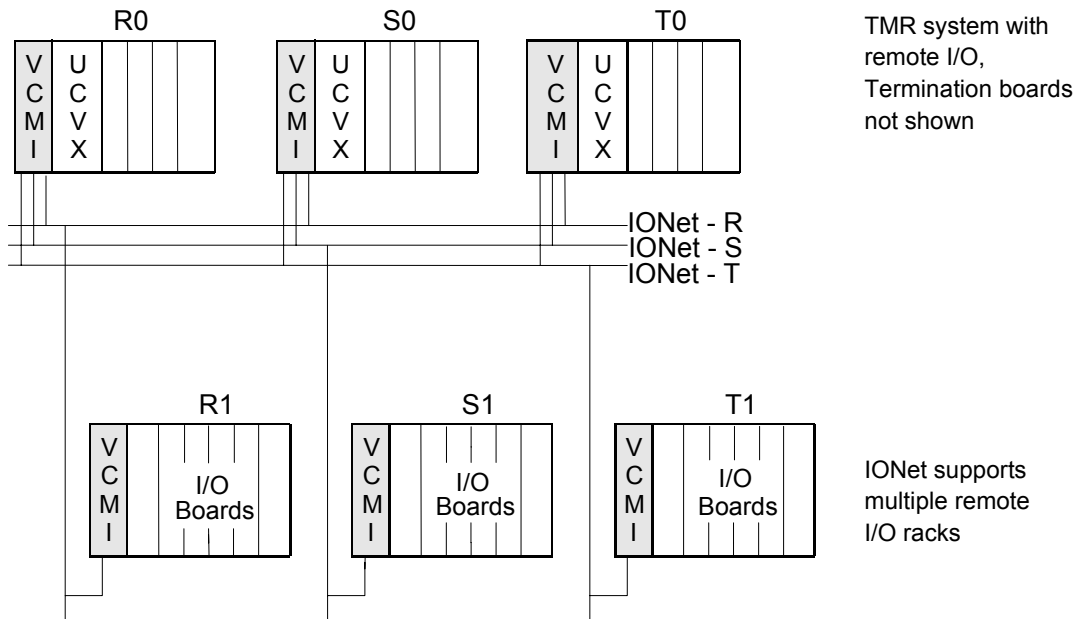
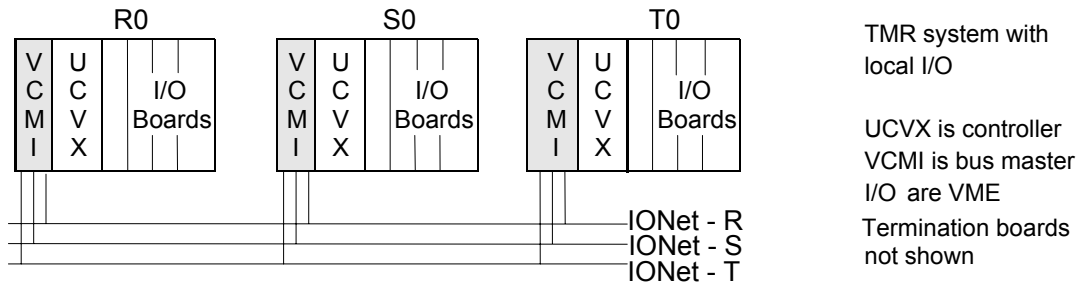
VCMI Boards, Single, and Triple Network Versions

Multiple I/O racks can be connected to the IONet, each rack with its own VCMI board. The following figure shows three simplex system configurations with local and remote I/O using the VCMI.



The following figure shows two sizes of triple modular redundant (TMR) systems. The first example is a small system where all the I/O is mounted in the VME control rack so no remote I/O racks are required. Each channel (R, S, T) has its own IONet, and the VCMI has three IONet ports.

The second example is a larger system with remote I/O racks. Each IONet supports multiple I/O racks, but only one rack is shown here. All I/O channels (R, S, T) are identical in terms of I/O boards and points.



TMR System Configurations with Local and Remote I/O

The VCMC card receives analog and digital feedback of power status through the J301 backplane connector. J301 connections are as follows:

Backplane		VCMC Hardware		VCMC Software	
J301 Pin	Signal	VCMC Signal	Description	Signal Space	Signal Space Description
1	P28AA		+28 V Power out		
2	PCOM		Power common		
5	SG201C28	AIN4P	Analog input 4 +	Spare 02	Analog spare 02
6	SG201C27	AIN4N	Analog input 4 -	Spare 01	Analog spare 01
7	SG201C26	AIN3P	Analog input 3 +		
8	SG201C25	AIN3N	Analog input 3 -		
9	SG201C24	DINRET	Digital input Power common		
10	SG201C23	DINPWROUT	Digital input Power output		
11	SG201C22	DIN12	Digital input 12	Logic_In_12	Spare 05
12	SG201C21	DIN11	Digital input 11	Logic_In_11	Spare 04
13	SG201C20	DIN10	Digital input 10	Logic_In_10	Spare 03
14	SG201C19	DIN9	Digital input 9	Logic_In_9	Spare 02
15	SG201C18	DIN8	Digital input 8	Logic_In_8	Spare 01
16	SG201C17	DIN7	Digital input 7	Logic_In_7	Fuse 29, J17 Fault
17	PCOM		Power common		
18	P28AA		+28 V Power out		
19	SIGCOM02		SCOM-DCOM JP2 Select		
20	N28		-28 V Power out		
21	PCOM		Power common		
26	SG201A26	AIN2P	Analog input 2 +	N125_Grd	N125 with respect to ground
27	SG201A25	AIN2N	Analog input 2 -		
28	SG201A24	AIN1P	Analog input 1 +	P125_Grd	P125 with respect to ground
29	SG201A23	AIN1N	Analog input 1 -		
30	SG201A22	DIN6	Digital input 6	Logic_In_6	Fuse 32, J20 Fault
31	SG201A21	DIN5	Digital input 5	Logic_In_5	Fuse 31, J19 Fault
32	SG201A20	DIN4	Digital input 4	Logic_In_4	Miscellaneous contact
33	SG201A19	DIN3	Digital input 3	Logic_In_3	AC2 source fault
34	SG201A18	DIN2	Digital input 2	Logic_In_2	AC1 source fault
35	SG201A17	DIN1	Digital input 1	Logic_In_1	Battery bus fault
36	SIGCOM01		SCOM-DCOM JP1 Select		
37	CBL301ID	CBL301ID	ID Cable signal		

Specifications

Item	Specification
Board Type	6U high VME board, 0.787 inch wide
Processor	Texas Instruments TMS320C32 32-bit digital signal processor
Memory	Dual-port memory, 32 Kbytes in 32-bit transfer configuration SRAM, 256k x 32 Flash memory, 512k x 8-VCMIH_B; 4096K x 8-VCMIH_C
Communication	H1 version: One IONet 10Base2 Ethernet port, BNC connector, 10 Mbps/sec H2 version: Three IONet 10Base2 Ethernet ports, BNC connectors, 10 Mbps/sec VME bus block transfers 1 RS-232C Serial port, D-style plug connector, 9600 (only)
Frame Rate	10 ms (100 Hz) for simplex 40 ms (25 Hz) for TMR 20 ms, 80 ms application dependent

Diagnostics

The internal +5 V, ± 12 V, ± 15 V, and ± 28 V power supply buses are monitored and alarmed. The alarm settings are configurable and usually set at 3.5%, except for the 28 V supplies, which are set at 5.5%.

Diagnostic signals from the power distribution module (PDM), connected through J301, are also monitored. These include ground fault and over/under voltage on the P125 V bus, two differential ± 5 V dc analog inputs, P28A and PCOM for external monitor circuits, and digital inputs.

Configuration

VCMI Toolbox Configuration (Part 1 of 2)

Parameter	Description	Choices
Configuration		
System Limits	Enable or disable all system limits	Enable, disable
PS_Limit1	$\pm$ Power supply limits for P5, P15, N15 in %	0 to 10
PS_Limit2	$\pm$ Power supply limits for P12, N12, P28, N28 in percent	0 to 10
PwrBusLimits	Enable or disable power bus diagnostics	Enable, disable
125 vBusHlim	High limit for 125 V dc bus in volts	0 to 150
125 vBusLlim	Low limit for 125 V dc bus in volts	0 to 150
125 vBusGlim	Low volts to ground limit for 125 V dc bus (diagnostic)	0 to 150
J3 Power Monitor	PDM monitor	Connected, not connected
Logic_In_1	First of 12 logical inputs – board point signal	Point edit (input BIT)
Logic_In	Configurable item	Used, unused
P125_Grd	P125 with respect to ground – board point signal	Point Edit (Input FLOAT)
Input_Type	Type of analog input	Used, unused
Low_Input	Input volts at low value	-10 to +10
Low_Value	Input value in engineering units at low MA	-3.4082e+038 to 3.4028e+038

Parameter	Description	Choices
High_Input	Input volts at high value	-10 to +10
High_Value	Input value in engineering units at high MA	-3.4082e+038 to 3.4028e+038
Input_Filter	Bandwidth of input signal filter in Hz	Unused, 0.75 Hz, 1.5 Hz, 3 Hz,
TMR_DiffLimit	Difference limit for voted TMR inputs in % of high-low values	0 to 10
Sys_Lim_1_Enabl	Enable system limit 1 fault check	Enable, disable
Sys_Lim_1_Latch	Input fault latch	Latch, unlatch
Sys_Lim_1_Type	Input fault type	Greater than or equal Less than or equal
Sys_Lim_1	Input limit in engineering units	-3.4082e+038 to 3.4028e+038
Sys_Lim_2	Same as above for Sys Lim 1	Same as for Sys_Lim_1
N125_Gnd	Same as for P125_Grd – board point signal	Same as for P125_Grd
Spare 01	Similar to P125_Grd – board point signal	Similar to P125_Grd
Spare 02	Similar to P125_Grd – board point signal	Similar to P125_Grd

VCMI Toolbox Configuration (Part 2 of 2)

Parameter	Description	Choices	
Board Point Signal	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3Diag_VCM11	Board diagnostic	Input	BIT
L3Diag_VCM12	Board diagnostic	Input	BIT
L3Diag_VCM13	Board diagnostic	Input	BIT
SysLimit1-1	P125_Grd (Input exceeds limit)	Input	BIT
SysLimit1-2	N125_Grd (Input exceeds limit)	Input	BIT
SysLimit1-3	Spare 01 (Input exceeds limit)	Input	BIT
SysLimit1-4	Spare 02 (Input exceeds limit)	Input	BIT
SysLimit1_125	P125 bus out of limits (Input exceeds limit)	Input	BIT
SysLimit2-1	P125_Grd (Input exceeds limit)	Input	BIT
SysLimit2-2	N125_Grd (Input exceeds limit)	Input	BIT
SysLimit2-3	Spare 01 (Input exceeds limit)	Input	BIT
SysLimit2-4	Spare 02 (Input exceeds limit)	Input	BIT
SysLimit2_125	P125 bus out of limits (Input exceeds limit)	Input	BIT
P125Bus	Calc 125 V dc bus voltage (P125Grd - N125Grd)	Input	FLOAT
ResetSYS	System limit reset (Special VCMI output to I/O bds)	Output	BIT
ResetDIA	Diagnostic reset (Special VCMI output to I/O bds)	Output	BIT
ResetSuicide	Suicide reset (Special VCMI output to I/O bds)	Output	BIT
MasterReset	Master reset L86MR (Special VCMI out to I/O bds)	Output	BIT
Logic_In_1	Battery bus fault	Input	BIT
Logic_In_2	AC1 source fault	Input	BIT
Logic_In_3	AC2 source fault	Input	BIT
Logic_In_4	Misc contact	Input	BIT
Logic_In_5	Fuse 31, J19 fault	Input	BIT
Logic_In_6	Fuse 32, J20 fault	Input	BIT
Logic_In_7	Fuse 29, J17 fault	Input	BIT
Logic_In_8	Spare 01	Input	BIT
Logic_In_9	Spare 02	Input	BIT
Logic_In_10	Spare 03	Input	BIT
Logic_In_11	Spare 04	Input	BIT
Logic_In_12	Spare 05	Input	BIT
P125_Grd	P125 with respect to ground, P3 – 28 to 29	Input	FLOAT

Parameter	Description	Choices	
N125_Grd	N125 with respect to ground, negative number, P3 – 26 to 27	Input	FLOAT
Spare01	Analog spare 01, P3 – 07 to 08	Input	FLOAT
Spare02	Analog spare 02, P3 – 05 to 06	Input	FLOAT

Alarms

Fault	Fault Description	Possible Cause
1	SOE Overrun. Sequence of Events data overrun	Communication problem on IONet
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC Failure Override is Active	Board firmware programming error (board is allowed to go online)
4	Watchdog circuitry is not armed	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
25	Board inputs disagree with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
30	ConfigCompatCode mismatch; Firmware: #, Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32	P5=####.## Volts is Outside of Limits. The P5 power supply is out of the specified operating limits	A VME rack backplane wiring problem and/or power supply problem
33	P15=####.## Volts is Outside of Limits. The P15 power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a back plane wiring or VME power supply problem.
34	N15=####.## Volts is Outside of Limits. The N15 power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem.
35	P12=####.## Volts is Outside of Limits. The P12 power supply is out of the specified operating limits	If "Remote I/O", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem.
36	N12=####.## Volts is Outside of Limits. The N12 power supply is out of the specified operating limits	If "Remote I/O", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem.
37	P28A=####.## Volts is Outside of Limits. The P28A power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem.
38	P28B=####.## Volts is Outside of Limits. The P28B power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem.

Fault	Fault Description	Possible Cause
39	P28C=####.## Volts is Outside of Limits. The P28C power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem.
40	P28D=####.## Volts is Outside of Limits. The P28D power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem.
41	P28E=####.## Volts is Outside of Limits. The P28E power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem.
42	N28=####.## Volts is Outside of Limits. The N28 power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem.
43	125 Volt Bus=####.## Volts is Outside of Limits. The 125-Volt bus voltage is out of the specified operating limits	A source voltage or cabling problem; disable 125 V monitoring if not applicable.
44	125 Volt Bus Ground =####.## Volts is Outside of Limits. The 125-Volt bus voltage ground is out of the specified operating limits	Leakage or a fault to ground causing an unbalance on the 125 V bus; disable 125 V monitoring if not applicable.
45	IONet-1 Communications Failure. Loss of communication on IONet1	Loose cable, rack power, or VCMI problem
46	IONet-2 Communications Failure. Loss of communication on IONet2	Loose cable, rack power, or VCMI problem
47	IONet-3 Communications Failure. Loss of communication on IONet3	Loose cable, rack power, or VCMI problem
48	VME Bus Error Detected (Total of #### Errors). The VCMI has detected errors on the VME bus	The sum of errors 60 through 66 - Contact the factory.
49	Using Default Input Data, Rack R.#. The VCMI is not getting data from the specified rack	IONet communications failure - Check the VCMI and/or IONet cables.
50	Using Default Input Data, Rack S.#. The VCMI is not getting data from the specified rack	IONet communications failure - Check the VCMI and/or IONet cables.
51	Using Default Input Data, Rack T.#. The VCMI is not getting data from the specified rack	IONet communications failure - Check the VCMI and/or IONet cables.
52	Missed Time Match Interrupt (## uSec). The VCMI has detected a missed interrupt	Possible VCMI hardware failure
53	VCMI Scheduler Task Overrun. The VCMI did not complete running all its code before the end of the frame	Possibly too many I/O
54	Auto Slot ID Failure (Perm. VME Interrupt). The VCMI cannot perform its AUTOSLOT ID function	I/O board or backplane problem
55	Card ID/Auto Slot ID Mismatch. The VCMI cannot read the identity of a card that it has found in the rack	Board ID chip failed
56	Topology File/Board ID Mismatch. The VCMI has detected a mismatch between the configuration file and what it actually detects in the rack	ID chip mismatch - Check your configuration
57	Controller Sequencing Overrun	Too much application code used in controller. Reduce the code size.
58	Controller PCODE Version Mismatch between R,S,and T. R, S, and T have different software versions	Error during controller download - revalidate, build, and download all 3 controllers.
59	IONet Communications Failure. Loss of communications on the slave VCMI IONet	Loose cable, rack power, or VCMI problem (VCMI slave only)
60-66	VME Error Bit # (Total ## Errors). The VCMI has detected errors on the VME bus	VME backplane errors - Contact factory.
67	Controller Board is Offline. The VCMI cannot communicate with the controller	Controller failed or is powered down.
68-87	I/O Board in Slot # is Offline. The VCMI cannot communicate with the specified board	I/O board is failed or removed. You must replace the board, or reconfigure the system and redownload to the VCMI, and reboot.

Fault	Fault Description	Possible Cause
88	U17 Sectors 0-5 are not write protected	Sectors not write protected in manufacturing. Contact the factory.
89	SRAM resources exceeded. Topology/config too large	The size of the configured system is too large for the VCMI. You must reduce the size of the system.
90	U54 Flashsectors ### not write protected	Sectors not write protected in manufacturing. Contact the factory

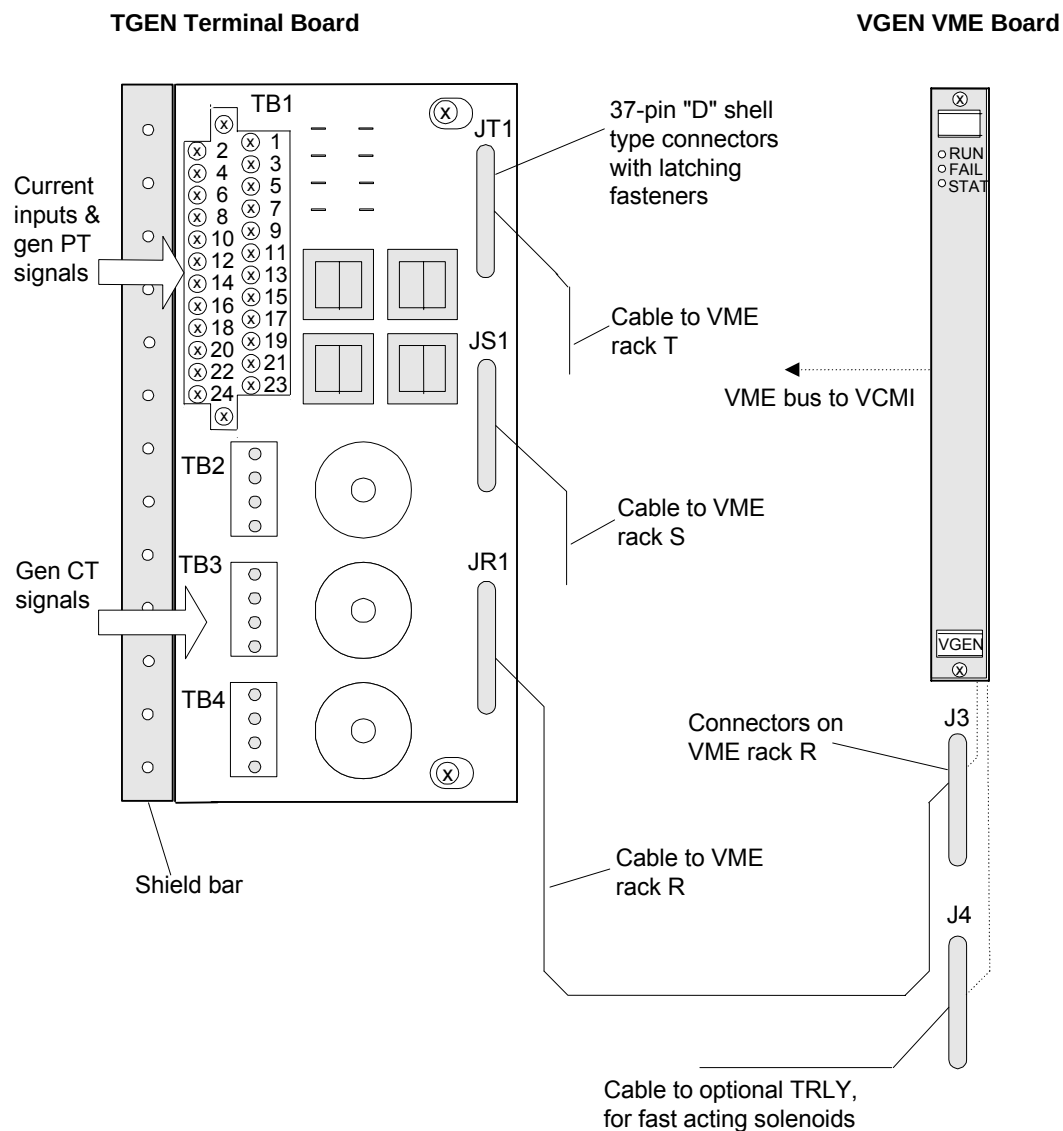
Notes

VGEN Generator Monitor and Trip

VGEN Generator Monitor and Trip

Functional Description

The Generator Monitor and Trip (VGEN) board and the TGEN terminal board monitor the generator three-phase voltage and currents, and calculate three-phase power and power factor. For large steam turbine applications, VGEN provides the power load unbalance (PLU) and early valve actuation (EVA) functions, using fast acting solenoids located on a TRLY terminal board.



Generator Terminal Board, Processor Board, and Cabling

Installation

➤ To install the VGEN board

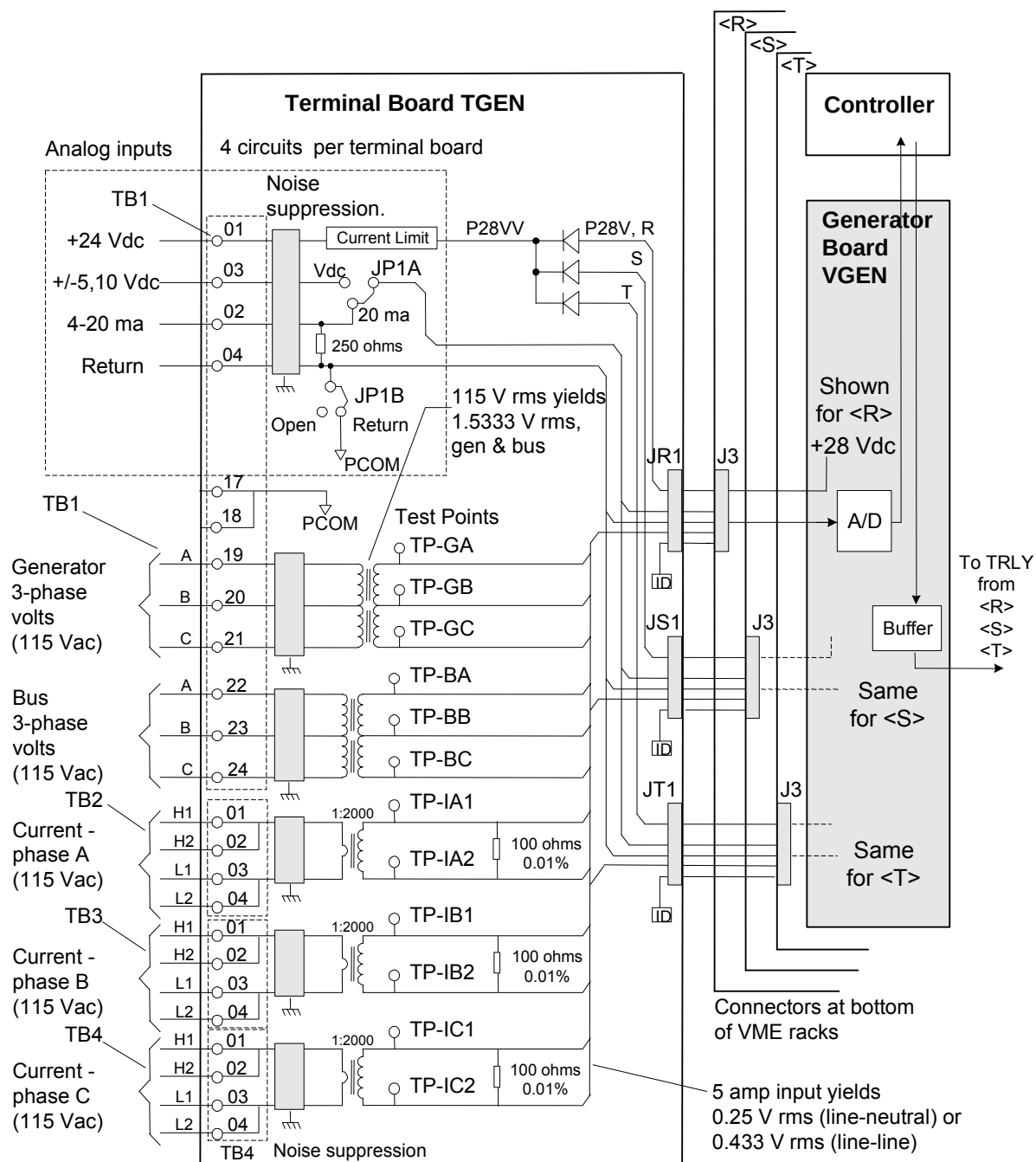
- 1** Power down the VME I/O processor rack.
- 2** Slide in the VGEN board and push the top and bottom levers in with your hands to seat its edge connectors.
- 3** Tighten the captive screws at the top and bottom of the front panel. These screws serve to hold the board firmly in place and enhance the board front ground integrity. The screws should not be used to actually seat the board.

Note Cable connection to the TGEN terminal board is made at the J3 connector on the lower portion of the VME rack. Cable connection to the optional TRLY terminal board is made at the J4 connector on the lower portion of the VME rack. J3 and J4 are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the *Diagnostics* section in this document.

Operation

VGEN monitors two, three-phase potential transformer (PT) inputs, and three, one-phase current transformer (CT) inputs. Using jumpers on TGEN, four analog inputs can be configured for 4-20 mA or ± 5 , ± 10 V dc. VGEN performs signal conversions and power, power factor, and frequency calculations.

Note A single VGEN can be used for simplex operation, or three VGENs can be used for TMR operation.



TGEN Board Showing Potential and Current Transformer Inputs

VGEN monitors generator three-phase power and supplies the PLU and EVA functions for large steam turbines. The generator and bus PT inputs are three-wire, open delta, voltage measurements that are used to calculate all three line-to-line voltages. They are not used for automatic synchronizing, which requires two separate single-phase PT inputs. Each PT input is magnetically isolated and is nominally 115 V rms.

Note Test points are provided for all PT and CT inputs to verify the phase in the field.

Three single-phase CT inputs are provided with a normal current range of 0 to 5 A continuous. The CTs are magnetically isolated on TGEN. CTs connect to non-pluggable terminal blocks with captive lugs accepting up to #10 AWG wires. The following parameters are calculated from these inputs:

- Total Mwatts
- Total Mvars
- Total MVA
- Power factor
- Bus frequency (5 to 66 Hz)

Note High frequency and 50/60 Hz noise is reduced with an analog hardware filter.

The four analog inputs accept 4-20 mA inputs or ± 5 , ± 10 V dc inputs. A +24 V dc source is available for all four circuits with individual current limits for each circuit. The 4-20 mA transducer can use the +24 V dc source from the turbine control or a self-powered source. A jumper on TGEN selects between current and voltage inputs for each circuit.

Specifications

Item	Specification
Inputs to TGEN and VGEN	2 three-phase generator and bus PTs 3 one-phase generator CTs 4 analog inputs (4-20 mA, ± 5 , ± 10 V dc)
Outputs from VGEN through TRLY	12 relay outputs (for large steam turbines)
Generator and bus voltages	Nominal 115 V rms with range of interest of 10 to 120% Nominal frequency 50/60 Hz with range of interest 45 to 66 Hz Magnetic isolation to 1,500 V rms and loading less than 3 VA Input measurement resolution is 0.1% Input accuracy is 0.5% of rated V rms from 45 to 66 Hz Input accuracy is 1.0% of rated V rms from 25 to 45 Hz Input loading less than 3 VA per circuit
Generator current inputs	Normal current range is 0 to 5 A with over-range to 10 A Nominal frequency 50/60 Hz with range of interest 45 to 66 Hz Magnetic isolation to 1,500 V rms Input accuracy 0.5% of full scale (5 A) with resolution of 0.1% FS Input burden less than 0.5 Ω per circuit

Item	Specification
Analog inputs	Current inputs: 4-20 mA Voltage inputs: ± 5 V dc or ± 10 V dc Transducers can be up to 300 m (984 ft) from the control cabinet with a two-way cable resistance of 15 Ω . Input burden resistor on TGEN is 250 Ω . Jumper selection of single ended or self powered inputs Jumper selection of voltage or current inputs Analog Input Filter: Breaks at 72 and 500 rad/sec Ac common mode rejection (CMR) 60 dB Dc common mode rejection (CMR) 80 dB
Conversion accuracy	Sampling type 16-bit A/D converter, 14 bit resolution Accuracy 0.1% overall
Frame rate	100 Hz
Calculated values	Total MW and MV have an accuracy of 1% FS, and 0.5% for totalizing. Total m VA and power factor have an accuracy of 1% full scale. Bus frequency (5 to 66 Hz) has an accuracy of $\pm 0.1\%$.

Diagnostics

Three LEDs at the top of the VGEN front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED shows STATUS and is normally off but displays a steady orange if a diagnostic alarm condition exists in the board.

Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check. The software limit check is adjustable in the field. Open wire detection is provided for voltage inputs, and relay drivers and coil currents are monitored.

Connectors JR1, JS1, and JT1, on TGEN have their own ID device that is interrogated by VGEN. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location.

Configuration

Parameter	Description	Choices
Configuration		
PLU_Enab	Enable PLU function	Enable, disable
PLU_Del_Enab	Enable PLU delay	Enable, disable
MechPwrInput	Mech. power through TMR (first 3 MA ccts), dual xducer (Max), single xducer, or signal space	TMR_1 through 3, dual 1 and 2, SMX_1, SMX_2, signal space
PLU_Rate	Select PLU threshold rate	37.5
PLU_Unbal	PLU Unbalance threshold %	20 to 80
PLU_Delay	PLU delay, secs	0.5
Press Ratg	Reheat press equiv. to 100% mechanical power	50 to 600
Current Ratg	Generator current equivalent to 100% electrical power	1,000 to 60,000
EVA_Enab	Enable EVA function	Enable, disable
EVA_ExtEnab	Enable external EVA function	Enable, disable
EVA_Rate	Select EVA threshold rate	LO, ME, HI
EVA_Unbal	EVA unbalance threshold %	20 to 80
EVA_Delay	EVA drop out time, seconds	0 to 10

Parameter	Description	Choices
MW_Ratg	Generator MW equivalent to 100 % electrical power	10 to 1,500
IVT_Enab	Enable IVT function	Enable, disable
Min_MA_Input	Minimum MA for healthy 4-20 mA input	0 to 21
MAx_MA_Input	Maximum MA for healthy 4-20 mA input	0 to 21
SystemFreq	System frequency in Hz	50 or 60
J3:IS200TGENH1A		Connected, Not Connected
AnalogIn1	First analog input (of four) - board point	Point edit (input FLOAT)
Input type	Type of analog input	Unused, 4-20 ma, ± 5 V, ± 10 V
Low input	Input MA at low value	-10 to 20
Low value	Input value in engineering units at low MA (configuration inputs the same as for TBAI)	-3.4028e+038 to 3.4028e+038
System limits	Standard System Limits (see TBAI configuration)	
GenPT_Vab_KV	Generator potential transformer input "ab", (first of 3) board point	Point edit (input FLOAT)
PT_Input	PT input in KV rms for PT_output	1 to 1,000
PT_Output	PT output in V rms for PT_Input-typically 115	60 to 150
Phase Shift	Compensating phase shift, applied to PT signals	Zero, plus 30, plus 60, minus 30, minus 60
System limits	Standard system limits (similar to analog Inputs)	
BusPT_Vab_KV	Bus potential transformer input "ab", (first of three) configuration similar to GenPT - board point	Point edit (input FLOAT)
GenCT_A	Generator current transformer A (first of three) - board point	Point edit (input FLOAT)
CT_Input	CT input in amperes rms for rated CT_Output	100 to 50,000
CT_Output	Rated CT output in amperes rms, typically 5	1 to 5
System Limits	Standard system limits (similar to genPT)	
J4:IS200TRLHY1A		Connected, not connected
Relay01_Tst	Fast acting solenoid #1 test, first of 12 relays - board point	Point edit (output BIT)
Relay Output	FAS valve type	Unused, CV, tst only, CV EVA
RelayDropTime	Relay dropout time	0 to 5

Board Points Signals	Description – Point Edit (Enter Signal Name)	Direction	Type
L3DIAG_VGEN1	Board diagnostic	Input	BIT
L3DIAG_VGEN2	Board diagnostic	Input	BIT
L3DIAG_VGEN3	Board diagnostic	Input	BIT
SysLim1Anal1	System limit 1 exceeded on analog cct #1	Input	BIT
:	:	Input	BIT
SysLim1Anal4	System limit 1 exceeded on Analog cct #4	Input	BIT
SysLim2Anal1	System limit 2 exceeded on Analog cct #1	Input	BIT
:	:	Input	BIT
SysLim2Anal4	System limit 2 exceeded on analog cct #4	Input	BIT
SysL1GenPTab	System limit 1 exceeded on gen PT, Vab	Input	BIT
SysL1GenPTbc	System limit 1 exceeded on gen PT, Vbc	Input	BIT
SysL1GenPTca	System limit 1 exceeded on gen PT, Vca	Input	BIT
SysL1BusPTab	System limit 1 exceeded on bus PT, Vab	Input	BIT
SysL1BusPTbc	System limit 1 exceeded on bus PT, Vbc	Input	BIT
SysL1BusPTca	System limit 1 exceeded on bus PT, Vca	Input	BIT
SysL2GenPTab	System limit 2 exceeded on gen PT, Vab	Input	BIT

Board Points Signals	Description – Point Edit (Enter Signal Name)	Direction	Type
SysL2GenPTbc	System limit 2 exceeded on gen PT, Vbc	Input	BIT
SysL2GenPTca	System limit 2 exceeded on gen PT, Vca	Input	BIT
SysL2BusPTab	System limit 2 exceeded on bus PT, Vab	Input	BIT
SysL2BusPTbc	System limit 2 exceeded on bus PT, Vbc	Input	BIT
SysL2BusPTca	System limit 2 exceeded on bus PT, Vca	Input	BIT
SysL1GenCTa	System limit 1 exceeded on gen CT, phase A	Input	BIT
SysL1GenCTb	System limit 1 exceeded on gen CT, phase B	Input	BIT
SysL1GenCTc	System limit 1 exceeded on gen CT, phase C	Input	BIT
SysL2GenCTa	System limit 2 exceeded on gen CT, phase A	Input	BIT
SysL2GenCTb	System limit 2 exceeded on gen CT, phase B	Input	BIT
SysL2GenCTc	System limit 2 exceeded on gen CT, phase C	Input	BIT
Relay01_Fdbk	Status of relay 01	Input	BIT
:	:	Input	BIT
Relay12_Fdbk	Status of relay 12	Input	BIT
L10PLU_EVT	Power load unbalance event	Input	BIT
L10EVA_EVA	Early valve actuation event	Input	BIT
GenMW	Generator MWatts	Input	FLOAT
GenMVAR	Generator MVars	Input	FLOAT
GenMVA	Generator MVA	Input	FLOAT
GenPF	Generator power factor, 0/1/0	Input	FLOAT
BusFreq	Bus frequency, Hz	Input	FLOAT
PLU_Tst	Power load unbalance test	Output	BIT
EVA_Tst	Early valve actuation test	Output	BIT
IV_Trgr	Intercept valve trigger command	Output	BIT
EVA_ExtCmd	Early valve actuation external command	Output	BIT
EVA_ExtPrm	Early valve actuation external permissive	Output	BIT
TN_Hz	PLL center frequency, Hz	Output	FLOAT
MechPower	Mechanical power, percent, when configured through signal space	Output	FLOAT
AnalogIn1	Analog input 1	Input	FLOAT
:	:	Input	FLOAT
AnalogIn4	Analog input 4	Input	FLOAT
GenPT_Vab_KV	Kilovolts rms	Input	FLOAT
GenPT_Vbc_KV	Kilovolts rms	Input	FLOAT
GenPT_Vca_KV	Kilovolts rms	Input	FLOAT
BusPT_Vab_KV	Kilovolts rms	Input	FLOAT
BusPT_Vbc_KV	Kilovolts rms	Input	FLOAT
BusPT_Vca_KV	Kilovolts rms	Input	FLOAT
GenCT_A	Generator Amperes RMS, phase A	Input	FLOAT
GenCT_B	Generator amperes rms, phase B, same configuration as phase A	Input	FLOAT
GenCT_C	Generator amperes rms, phase C, same configuration as phase A	Input	FLOAT
Relay01_Tst	Fast acting solenoid #1 test	Output	BIT
:	:	Output	BIT
Relay12_Tst	Fast acting solenoid #12 test	Output	BIT

Alarms

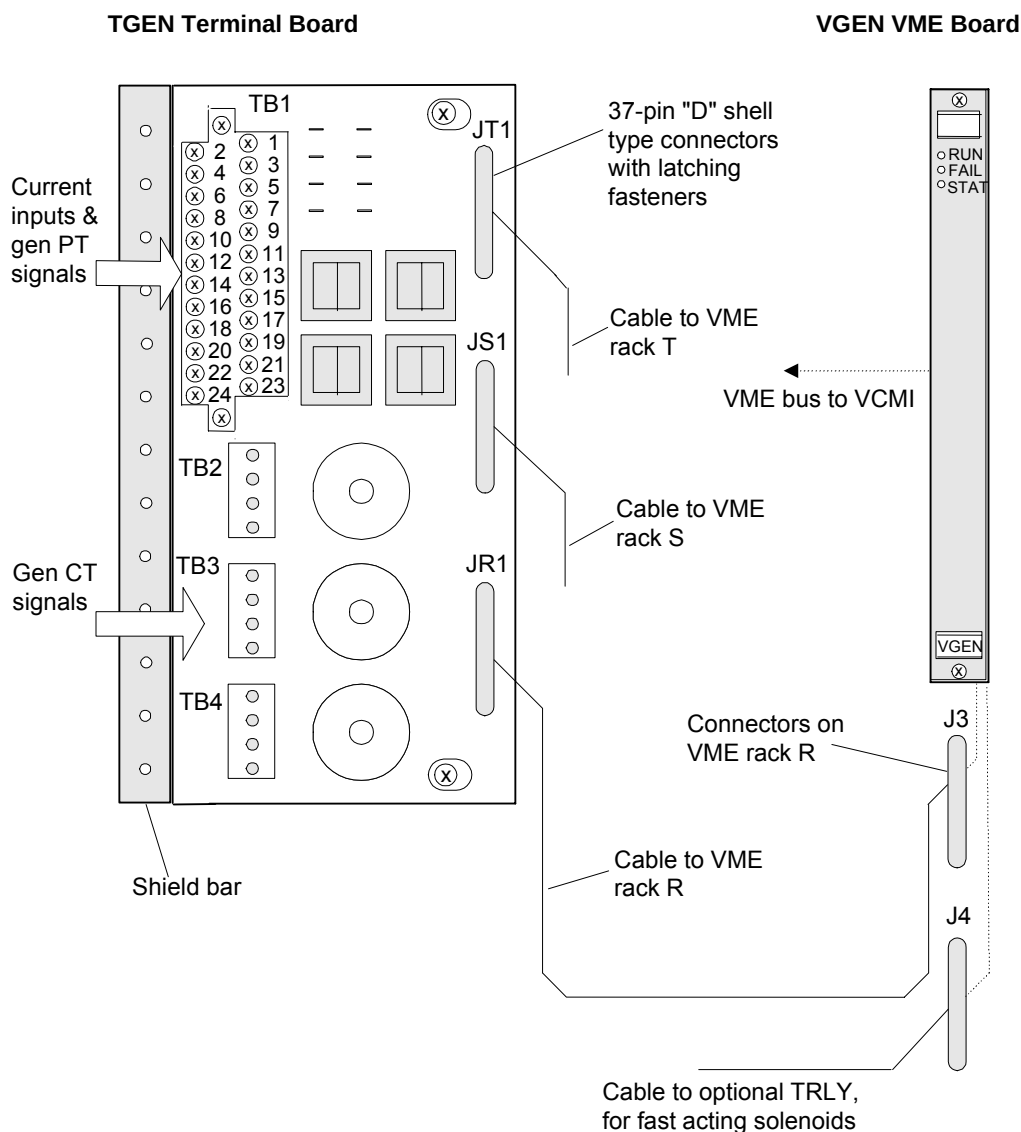
Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32-43	Relay Driver # does not Match Requested State. There is a mismatch between the relay driver command and the state of the output to the relay as sensed by VGEN	The relay terminal board may not exist and the relay is configured a used, or there may be a faulty relay driver circuit or drive sensors on VGEN.
44-55	Relay Output Coil # does not Match Requested State. There is a mismatch between the relay driver command and the state of the current sensed on the relay coil on the relay terminal board	Relay is defective, or the connector cable J4 to the relay terminal board J1 is disconnected, or the relay terminal board does not exist.
56-59	Analog Input # Unhealthy. Analog Input 4-20 mA ## has exceeded the A/D converter's limits	Analog input is too large, TGEN jumper (JP1, JP3, JP5, JP7) is in the wrong position, signal conditioning circuit on TGEN is defective, multiplexer or A/D converter circuit on VGEN is defective.
60-65	Fuse # and/or # Blown. The fuse monitor requires the jumpers to be set and to drive a load, or it will not respond correctly	One or both of the listed fuses is blown, or there is a loss of power on TB3, or the terminal board does not exist, or the jumpers are not set.
66-69	Analog 4-20 mA Auto Calibration Faulty. One of the analog 4-20 mA auto calibration signals has failed. Auto calibration or 4-20 mA inputs are invalid	3 Volt or 9 Volt precision reference or null reference on VGEN is defective, or multiplexer or A/D converter circuit on VGEN is defective.
70-73	PT Auto Calibration Faulty. One of the PT auto calibration signals has gone bad. Auto calibration of PT input signals is invalid, PT inputs are invalid	Precision reference voltage or null reference is defective on VGEN, or multiplexer or A/D converter circuit on VGEN is defective.
74-79	CT Auto Calibration Faulty. One of the CT auto calibration signals has gone bad. Auto calibration of CT input signals is invalid, CT inputs are invalid	Precision reference voltage or null reference is defective on VGEN, or multiplexer or A/D converter circuit on VGEN is defective.
96-223	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
224-241	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TGEN Generator Monitor

Functional Description

The Generator Monitor (TGEN) terminal board works with the VGEN processor to monitor the generator three-phase voltage and currents, and calculate three-phase power and power factor. For large steam turbine applications, VGEN provides the PLU and EVA functions, using fast acting solenoids located on the TRLY terminal board.

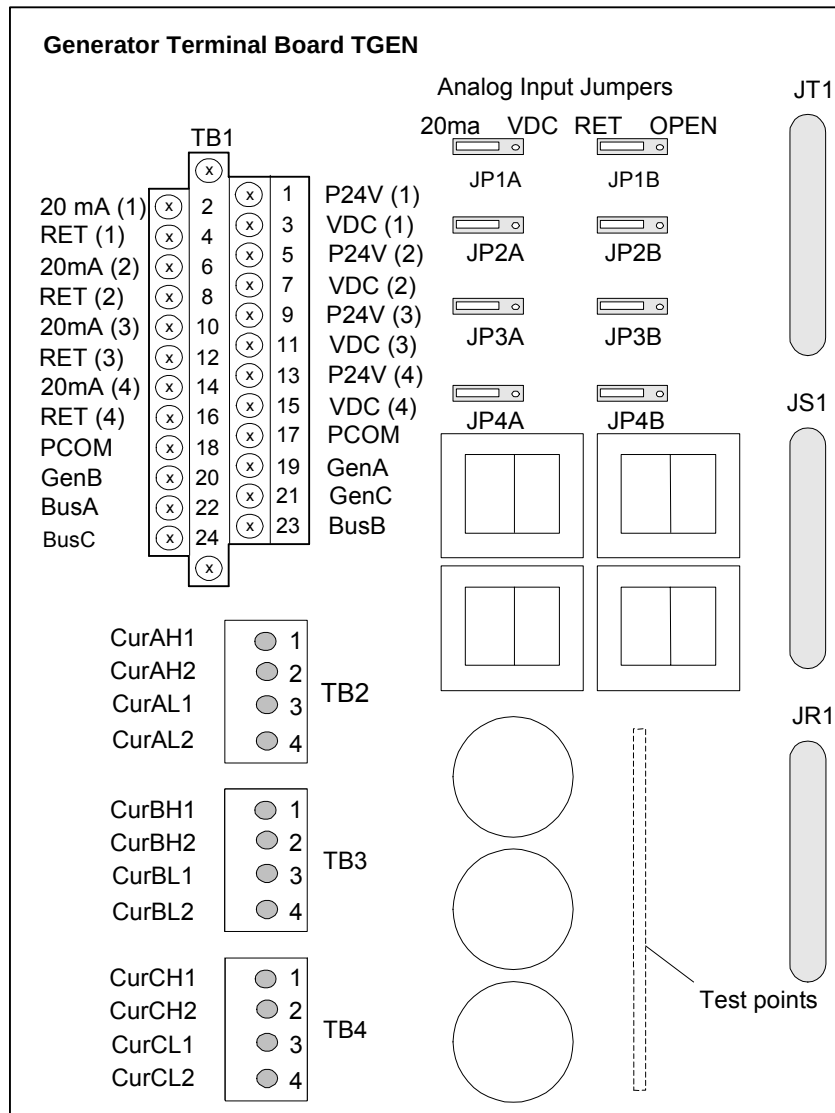
In the Mark* VI system, the TGEN works with the VGEN processor and supports simplex and TMR applications. One TGEN connects to the VGEN with a single cable. In TMR systems, TGEN connects to three VGEN boards with three separate cables.



Generator Terminal Board, Processor Board, and Cabling

Installation

Connect the wires for the analog current and PT inputs to TB1. Connect the wires for the CT inputs to special terminal blocks TB2, TB3, and TB4. The blocks cannot be unplugged, protecting against an open CT circuit. Use jumpers J#A and J#B to select the input as a current or voltage input on analog inputs 1 through 4.



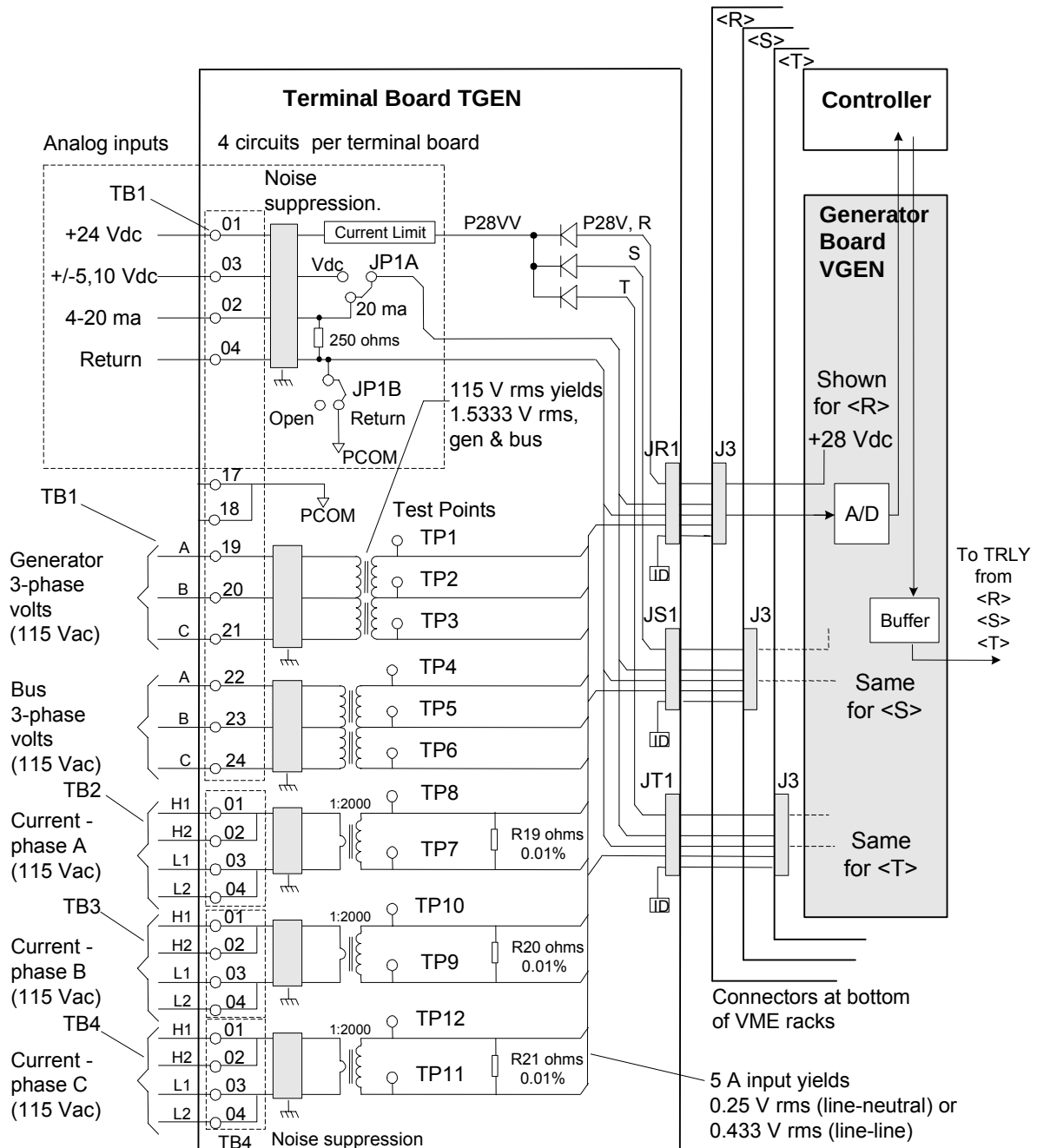
Terminal block 1 can be unplugged from terminal board for maintenance. TB2, TB3, TB4 are not pluggable.

TGEN Terminal Board and Wiring

Operation

VGEN monitors two, three-phase PT inputs, and three, one-phase current transformer CT inputs from TGEN. Using jumpers, four analog inputs can be configured for 4-20 mA or ± 5 , ± 10 V dc.

Test points on the generator and bus voltages and currents are used to check the phase of the input signals. VGEN performs signal conversions and power, power factor, and frequency calculations.



Note Test points are provided for all PT and CT inputs to verify the phase in the field.

Three single-phase CT inputs are provided with a normal current range of 0 to 5 A continuous. The CTs are magnetically isolated on TGEN. The CTs connect to non-pluggable terminal blocks with captive lugs accepting are up to #10 AWG wires.

The four analog inputs accept 4-20 mA inputs or ± 5 , ± 10 V dc inputs. A +24 V dc source is available for all four circuits with individual current limits for each circuit. The 4-20 mA transducer can use the +24 V dc source from the turbine control or a self-powered source.

Specifications

Item	Specification
Inputs to TGEN and VGEN	2 three-phase generator and bus PTs 3 one-phase generator CTs 4 analog inputs (4-20 mA, ± 5 , ± 10 V dc)
Generator and bus voltages	Nominal 115 V rms with range of interest of 10 to 120% Nominal frequency 50/60 Hz with range of interest 25 to 66 Hz Magnetic isolation to 1,500 V rms and loading less than 3 VA Input loading less than 3 VA per circuit
Generator current inputs	Normal current range is 0 to 5 A with over-range to 10 A Nominal frequency 50/60 Hz with range of interest 45 to 66 Hz Magnetic isolation to 1,500 V rms Input burden less than 0.5 Ω per circuit
Analog inputs	Current inputs: 4-20 mA Voltage inputs: ± 5 V dc or ± 10 V dc Transducers can be up to 300 m (984 ft) from the control cabinet with a two-way cable resistance of 15 Ω . Input burden resistor on TGEN is 250 Ω . Jumper selection of single ended or self powered inputs Jumper selection of voltage or current inputs

Diagnostics

Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check. The software limit check is adjustable in the field. Open wire detection is provided for voltage inputs, and relay drivers and coil currents are monitored.

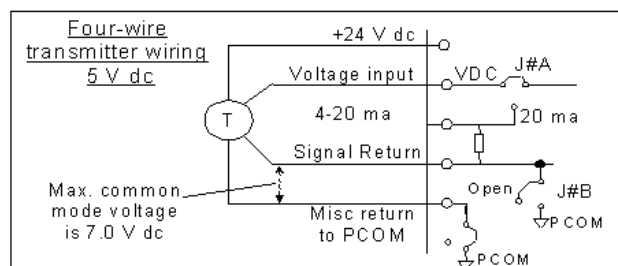
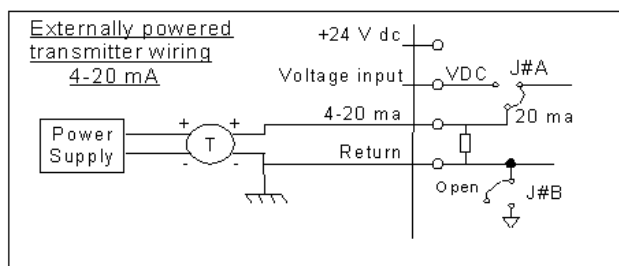
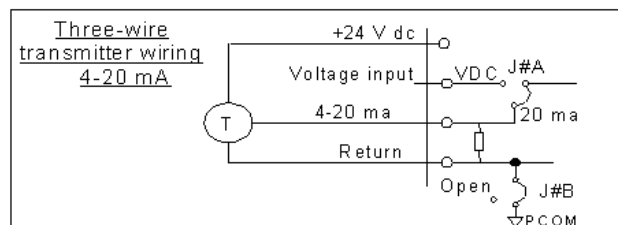
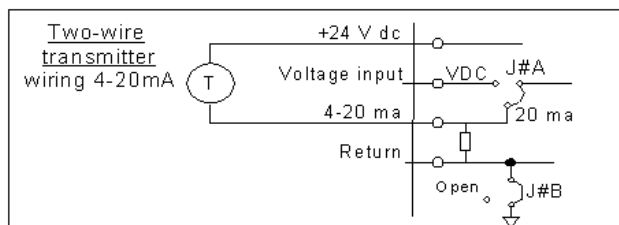
Connectors JR1, JS1, and JT1 on TGEN have their own ID device that is interrogated by VGEN. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location.

Configuration

Configuration of the terminal board is by means of jumpers. For location of these jumpers refer to the installation diagram. The jumper choices are as follows:

- Jumpers J1A through J4A select either current input or voltage input
- Jumpers J1B through J4B select whether the return is connected to common or is left open

The following diagrams illustrate connections for common analog inputs.



TRL YH1B Relay Output with Coil Sensing

Functional Description

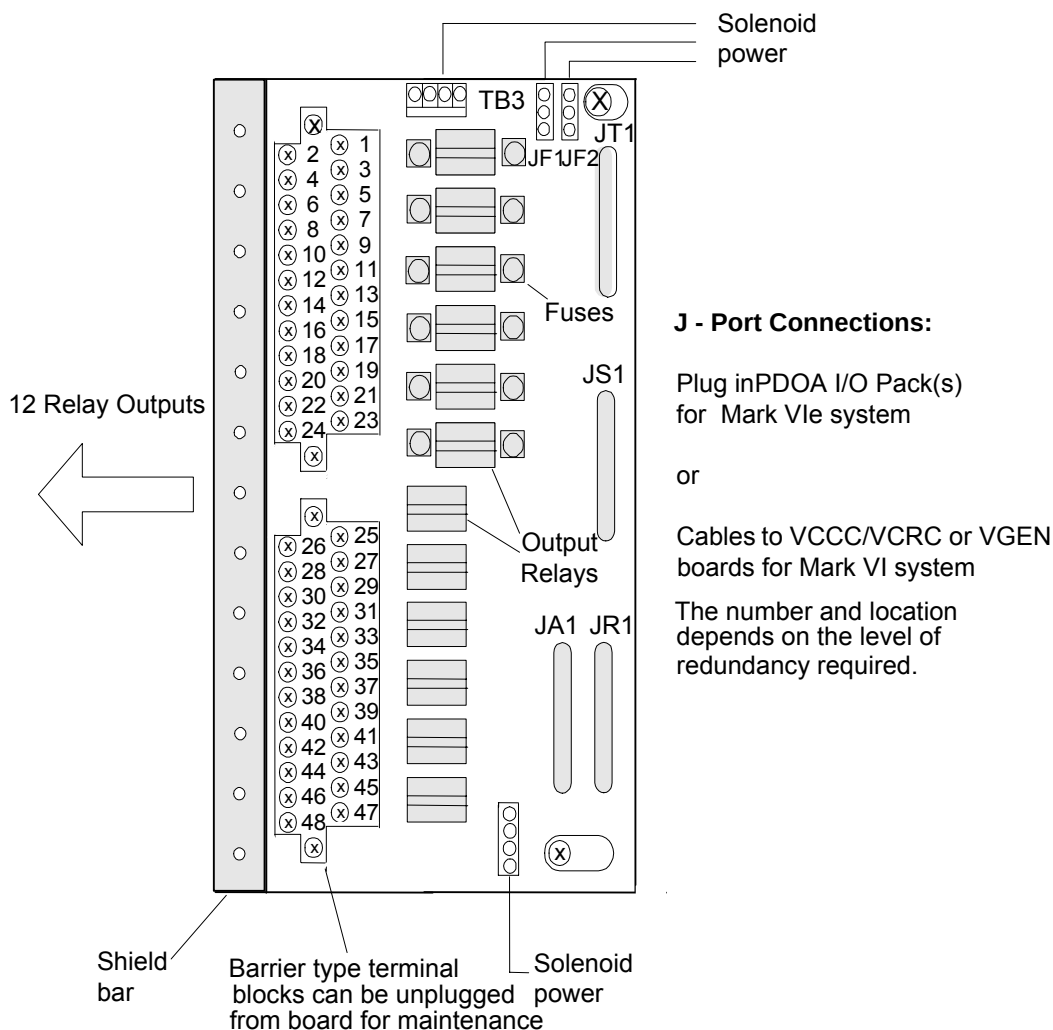
The Relay Output with coil sensing (TRL YH1B) terminal board holds 12 plug-in magnetic relays. The first six relay circuits configured by jumpers for either dry, Form-C contact outputs, or to drive external solenoids. A standard 125 V dc or 115/230 V ac source, or an optional 24 V dc source with individual jumper selectable fuses and on-board suppression, can be provided for field solenoid power. The next five relays (7-11) are unpowered isolated Form-C contacts. Output 12 is an isolated Form-C contact, used for special applications such as ignition transformers.

Mark VI Systems

In Mark* VI systems, TRLY is controlled by the VCCC, VCRC, or VGEN board and supports simplex and TMR applications. Cables with molded plugs connect the terminal board to the VME rack where the I/O boards are mounted. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.

Mark VIe Systems

In the Mark VIe system, the TRLY works with the PDOA I/O pack and supports simplex and TMR applications. PDOA plugs into the DC-37 pin connectors on the terminal board. Connector JA1 is used on simplex systems, and connectors JR1, JS1, and JT1 are used for TMR systems.



TRLYH1B Relay Output Terminal Board

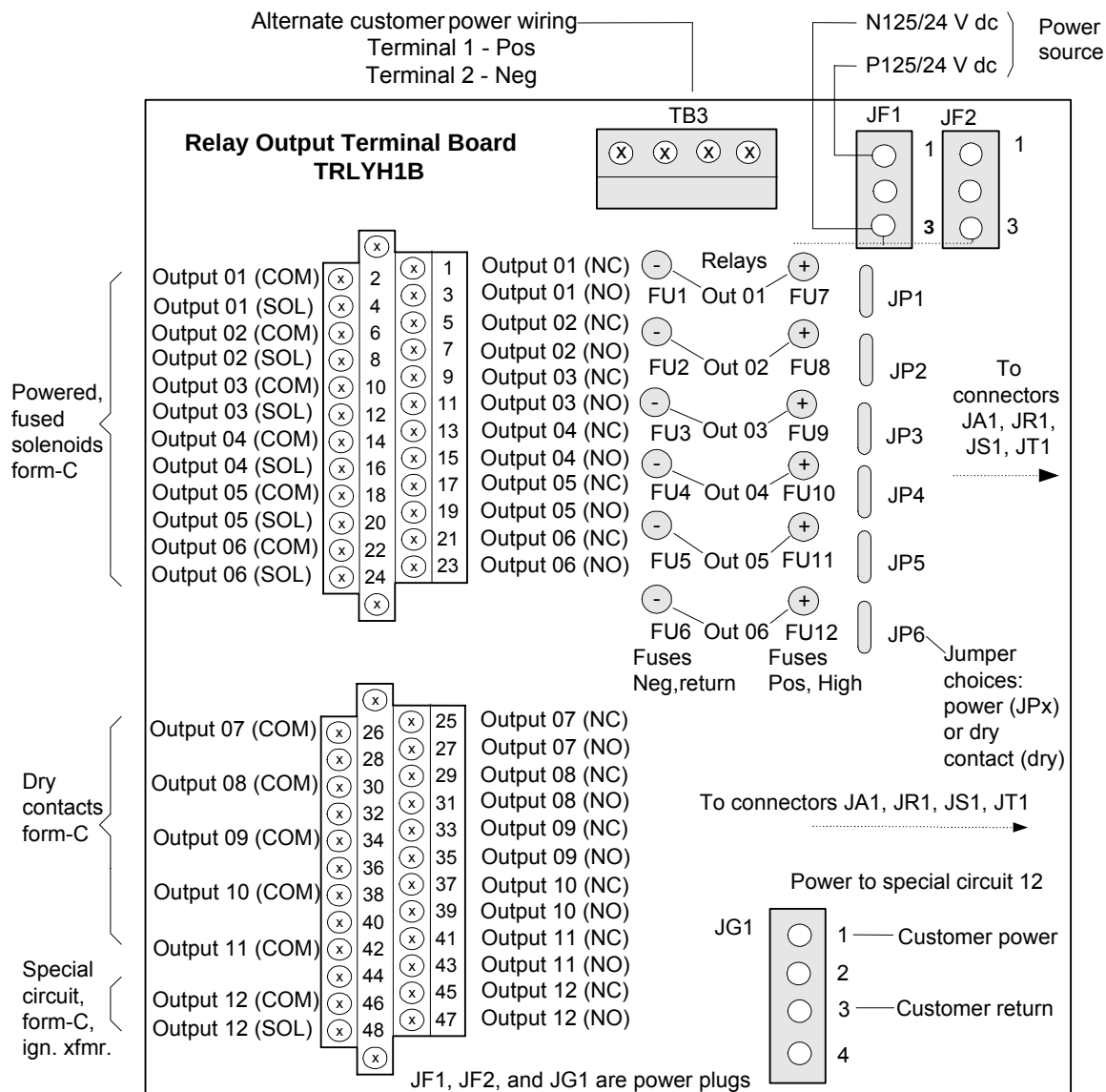
Installation

Connect the wires for the 12 relay outputs directly to two I/O terminal blocks on the terminal board as shown in the figure, *TRLYH1B Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on the left side of each terminal block.

Connect the solenoid power for outputs 1-6 to JF1. JF2 can be used to daisy chain power to other TRLYs. Alternatively, power can be wired directly to TB3 when JF1/JF2 are not used. Connect power for the special solenoid, Output 12, to connector JG1.

Jumpers JP1-JP6 are removed in the factory and shipped in a plastic bag. Re-install the appropriate jumper if power to a field solenoid is required. Conduct individual loop energization checks as per standard practices and install the jumpers as required. For isolated contact applications, remove the fuses to ensure that suppression leakage is removed from the power bus.

Note These jumpers are also for isolation of the monitor circuit when used on isolated contact applications.

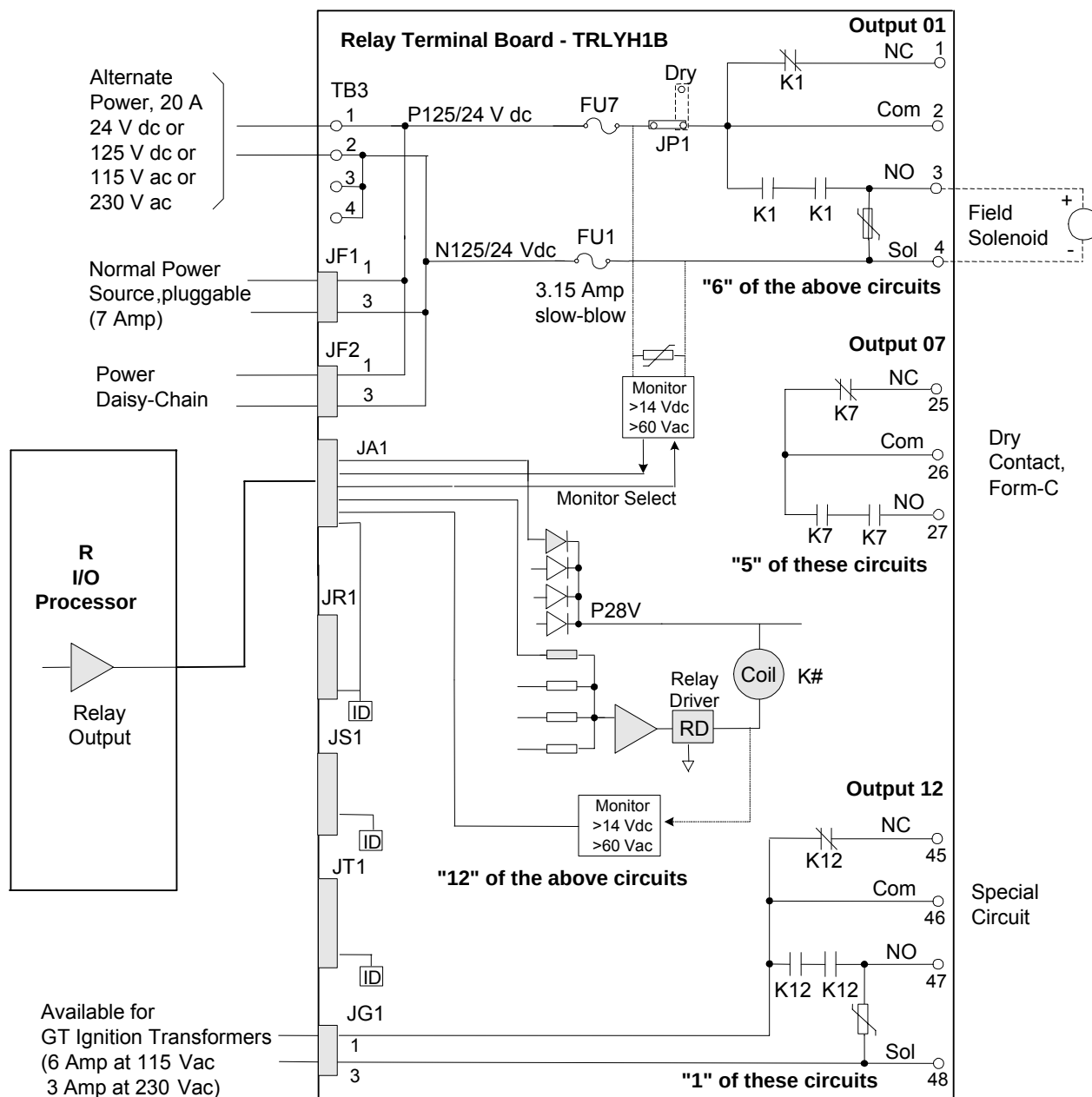


TRLYH1B Terminal Board Wiring

Operation

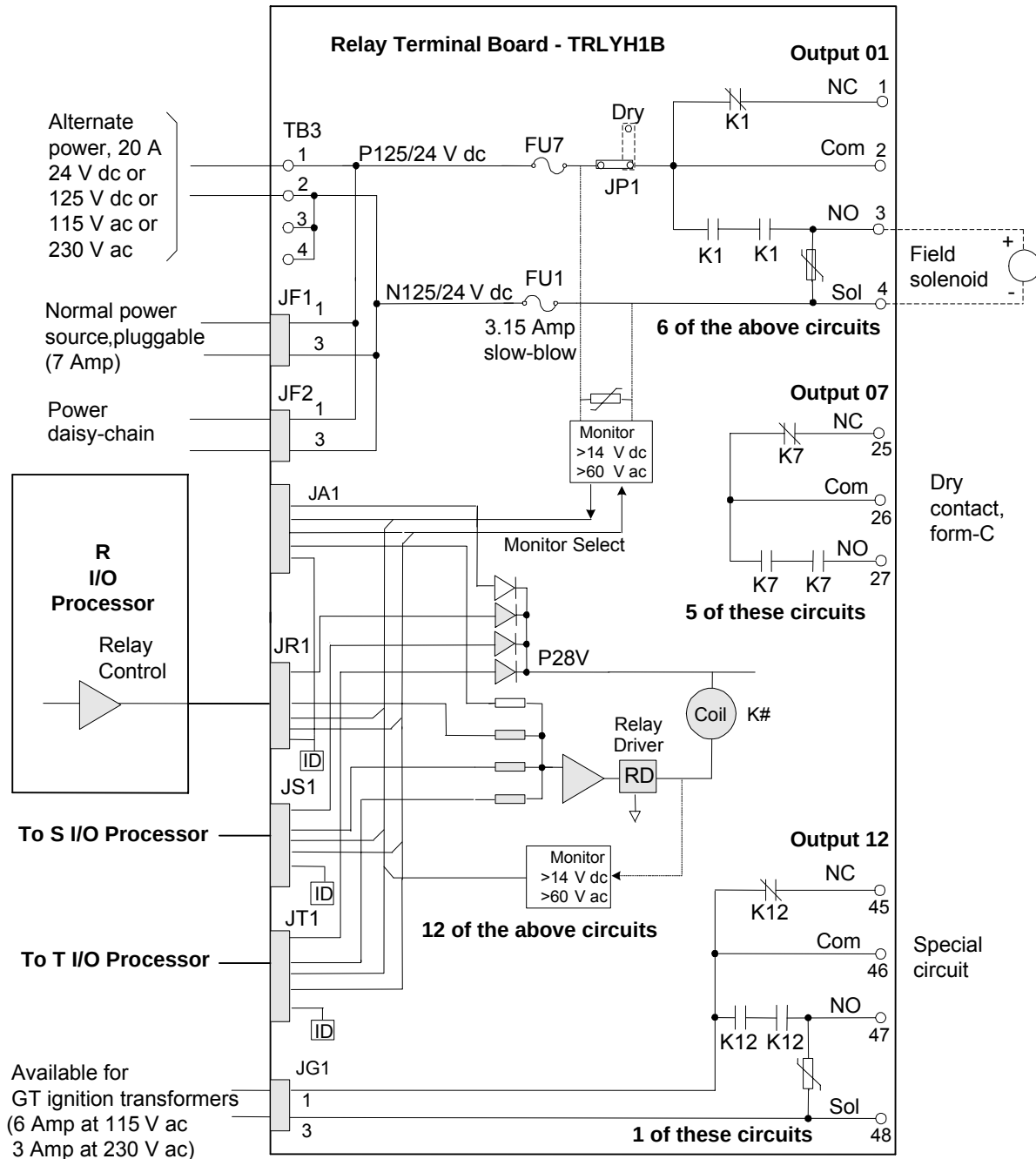
Relay drivers, fuses, and jumpers are mounted on the TRLYH1B. For simplex operation, D-type connectors carry control signals and monitor feedback voltages between the I/O processors and TRLY through JA1.

Relays are driven at the frame rate and have a 3.0 A rating. The rated contact-to-contact voltage is 500 V ac for one minute. The rated coil to contact voltage is 1,500 V ac for one minute. The typical time to operate is 10 ms. Relays 1-6 have a 250 V metal oxide varistor (MOV) for transient suppression between normally open (NO) and the power return terminals. The relay outputs have a failsafe feature that vote to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O processor is lost.



TRLYH1B Circuits, Simplex System

For TMR applications, relay control signals are fanned into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals are voted and the result controls the corresponding relay driver. Power for the relay coils comes from all three I/O processors and is diode-shared. The following figure shows a TRLYH1B in a TMR system.



TRLYH1B Circuits, TMR System

Specifications

Item	Specifications
Number of relay channels on one TRLY board	12: 6 relays with optional solenoid driver voltages 5 relays with dry contacts only 1 relay with 7 A rating
Rated voltage on relays	a: Nominal 125 V dc or 24 V dc b: Nominal 115/230 V ac
Max load current	a: 0.6 A for 125 V dc operation b: 3.0 A for 24 V dc operation c: 3.0 A for 115/230 V ac, 50/60 Hz operation
Max response time on	25 ms typical
Max response time off	25 ms typical
Maximum inrush current	10 A
Contact material	Silver cad-oxide
Contact life	Electrical operations: 100,000 Mechanical operations: 10,000,000
Fault detection	Loss of relay solenoid excitation current Coil current disagreement with command Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost.
Physical	
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to +149 °F)

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The output of each relay (coil current) is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The solenoid excitation voltage is monitored downstream of the fuses and an alarm is latched if it falls below 12 V dc.
- If any one of the outputs goes unhealthy a composite diagnostics alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O pack/board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location. When the chip is read by the I/O processor and mismatch is encountered, a hardware incompatibility fault is created.
- Relay contact voltage is monitored.
- Details of the individual diagnostics are available in the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

Board adjustments are made as follows:

- Jumpers JP1 through JP12. If contact voltage sensing is required, insert jumpers for selected relays.
- Fuses FU1 through FU12. If power is required for relays 1-6, two fuses should be placed in each power circuit supplying those relays. For example, FU1 and FU7 supply relay output 1. Refer to terminal board wiring diagram for more information.

TRL YH1F Relay Output with TMR Contact Voting

Functional Description

The Relay Output with TMR contact voting (TRL YH1F) terminal board provides 12 contact-voted relay outputs. The board holds 12 sealed relays in each TMR section, for a total of 36 relays. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied.

Note TRL YH1F and H2F do not support simplex arrangements

TRL YH1F does not have power distribution. However, an optional power distribution board, IS200WPDFH1A, can be added so that a standard 125 V dc or 115 V ac source, or an optional 24 V dc source with individual fuses, can be provided for field solenoid power.

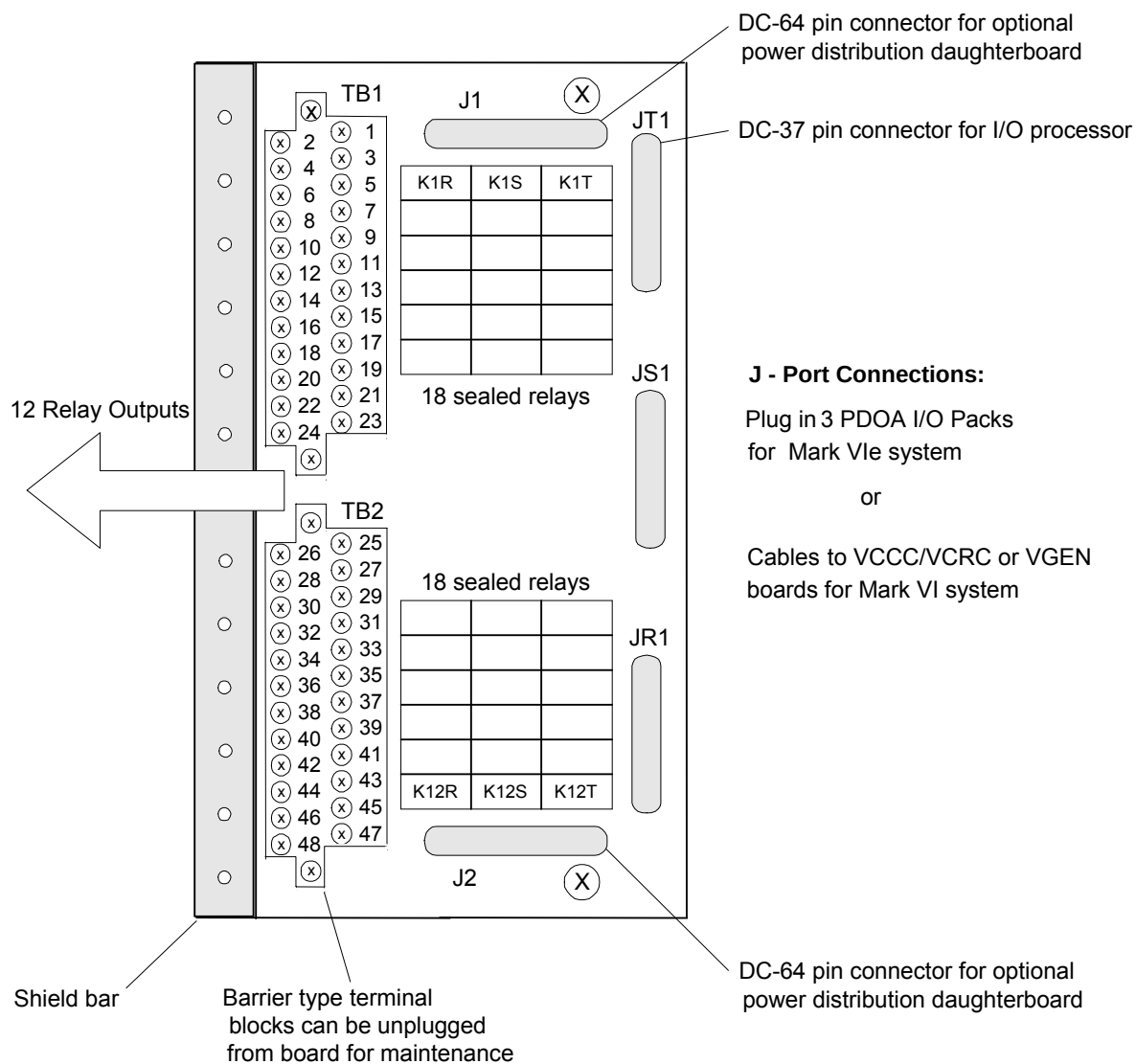
TRL YH2F is same as TRL YH1F except that the voted contacts form a Form B (NC) output. Both boards can be used in Class 1 Division 2 applications.

Mark VI Systems

In the Mark* VI system, the TRL Y is controlled by the VCCC, VCRC, or VGEN board and only supports TMR applications. Cables with molded plugs connect JR1, JS1, and JT1 to the VME rack where the I/O boards are mounted.

Mark VIe Systems

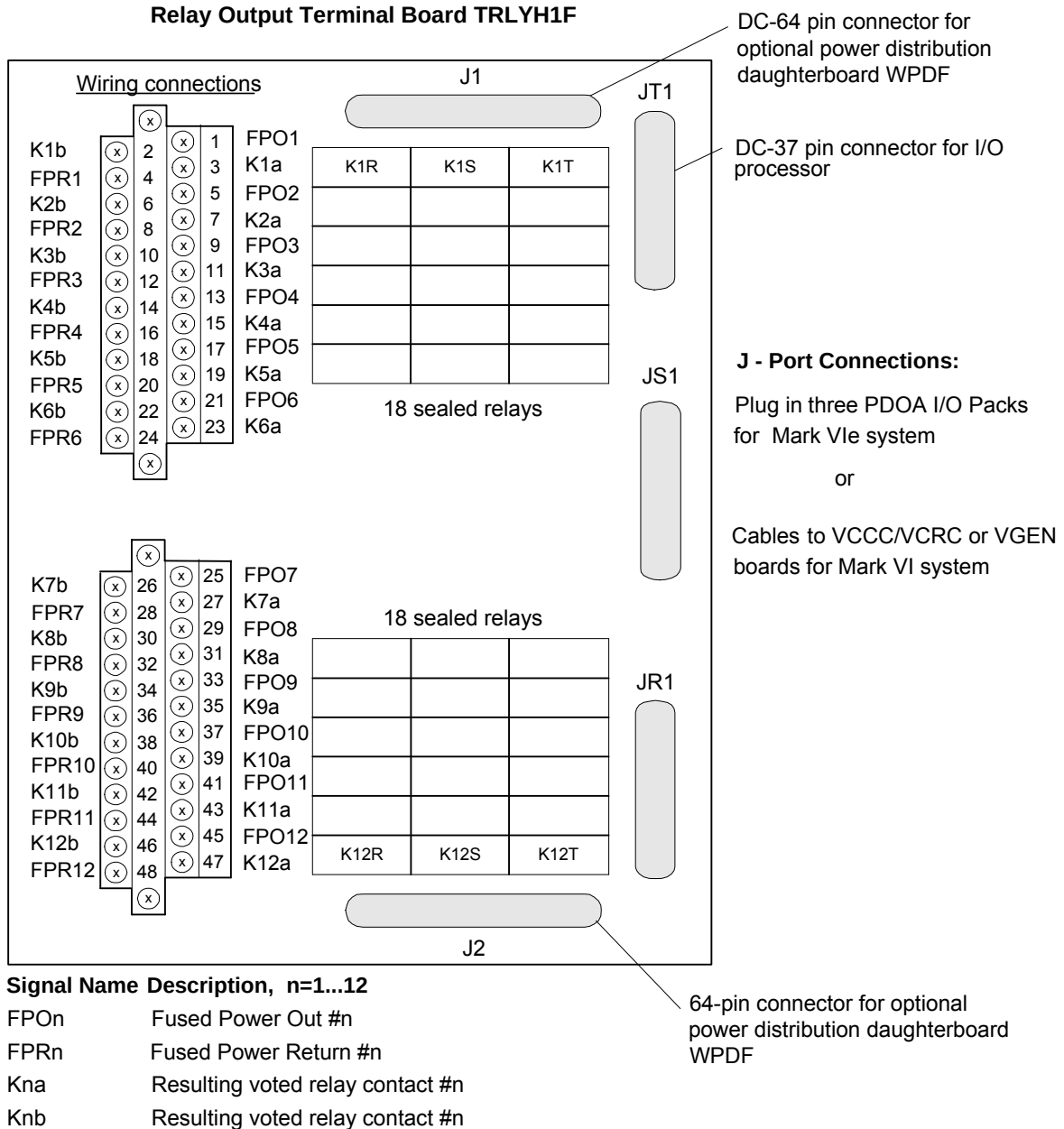
In the Mark VIe system, the TRL Y works with PDOA I/O pack and only supports TMR applications. Three TMR PDOA packs plug into the JR1, JS1, and JT1 37-pin D-type connectors on the terminal board.



TRL YH1F Relay Output Terminal Board

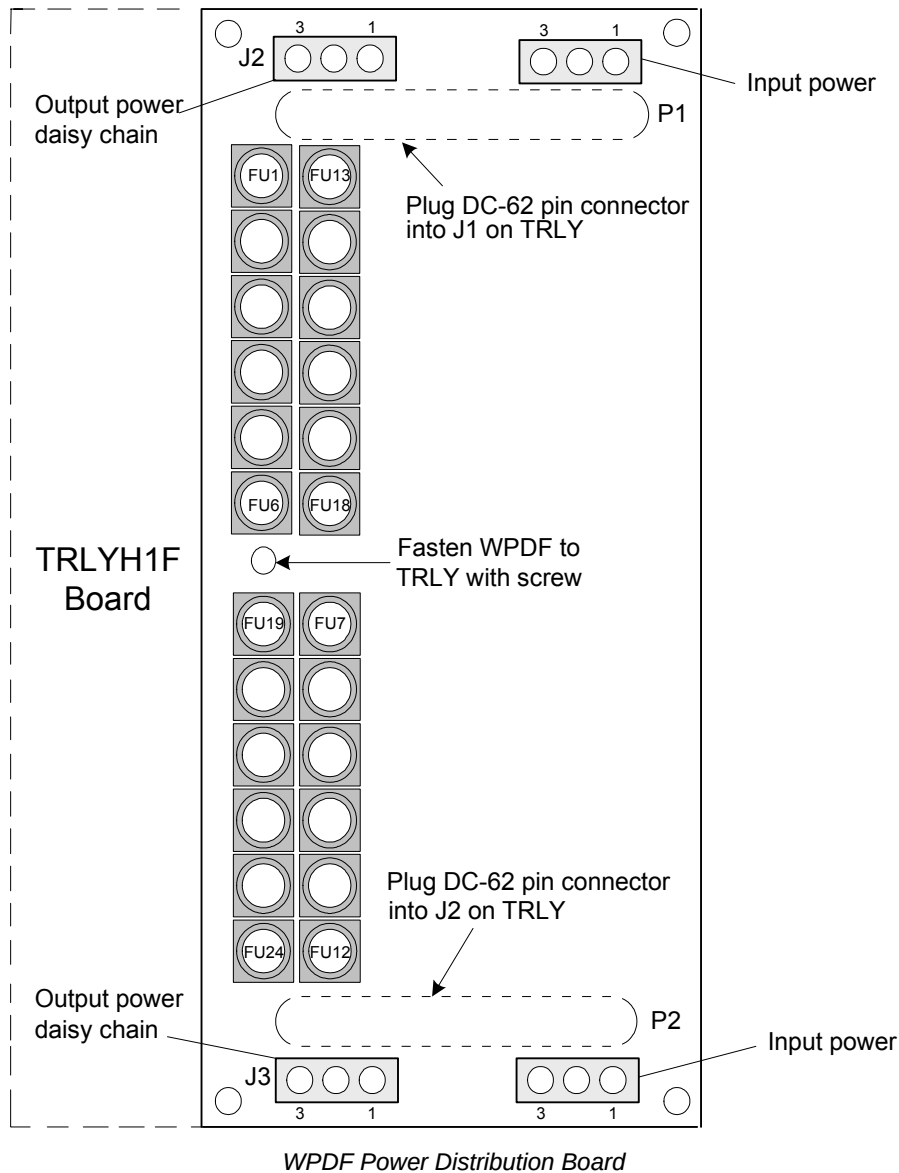
Installation

Connect the wires for the 12 solenoids directly to two I/O terminal blocks on the terminal board as shown in the following figure, *TRLYH1F Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left side of each terminal block. Solenoid power for outputs 1-12 is available if the WPDF daughterboard is used. Alternatively, power can be wired directly to the terminal block.

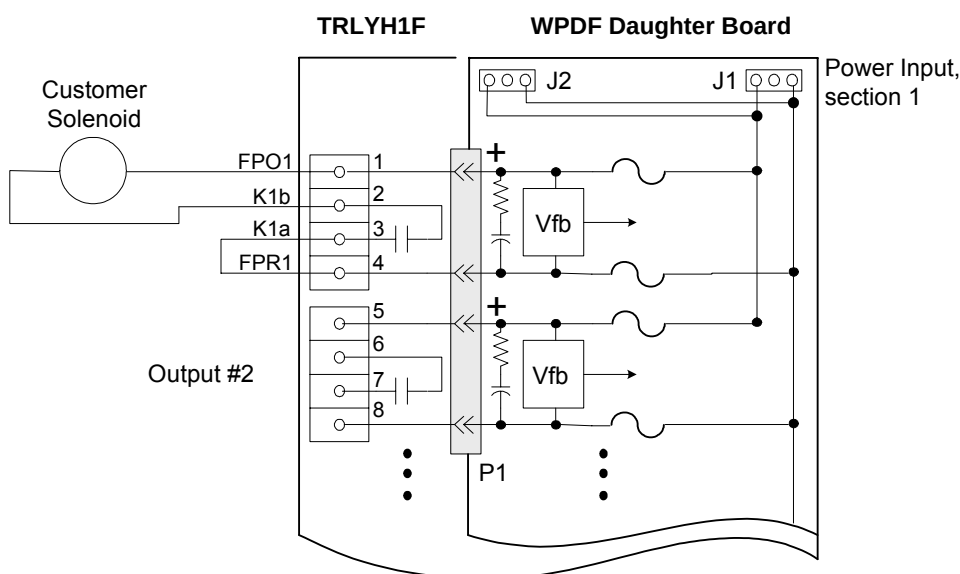


Power Distribution Board

If using the optional WPDF power distribution board, mount it on top of TRLY on the J1 and J2 connectors. Secure WPDF to TRLY by fastening a screw in the hole located at the center of WPDF. Connect the power for the two sections of the board on the three-pin connectors J1 and J4. Power can be daisy-chained out through the adjacent plugs, J2 and J3.



The solenoids must be wired as shown in the following figure. If WPDF is not used, the customer must supply power to the solenoids.



Wiring to Solenoid using WPDF

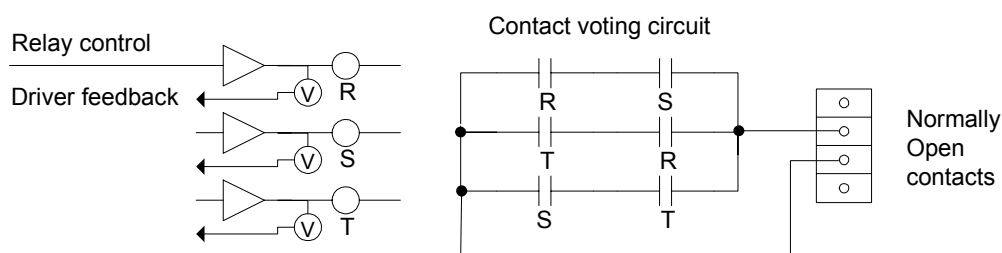
Operation

The 28 V dc power for the terminal board relay coils and logic comes from the three I/O processors connected at JR1, JS1, and JT1. The same relays are used for ac voltages and dc voltages, as specified in the *Specifications* section. H1F and H2F use the same relays with differing circuits.

Relay drivers are mounted on the TRLYH1F and drive the relays at the frame rate. The relay outputs have a failsafe feature that votes to de-energize the corresponding relay when a cable is unplugged or communication with the associated I/O board or I/O pack is lost.

This board only supports TMR applications. The relay control signals are routed into TRLY from the three I/O processors R, S, and T through plugs JR1, JS1, and JT1. These signals directly control the corresponding relay driver for each TMR section R, S, and T. Power for each section's relay coils comes in from its own I/O processor and is not shared with the other sections.

TRLYH1F features TMR contact voting. The relay contacts from R, S, and T are combined to form a voted Form A (NO) contact. 24/125 V dc or 115 V ac can be applied. TRLYH2F is the same except that the voted contacts form a Form B (NC) output. The following figure shows TMR voting contact circuit.

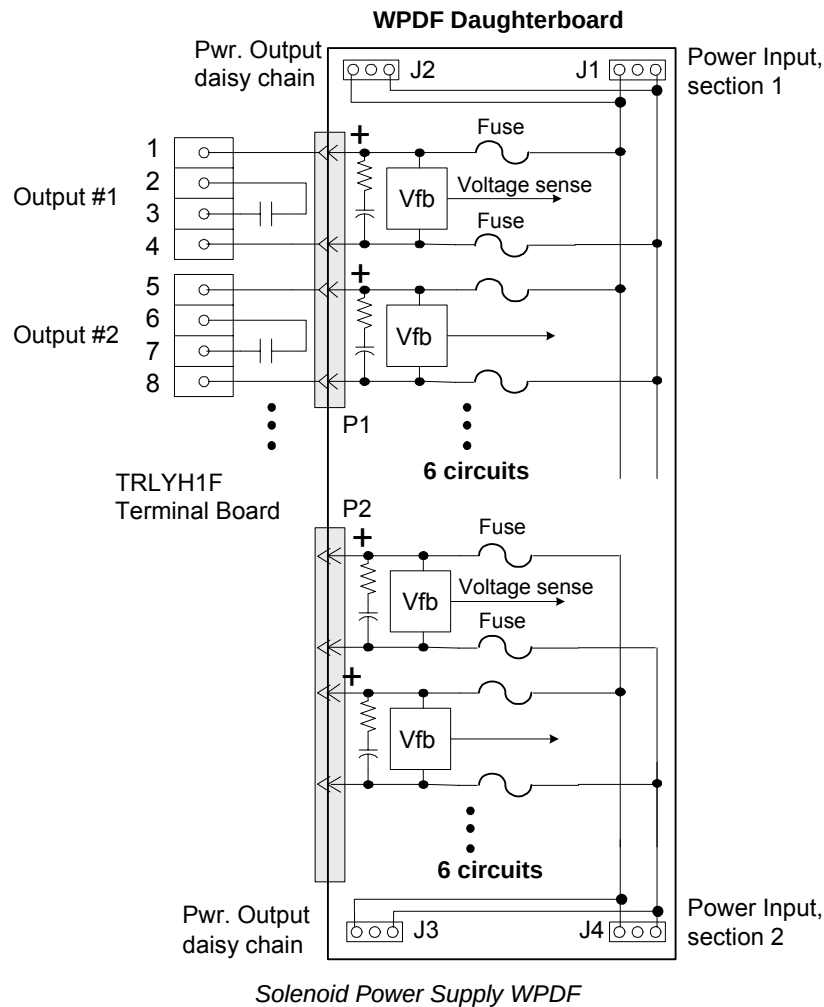


TRLYH1F Contact Arrangement for TMR Voting

Field Solenoid Power Option

The WPDFH1A daughterboard supplies power to TRLYH#F to power solenoids. WPDF holds two power distribution circuits, which can be independently used for standard 125 V dc, 115 V ac, or 24 V dc sources. Each section consists of six fused branches that provide power to TRLYH#F. Each branch has its own voltage monitor across its secondary fuse pair. Each voltage detector is fanned to three independent open-collector drivers for feedback to each of the I/O processors R, S, and T.

WPDF should not be used without TRLYH#F. Fused power flows through this board down to the TRLY terminal board points. TRLY controls the fuse power feedback. The following figure shows TRLYH1F/WPDF solenoid power circuit.



Specifications

Item	Specification
Number of output relay channels	12
Board types	H1F: NO contacts H2F: NC contacts
Rated voltage on relays	a: Nominal 100/125 V dc or 24 V dc b: Nominal 115 V ac
Maximum load current	a: 0.5/0.3 A resistive for 100/125 V dc operation b: 5.0 A resistive for 24 V dc operation c: 5.0 A resistive for 115 V ac
Maximum response time on Contact life	25 ms Electrical operations: 100,000
Fault detection	Coil Voltage disagreement with command Blown fuse indication (with WPDF power daughterboard). Unplugged cable or loss of communication with I/O board; relays de-energize if communication with associated I/O board is lost.
WPDF Solenoid Power Distribution Board	
Number of Power Distribution Circuits (PDC)	2: Each rated 10 A, nominal 115 V ac or 125 V dc.
Number of Fused Branches	12: 6 for each PDC
Fuse rating	3.15 A at 25°C (77 °F) 2.36 A – recommended maximum usage at 65°C (149 °F)
Voltage monitor, maximum response delay	60 ms typical
Voltage monitor, minimum detection voltage	16 V dc 72 V ac
Voltage monitor, max current (leakage)	3 mA
Physical	
Size - TRLY	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)
Size - WPDF	10.16 cm wide x 33.02 cm high (4.0 in x 13.0 in)
Temperature	-30 to + 65°C (-22 to +149 °F)
Technology	Surface-mount

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- The voltage to each relay coil is monitored and checked against the command at the frame rate. If there is no agreement for two consecutive checks, an alarm is latched.
- The voltage across each solenoid power supply is monitored and if it goes below 16 V ac/dc, an alarm is created.
- If any one of the outputs goes unhealthy a composite diagnostic alarm, L3DIAG_xxxx occurs.
- When an ID chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the JR1/JS1/JT1 connector location.

Details of the individual diagnostics are available from the configuration application. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

There are no jumpers or hardware settings on the board.

VPRO Turbine Protection Board

VPRO Emergency Turbine Protection

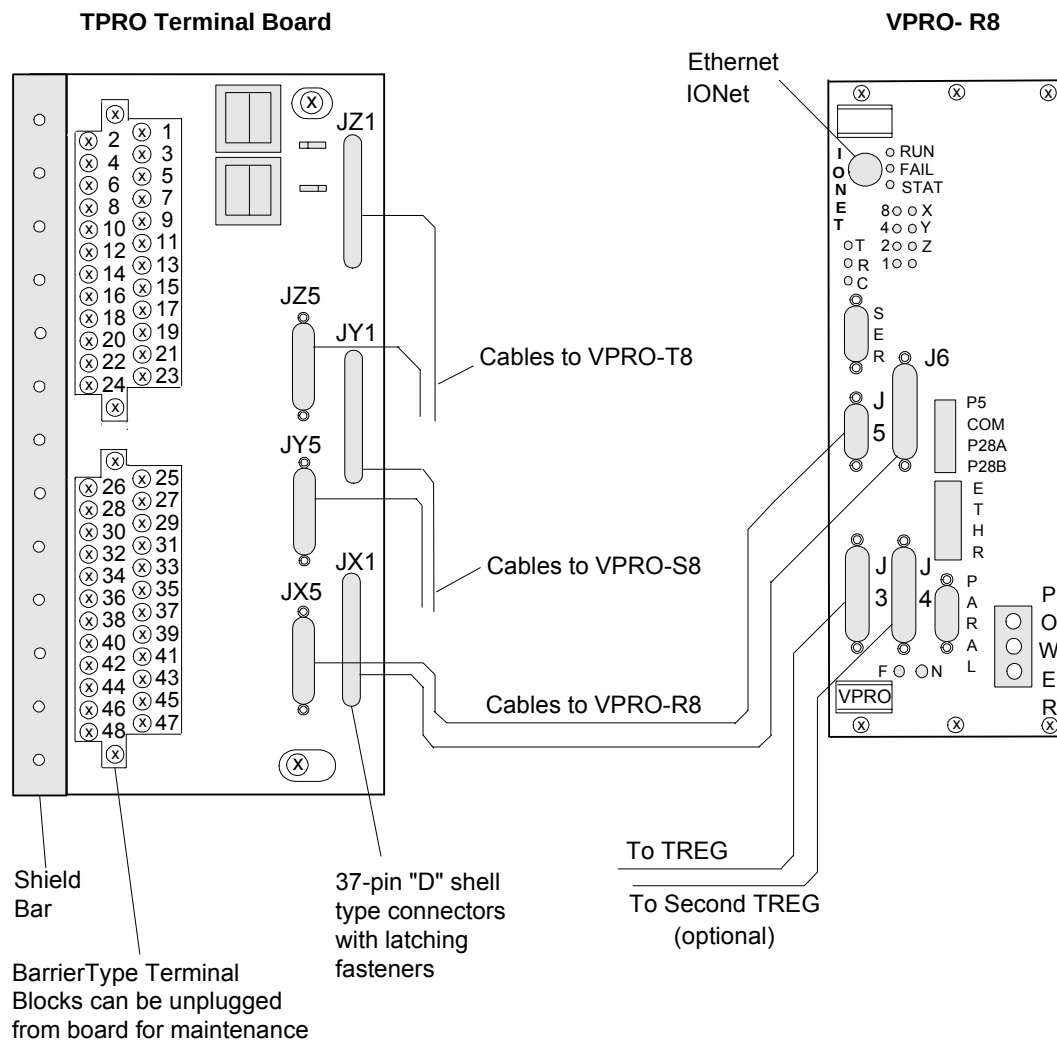
Functional Description

The Emergency Turbine Protection (VPRO) board and associated terminal boards (TPRO and TREG) provide an independent emergency overspeed protection system. The protection system consists of triple redundant VPRO boards in a module separate from the turbine control system, controlling the trip solenoids through TREG. The figures show the cabling to VPRO from the TPRO and TREG terminal boards.

Note VPRO also has an Ethernet connection for IONet communications with the control modules.

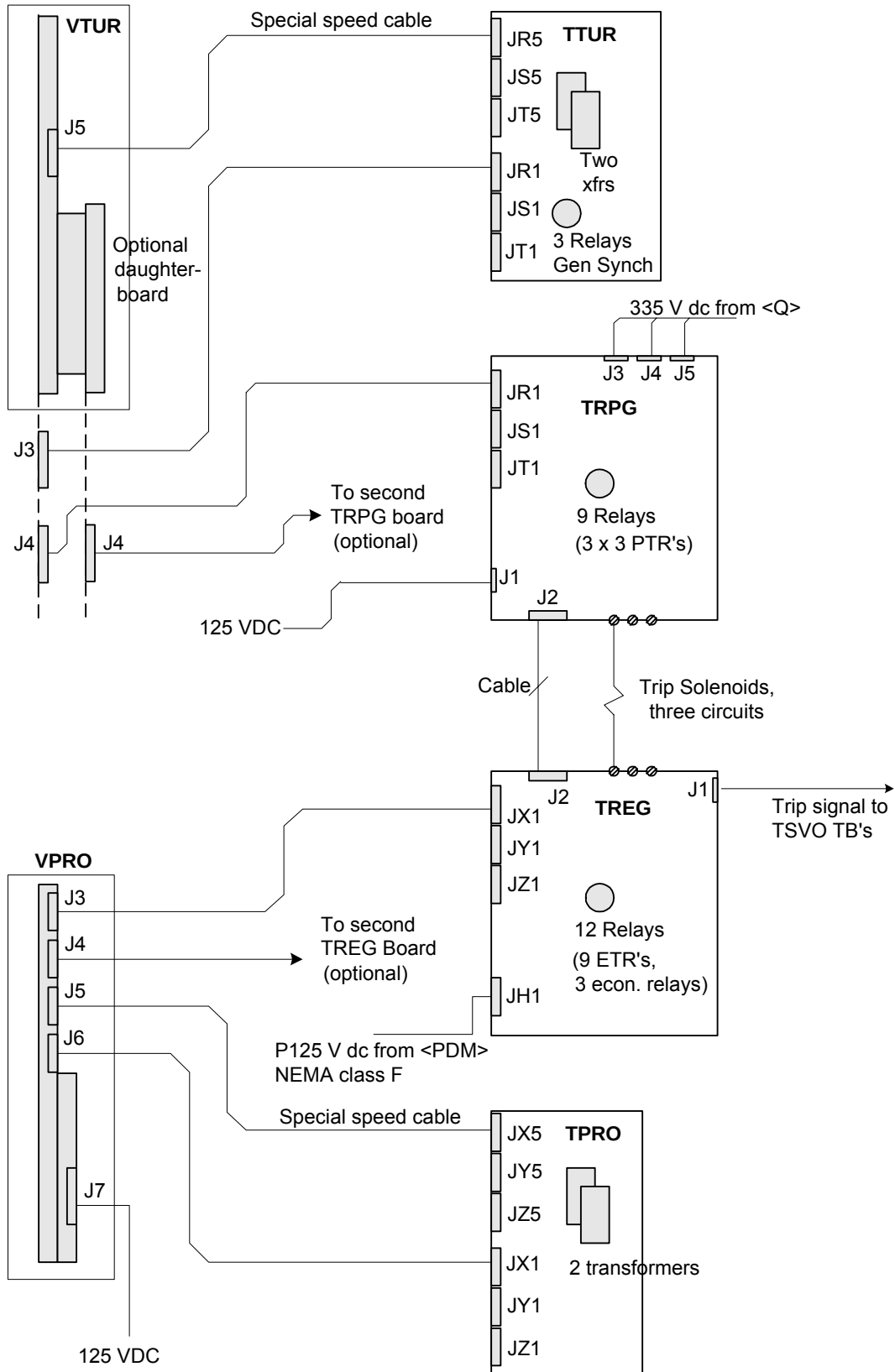
The VPRO board in the Protection Module <P> provides the emergency trip function. Up to three trip solenoids can be connected between the TREG and TRPG terminal boards. TREG provides the positive side of the 125 V dc to the solenoids and TRPG provides the negative side. Either board can trip the turbine. VPRO provides emergency overspeed protection and the emergency stop functions. It controls the 12 relays on TREG, nine of which form three groups of three to vote inputs controlling the three trip solenoids.

The original VPROH1A has been superseded by the functionally equivalent VPROH1B. VPROH1A and VPROH1B supports a second TREG board driven from VPRO connector J4. VPROH2B is a lower power version of VPRO that omits support for the second TREG board. Applications using a second TREG board connected to J4 must use VPROH1A or VPROH1B, not VPROH2B.



VPRO Board, TPRO Terminal Board, and Cabling

The figure shows how the VTUR and VPRO processor boards share in the turbine protection scheme. Either one can independently trip the turbine using the relays on TRPG or TREG.



Turbine Control and Protection Boards

Installation

➤ To install the V-type board

- 1 Power down the VME I/O processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel
- 4 Power up the VME rack and check the diagnostic lights at the top of the front panel

Note Cable connections to the terminal boards are made at the J3, J4, J5, and J6 connectors on VPRO front panel. These are latching type connectors to secure the cables. Connector J7 is for 125 V dc power. For details refer to the section on diagnostics in this document.

It may be necessary to update the VPRO firmware to the latest level. For instructions, refer to *GEH-6403 Control System Toolbox for a Mark VI Turbine Controller*.

Operation

The main purpose of the protection module is emergency overspeed (EOS) protection for the turbine, using three VPRO boards. In addition, VPRO has backup synchronization check protection, three analog current inputs, and nine thermocouple inputs, primarily intended for exhaust over-temperature protection on gas turbines.

The protection module is always triple redundant with three completely separate and independent VPRO boards named R8, S8, and T8 (originally named X, Y, and Z). Any one of these boards can be powered down and replaced while the turbine is running without jeopardizing the protection system. Each board contains its own I/O interface, processor, power supply, and Ethernet communications (IONet) to the controller. The communications allow initiation of test commands from the controller to the protection module and the monitoring of EOS system diagnostics in the controller and on the operator interface. Communications are resident on the VPRO board. The VPRO board has a VME interface that allows programming and testing in a VME rack. However, the backplane is neutralized when plugged into the protection module to eliminate any continuity between the three independent sections.

Speed Control and Overspeed Protection

Speed control and overspeed protection is implemented with six passive, magnetic speed pickups. The first three are monitored by the controllers, which use the median signal for speed control and primary overspeed protection. The second three are separately connected to the R8, S8, and T8 VPROs in the protection module. Provision is made for nine passive magnetic speed pickups or active pulse rate transducers (TTL type) on the TPRO terminal board with three being monitored by each of the R8, S8, and T8 VPROs. Separate overspeed trip settings are programmed into the application software for the primary and emergency overspeed trip limits, and a second emergency overspeed trip limit must be programmed into the I/O configurator to confirm the emergency overspeed (EOS) trip point.

The speed is calculated by counting passing teeth on the wheel and measuring the time involved. Another protection feature is: after the turbine reaches a predetermined steady-state speed, the rate of change of speed is continuously calculated and compared with 100%/sec and transmitted to the controller to trip the unit if it is detected. This steady-state speed limit is a tuning constant located in the controller's application software. Another speed threshold which is monitored by the EOS system, is 10% speed. This is transmitted to the controller to verify that there is no gross disagreement between the first set of three speed pickups being monitored by the controller (for speed control and the primary overspeed protection) and the second set of three speed pickups being monitored by the EOS system.

Speed Difference Detection

There should never be a reason why the speed calculated by PPRO is significantly different from the speed calculated by the main control. Speed difference detection looks at the difference in magnitude between pulse rate 1 from both PPRO and the main control. If the difference is greater than the set threshold for three successive samples, a SpeedDifTrip is latched. If the main control recovers for 60 seconds, the trip is removed. This allows the main control to recover with subsequent re-arming of the backup protection.

Interface To Trip Solenoids

The trip system combines the Primary Trip Interface from the controller with the EOS Trip Interface from the protection module. Three separate, triple redundant trip solenoids (also called Electrical Trip Devices - ETDs) are used to interface with the hydraulics. The ETDs are connected between the TRPG and TREG terminal boards. A separately fused 125 V dc feeder is provided from the turbine control for each solenoid, which is energized in the run mode and de-energized in the trip mode.

Backup Synch Check Protection

Backup synch check protection is provided in the Protection Module. The generator and bus voltages are supplied from two, single phase, potential transformers (PTs) secondary output supplying a nominal 115 V rms. The maximum cable length between the PTs and the turbine control is 100 meters of 18 AWG twisted, shielded wire. Each PT is magnetically isolated with a 1,500 V rms rated barrier and a circuit load less than 3 VA. The synch algorithms are based on phase lock loop techniques. Phase error between the generator and bus voltages is less than +/-1 degree at nominal voltage and 50/60 Hz. A frequency range of 45 to 66 Hz is supported with the measured frequency within 0.05% of the input frequency. The algorithm is illustrated under TTUR, generator synchronizing.

Each PT input is internally connected in parallel to the R8, S8, and T8 VPROs. The triple redundant phase slip windows result in a voted logical output on the TREG terminal board, which drives the K25A relay. This relay's contacts are connected in series with the synch permissive relay (K25P) and the auto synch relay (K25) to insure that no false command is issued to close the generator breaker. Similarly, contacts from the K25A contact are connected in series with the contacts from remote, manual synchronizing equipment to insure no false commands.

Thermocouple and Analog Inputs

Thermocouple and analog inputs are available in the VPRO, primarily for gas turbine applications. Nine thermocouple inputs are monitored with three connected to each VPRO. These are generally used for backup exhaust over-temperature protection. Also, one ± 5 , 10 V dc, 4-20 mA (selectable) input, and two 4-20 mA inputs can be connected to the TPRO terminal board, which feeds the inputs in parallel to the three VPROs.

Power Supply

Each VPRO board has its own on-board power supply. This generates 5 V dc and 28 V dc using 125 V dc supplied from the cabinet PDM. The entire protection module therefore has three power supplies for high reliability

TREG is entirely controlled by VPRO, and the only connections to the control modules are the J2 power cable and the trip solenoids. In simplex systems a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

Control of Trip Solenoids

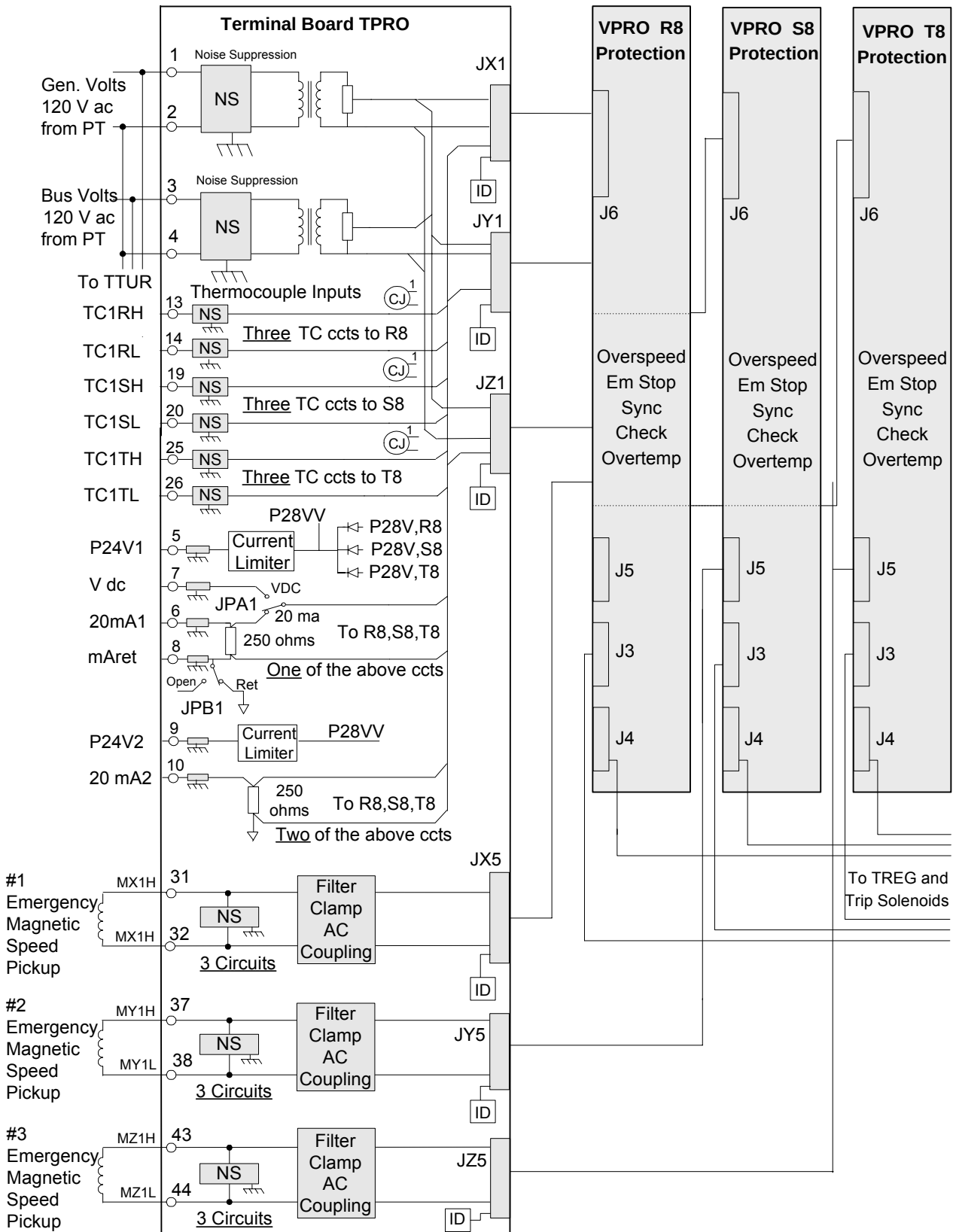
Note The solenoid circuit has a metal oxide varistor (MOV) for current suppression and a 10 Ω , 70 W economizing resistor.

Both TRPG and TREG control the trip solenoids so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. The three trip solenoids are supplied with 125 V dc through plug J2, and draw up to 1 A with a 0.1 second L/R time constant. The nine trip relay coils on TREG are supplied with 28 V dc from VPRO boards in R8, S8, and T8.

A separately fused 125 V dc feeder is provided for the solenoids, which energize in the run mode and de-energize in the trip mode. Diagnostics monitor each 125 V dc feeder from the power distribution module at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Solenoid Trip Tests

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time either through the PTR relays from the controller or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.



TMR VPROs and TPPO Terminal Board

Specifications

Item	Specification
Number of Inputs	3 Passive speed pickups 1 Generator and 1 Bus Voltage 3 Thermocouples 1 4-20 mA current or voltage 2 4-20 mA current 7 Trip interlocks 2 Emergency Stop
Number of Outputs	6 Trip Solenoids 6 Economizer relays 1 Breaker relay command, K25A on TTUR 1 Servo clamp relay contact, to TSVO boards
Power Supply Voltage	Input supply 125 V dc (70-145 V dc) Output 5 V dc and 28 V dc
Frame Rate	Up to 100 Hz
MPU Characteristics	Output resistance 200 Ω with inductance of 85 mH. Output generates 150 V p-p into 60 K Ω at the TPRO terminal block, with insufficient energy for a spark. The maximum short circuit current is approximately 100 mA. The system applies up to 400 Ω normal mode load to the input signal to reduce the voltage at the terminals.
MPU Cable	Sensors can be up to 300 m (984 ft) from the cabinet, assuming that shielded pair cable is used, with typical 70 nF single ended or 35 nF differential capacitance, and 15 Ω resistance.
MPU Pulse Rate Range	2 Hz to 20 kHz
MPU Pulse Rate Accuracy	0.05% of reading; resolution is 15 bits at 100 Hz Noise of the acceleration measurement is less than ± 50 Hz/sec for a 10,000 Hz signal being read at 10 ms.
MPU Input Circuit Sensitivity	Minimum signal is 27 mV pk at 2 Hz Minimum signal is 450 mV pk at 14 kHz
Generator and Bus Voltage Sensors	Two Single-Phase Potential Transformers, 115 V rms secondary voltage accuracy is 0.5% of rated Volts rms Frequency Accuracy 0.05% Phase Difference Measurement better than 1 degree. Allowable voltage range for synchronizing is 75 to 130 V rms. Each input has a load of less than 3 VA.
Thermocouple Inputs	Same specifications as for VTCC board
Analog Inputs	2 current inputs, 4-20 mA 1 current input, with selection of 4-20 mA, or ± 5 V dc, or ± 10 V dc. Same specifications as for VAIC board

Diagnostics

Three LEDs at the top of the VPRO front panel provide status information. The normal RUN condition is a flashing green, FAIL is a solid red. The third LED is STATUS and is normally off but shows a steady orange if a diagnostic alarm condition exists in the board. VPRO makes diagnostic checks and creates faults as follows:

- Trip relay driver and contact feedbacks
- Solenoid voltage and solenoid voltage source
- Economizer relay driver and contact feedbacks
- K25A relay driver and coil
- Servo clamp relay driver and contact feedback
- High and low limits on all analog inputs
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VPROR, or S, or T occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy.

Terminal board connectors on TPRO and TREG have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VPRO and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Parameter	Description	Choices
Configuration		
Turbine_Type	Define the type of turbine from selection of ten types	Two gas turbine, two LM, two large steam, one medium steam, one small steam, two stag GT
LMTripZEnable	On LM machine, when no PR on Z, enable vote for trip	Enable, disable
OT_Trip_Enbl	Enable overtemperature trip	Enable, disable
OvrTemp_Trip	Iso-thermal overtemperature trip setting for exhaust thermocouples in degree F	-60 to 2,000
TA_Trip_Enab1	Steam, enable trip anticipation on ETR1 (same for four ETRs)	Enable, disable
ContWdogEn	Enable trip on loss of control outputs to VPRO	Enable, disable
SpeedDifEn	Enable trip on speed difference between controller & VPRO	Enable, disable
StaleSpdEn	Enable trip on speed from controller freezing	Enable, disable
DiagSolPwrA	For TREL/TRES, sol power, BusA, diagnostic (same for three solenoids)	Enable, disable
RatedRPM_TA	Steam, rated RPM, used for trip anticipation calc	0 to 20,000
AccelCalType	Select acceleration calculation type	Slow, medium, fast
Auto Reset	Automatic restoring of thermocouples removed from scan	Enable, disable
OTBias_RampP	Overtemperature bias ramp positive	
OTBias_RampN	Overtemperature bias ramp negative	
Min_MA_Input	Minimum MA for healthy 4/20 ma Input	0 to 21
Max_MA_Input	Maximum MA for healthy 4/20 ma Input	0 to 21
OTBias_Dflt	Overtemperature bias	

Parameter	Description	Choices
OS_Diff	Absolute speed difference, in percent, for trip threshold (if SpeedDifEn enabled)	0 to 10
5J6:IS200TPRO		
PulseRate1	First of three speed inputs - card point	point edit (input FLOAT)
PRTYPE	Selects gearing (resolution)	Unused, PR<6,000 Hz, PR>6,000 Hz
PRScale	Pulses per revolution (output RPM)	0 to 1,000
OS_Setpoint	Overspeed trip setpoint in RPM	0 to 20,000
OS_Tst_Delta	Offline overspeed test setpoint delta in RPM	-2,000 to 2,000
Zero_Speed	Zero speed for this shaft in RPM	0 to 20,000
Min_Speed	Minimum speed for this shaft in RPM	0 to 20,000
Accel_Trip	Enable acceleration trip	Enable, disable
Acc_Setpoint	Accelerate trip setpoint in RPM/second	0 to 20,000
TMR_DiffLimt	Difference limit for voted pulse rate inputs in engineering units	0 to 20,000
BusPT_KVolts	Kilo-Volts RMS, bus potential transformer - card point	Point edit (input FLOAT)
PT_Input	PT input in kilovolts rms for PT_Output	0 to 1,000
PT_Output	PT output in volts rms for PT_Input typically 115	60 to 150
TMR_DiffLimt	Difference limit for voted PT inputs in percent	0 to 100
GenPT_KVolts	Kilo-Volts RMS, generator PT, configuration similar to Bus PT-card point	Point edit (input FLOAT)
TC1R	Thermocouple 1, for R module (first of R, S, and T) - card point	Point edit (input FLOAT)
ThermCplType	Select thermocouple type or mV input	Unused, mV, T, K, J, E
Low Pass Filter	Enable 2 Hz low pass filter	Enable, disable
TC2R	Thermocouple 2, for R module (first of R, S, and T) config as above - card point	Point edit (Input FLOAT)
TC3R	Thermocouple 3, for R module (first of R, S, and T) config as above - card point	Point edit (Input FLOAT)
Cold Junction	Cold junction for thermocouples 1-3	Point edit (Input FLOAT)
TMR_DiffLimt	Difference limit for voted TMR cold junction inputs in Deg F	-60 to 2,000
AnalogIn1	First of three analog inputs - card point	Point Edit (Input FLOAT)
Input Type	Type of analog input	Unused, 4-20 mA, ± 10 V
Low_Input	Input mA at low value	-10 to 20
Low_Value	Input value in engineering units at low value	-3.402e +38 to 3.402e +38
High_Input	Input mA at high value	-10 to 20
High_Value	Input value in engineering units at high mA	-3.402e +38 to 3.402e +38
InputFilter	Filter bandwidth in Hz	Unused, 12 Hz, 6 Hz, 3Hz, 1.5 Hz, 0.75 Hz
Trip_Enable	Enable trip for this mA input	Enable, Disable
DiagHighEnab	Enable high input limit diag	Enable, Disable
DiagLowEnab	Enable low input limit diag	Enable, disable
TripSetpoint	Trip setpoint in engineering units	-3.402e +38 to 3.402e +38
TripTimeDelay	Time delay before tripping turbine after signal exceeds setpoint in seconds	0 to 10
TMR_DiffLimt	Difference limit for voted TMR inputs in per cent of (High_Value-Low_Value)	0 to 100
J3:IS200TREG	First TREG board	Connected, not connected
KESTOP1_Fdbk1	Emergency Stop ESTOP1, inverse sense, K4 relay, True=Run - card point	Point edit (input BIT)
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
Contact1	Trip interlock 1 (first of 7) - card point	Point edit (Input BIT)

Parameter	Description	Choices
ContactInput	Trip interlock 1 used	Used, unused
SeqOfEvents	Record contact transitions in sequence of events	Enable, disable
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
TrpTimeDelay	Time delay before tripping turbine after contact opens (sec)	0 to 10
TripMode	Trip mode	Direct, conditional, disable
K1_Fdbk	Trip relay 1 feedback (first of 3) - card point	Point edit (Input BIT)
RelayOutput	Relay feedback used	Used, unused
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
DiagSolEnab	Enable solenoid voltage diagnostic	Enable, disable
KE1_Fdbk	Economizer relay for trip solenoid feedback (first of 3) - card point	Point edit (Input BIT)
RelayOutput	Economizer relay feedback used	Used, unused
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
K4CL_Fdbk	Drive control valve servos closed, use only for steam turbine simplex - card Point	Point edit (Input BIT)
Relay Output	Servo valve clamp used	Used, unused
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
K25A_Fdbk	Synchronizing check relay on TTUR - card point	Point edit (Input BIT)
SynchCheck	Synch check relay K25A used	Used, unused
DiagVoteEnab	Enable voting disagreement diagnostic	Enable, disable
SystemFreq	System frequency in Hz	50 or 60
ReferFreq	Select generator frequency reference for PLL, standard PR input or from signal space	PR Std or Sg space
TurbRPM	Rated load turbine RPM	0 to 20,000
VoltageDiff	Maximum voltage difference in kV rms for synchronizing	0 to 1,000
FreqDiff	Maximum frequency difference in Hz for synchronizing	0 to 0.5
PhaseDiff	Maximum phase difference in degrees for synchronizing	0 to 30
GenVoltage	Minimum generator voltage in kV rms for synchronizing	1 to 1,000
BusVoltage	Minimum bus voltage in kV rms for synchronizing	1 to 1,000
J4A:IS200TREG	Second TREG board	Connected, not con.
KESTOP2_Fdbk	Emergency stop ESTOP2, inverse sense, K4 relay, True= run - card point	Point edit (Input BIT)
K4_Fdbk	Trip relay 4 feedback (first of 4,5,6) - card point	Point edit (Input BIT)
KE4_Fdbk	Economizing relay for trip solenoid 4 (first of 4,5,6) - card point	Point edit (Input BIT)

Card Points(Signals)	Description–Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG-VPROR	Card Diagnostic	Input	BIT
L3DIAG-VPROS	Card Diagnostic	Input	BIT
L3DIAG-VPROT	Card Diagnostic	Input	BIT
PR1_Zero	L14HP_ZE	Input	BIT
PR2_Zero	L14IP_ZE	Input	BIT
PR3_Zero	L14LP_ZE	Input	BIT
K1_FdbkNVR	Non voted L4ETR1_FB, Trip Relay 1 Feedback R	Input	BIT
K1_FdbkNVS	Non voted L4ETS1_FB, Trip Relay 1 Feedback S	Input	BIT
K1_FdbkNVT	Non voted L4ETT1_FB, Trip Relay 1 Feedback T	Input	BIT
:	:	:	:
K6_FdbkNVR	Non voted L4ETR6_FB, Trip Relay 6 Feedback R	Input	BIT
K6_FdbkNVS	Non voted L4ETS6_FB, Trip Relay 6 Feedback S	Input	BIT
K6_FdbkNVT	Non voted L4ETT6_FB, Trip Relay 6 Feedback T	Input	BIT

Card Points(Signals)	Description–Point Edit (Enter Signal Connection)	Direction	Type
OS1_Trip	L12HP_TP	Input	BIT
OS2_Trip	L12IP_TP	Input	BIT
OS3_Trip	L12LP_TP	Input	BIT
Dec1_Trip	L12HP_DEC	Input	BIT
Dec2_Trip	L12IP_DEC	Input	BIT
Dec3_Trip	L12LP_DEC	Input	BIT
Acc1_Trip	L12HP_ACC	Input	BIT
Acc2_Trip	L12IP_ACC	Input	BIT
Acc3_Trip	L12LP_ACC	Input	BIT
TA_Trip	Trip Anticipate Trip L12TA_TP	Input	BIT
TA_StpLoss	L30TA	Input	BIT
OT_Trip	L26TRP	Input	BIT
MA1_Trip	L3MA_TRP1	Input	BIT
MA2_Trip	L3MA_TRP2	Input	BIT
MA3_Trip	L3MA_TRP3	Input	BIT
SOL1_Vfdbk	When TREG used, Trip Solenoid 1 Voltage detected status	Input	BIT
:	:	Input	BIT
SOL6_Vfdbk	When TREG used, Trip Solenoid 6 Voltage detected status	Input	BIT
L25A_Cmd	L25A Breaker Close Pulse	Input	BIT

The following Input BITs marked config are set by Configuration

Card Points(Signals)	Description–Point Edit (Enter Signal Connection)	Direction	Type
Cont1_TrEnab	Config_Contact 1 Trip Enabled	Input	BIT
:	:	Input	BIT
Cont7_TrEnab	Config -contact 7 trip enabled	Input	BIT
Acc1_TrEnab	Config- accel 1 trip enabled	Input	BIT
Acc2_TrEnab	Config- accel 2 trip enabled	Input	BIT
Acc3_TrEnab	Config- accel 3 trip enabled	Input	BIT
OT_TrEnab	Config – overtemp trip enabled	Input	BIT
GT_1Shaft	Config – gas turb, 1 shaft enabled	Input	BIT
GT_2Shaft	Config – gas turb, 2 shaft enabled	Input	BIT
LM_2Shaft	Config – LM turb, 2 shaft enabled	Input	BIT
LM_3Shaft	Config – LM turb, 3 shaft enabled	Input	BIT
LargeSteam	Config – Large steam 1, enabled	Input	BIT
MediumSteam	Config – medium steam, enabled	Input	BIT
SmallSteam	Config – small steam, enabled	Input	BIT
STag_GT_1S	Config - stag 1 shaft, enabled	Input	BIT
STag_GT_2S	Config - stag 2 shaft, enabled	Input	BIT
ETR1_Enab	Config - ETR1 relay enabled	Input	BIT
:	:	:	:
ETR6_Enab	Config - ETR6 relay enabled	Input	BIT
KE1_Enab	Config - economizing relay 1 enabled	Input	BIT
KE2_Enab	Config - economizing relay 2 enabled	Input	BIT
KE3_Enab	Config - economizing relay 3 enabled	Input	BIT
KE4_Enab	Config - economizing relay 4 enabled	Input	BIT
KE5_Enab	Config - economizing relay 5 enabled	Input	BIT
KE6_Enab	Config - economizing relay 6 enabled	Input	BIT
K4CL_Enab	Config - servo clamp relay enabled	Input	BIT
K25A_Enab	Config - sync check relay enabled	Input	BIT

Card Points(Signals)	Description–Point Edit (Enter Signal Connection)	Direction	Type
L5CFG1_Trip	HP config Trip	Input	BIT
L5CFG2_Trip	IP config Trip	Input	BIT
L5CFG3_Trip	LP config Trip	Input	BIT
OS1_SP_CfgEr	HP overspeed setpoint config mismatch error	Input	BIT
OS2_SP_CfgEr	IP overspeed setpoint config mismatch error	Input	BIT
OS3_SP_CfgEr	LP overspeed setpoint config mismatch error	Input	BIT
ComposTrip1	Composite trip 1	Input	BIT
ComposTrip2	Composite trip 2	Input	BIT
ComposTrip3	Composite trip 3	Input	BIT
L5ESTOP1	ESTOP1 trip, TREG, J3	Input	BIT
L5ESTOP2	ESTOP2 trip, TREG, J4	Input	BIT
L5Cont1_Trip	Contact1 trip	Input	BIT
:	:	Input	BIT
L5Cont7_Trip	Contact7 trip	Input	BIT
LPShaftLock	LP shaft locked	Input	BIT
Inhbt1_Fdbk	Trip inhibit signal feedback for contact 1	Input	BIT
:	:	:	:
Inhbt7_Fdbk	Trip inhibit signal feedback for contact 7	Input	BIT
L3SS_Comm	Valid communications with VCM status	Input	BIT
Trip1_EnCon	Contact1 trip enabled conditional	Input	BIT
:	:	Input	BIT
Trip7_EnCon	Contact7 trip enabled conditional	Input	BIT
BusFreq	Bus frequency SFL 2 Hz	Input	FLOAT
GenFreq	Gen frequency SF 2 Hz	Input	FLOAT
GenVoltsDiff	Gen - bus kV difference rms: gen low is negative	Input	FLOAT
GenFreqDiff	Gen - bus slip Hz: gen slow is negative	Input	FLOAT
GenPhaseDiff	Gen - bus phase difference degrees: gen lag is negative	Input	FLOAT
PR1_Accel	HP accel in RPM/SEC	Input	FLOAT
PR2_Accel	IP accel in RPM/SEC	Input	FLOAT
PR3_Accel	LP accel in RPM/SEC	Input	FLOAT
PR1_Max	HP max speed since last zero speed in RPM (see Vol 1 Chap 8 overspeed protection)	Input	FLOAT
PR2_Max	IP max speed since last zero speed in RPM	Input	FLOAT
PR3_Max	LP max speed since last zero speed in RPM	Input	FLOAT
OTSPBias	Overtemperature setpoint bias	Input	FLOAT
OTSetpoint	Overtemperature setpoint	Input	FLOAT
SynCk_Perm	L25A_PERM – sync check permissive	Output	BIT
SynCk_ByPass	L25A_BYPASS – sync check bypass	Output	BIT
Cross_Trip	L4Z_XTRP – control cross trip	Output	BIT
OnLineOS1Tst	L97HP_TST1 – on line HP overspeed test	Output	BIT
OnLineOS2Tst	L97LP_TST1 – on line HP overspeed test	Output	BIT
OnLineOS3Tst	L97IP_TST1 – on line LP overspeed test	Output	BIT
OffLineOS1Tst	L97HP_TST2 – offline HP overspeed test	Output	BIT
OffLineOS2Tst	L97LP_TST2 – offline IP overspeed test	Output	BIT
OffLineOS3Tst	L97IP_TST2 – offline LP overspeed test	Output	BIT
TrpAntcptTst	L97A_TST – trip anticipate test	Output	BIT
LokdRotorByp	L97LR_BYP – locked rotor bypass	Output	BIT
HPZeroSpdByp	L97ZSC_BYP – HP zero speed check bypass	Output	BIT

Card Points(Signals)	Description–Point Edit (Enter Signal Connection)	Direction	Type
TestETR1	L97ETR1 – ETR1 test, true denergizes relay	Output	BIT
:	:	:	:
TestETR4	L97ETR4 – ETR4 Test, true denergizes relay	Output	BIT
PTR1	L20PTR1 – primary trip relay CMD for diagnostic only	Output	BIT
:	:	:	:
PTR6	L20PTR6 – primary trip relay CMD for diagnostic only	Output	BIT
PR_Max_Rst	Max speed reset (see Vol 1 Chap 8 overspeed protection)	Output	BIT
OnLineOS1X	L43EOST_ONL – online HP overspeed test with auto reset	Output	BIT
Trip1 Inhbt	Contact1 trip inhibit	Output	BIT
:	:	:	:
Trip7 Inhbt	Contact7 trip inhibit	Output	BIT
CJBackup	Estimated TC cold junction temperature in Deg F	Output	FLOAT
OS1_Setpoint	HP overspeed setpoint in RPM	Output	FLOAT
OS2_Setpoint	IP overspeed setpoint in RPM	Output	FLOAT
OS3_Setpoint	LP overspeed setpoint in RPM	Output	FLOAT
OS1_TATrpSp	PR1 overspeed trip setpoint in RPM for trip anticipate Fn	Output	FLOAT
OTBias	Overttemperature bias signal	Output	FLOAT
DriveFreq	Drive (Gen) Freq (Hz), used for non standard drive config.	Output	FLOAT
Speed1	Shaft speed 1 in RPM	Output	FLOAT
ContWdog	Controller watchdog counter	Output	LONG INT

Alarms

Fault	Fault Description	Possible Cause
2	Flash memory CRC failure	Board firmware programming error (board will not go online)
3	CRC failure override is active	Board firmware programming error (board is allowed to go online)
4-15	Reserved for future use	
16	System limit checking is disabled	System checking was disabled by configuration.
17	Board ID failure	Failed ID chip on the VME I/O board
18	J3 ID failure	Failed ID chip on connector J3, or cable problem
19	J4 ID failure	Failed ID chip on connector J4, or cable problem
20	J5 ID failure	Failed ID chip on connector J5, or cable problem
21	J6 ID failure	Failed ID chip on connector J6, or cable problem
22	J3A ID failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware incompatibility	Invalid terminal board connected to VME I/O board
25-29	Reserved for future use	
30	ConfigCompatCode mismatch; firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32-38	Contact input # not responding to test mode trip interlock number # is not reliable	Contact input circuit failure on VPRO or TREG/TREL/TRES board.
39-40	Contact excitation voltage test failure contact excitation voltage has failed, trip interlock monitoring voltage is lost	Loss of P125 voltage caused by disconnection of JH1 to TREG/TREL/TRES, or disconnect of JX1, JY1, JZ1 on TREG/TREL/TRES to J3 on VPRO.

Fault	Fault Description	Possible Cause
41-43	Thermocouple ## raw counts high. The ## thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	A condition such as stray voltage or noise caused the input to exceed +63 mV.
44-46	Thermocouple ## raw counts low. The ## thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	The board detected a thermocouple open and applied a bias to the circuit driving it to a large negative number, or the TC is not connected, or a condition such as stray voltage or noise caused the input to exceed -63 mV.
47	Cold junction raw counts high. Cold junction device input to the A/D converter has exceeded the limits of the converter. Normally two cold junction inputs are averaged; if one is detected as bad then the other is used. If both cold junctions fail, a predetermined value is used	The cold junction device on the terminal board has failed.
48	Cold junction raw counts low. Cold junction device input to the A/D converter has exceeded the limits of the converter	The cold junction device on the terminal board has failed.
49	Calibration reference # raw counts high. Calibration reference # input to the A/D converter exceeded the converter limits. If Cal. Ref. 1, all even numbered TC inputs will be wrong; if Cal. Ref. 2, all odd numbered TC inputs will be wrong	The precision reference voltage on the board has failed.
50	Calibration reference raw counts low. Calibration reference input to the A/D converter exceeded the converter limits	The precision reference voltage on the board has failed.
51	Null reference raw counts high. The null (zero) reference input to the A/D converter has exceeded the converter limits	The null reference voltage signal on the board has failed.
52	Null reference raw counts low. The null (zero) reference input to the A/D converter has exceeded the converter limits	The null reference voltage signal on the board has failed.
53-55	Thermocouple ## linearization table high. The thermocouple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's maximum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong.
56-58	Thermocouple ## linearization table low. The thermocouple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's minimum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the cold junction compensation is wrong.
59-61	Analog Input # unhealthy. The number # analog input to the A/D converter has exceeded the converter limits	The input has exceeded 4-20 mA range, or for input #1 if jumpered for ± 10 V, it has exceeded ± 10 V range, or the 250 Ω burden resistor on TPRO has failed.
63	P15=####.## volts is outside of limits. The P15 power supply is out of the specified +12.75 to +17.25 V operating limits	Analog ± 15 V power supply on VPRO board has failed.
64	N15=####.## volts is outside of Limits. The N15 power supply is out of the specified -17.25 to -12.75 V operating limits	Analog ± 15 V power supply on VPRO board has failed.
65-66	Reserved for future use	
67	P28A=####.## Volts is Outside of Limits. The P28A power supply is out of the specified 23.8 to 31.0 V operating limits	The P28A power supply on VPWR board has failed, otherwise there may be a bad connection at J9, the VPWR to VPRO interconnect.
68	P28B=####.## Volts is Outside of Limits. The P28B power supply is out of the specified 23.8 to 31.0 V operating limits	The P28B power supply on VPWR board has failed, otherwise there may be a bad connection at J9, the VPWR to VPRO interconnect.
69-82	Relay driver feedback does not match the requested state. The state of the command to the relay does not match the state of the relay driver feedback signal; the relay cannot be reliably driven until corrected	The relay driver or relay driver feedback monitor on the TREG/TREL/TRES terminal board has failed, or the cabling between VPRO and TREG/TREL/TRES is incorrect.

Fault	Fault Description	Possible Cause
69-71	Trip Relay (ETR) Driver # Mismatch requested State. Terminal Board 1	See 69-82 above
72-74	Econ Relay Driver # Mismatch Requested State. Terminal Board 1	See 69-82 above
75	Servo Clamp Relay Driver Mismatch (K4CL) Requested State.	See 69-82 above
76	K25A Relay (Synch Check) Driver Mismatch Requested State.	See 69-82 above
77-79	Trip Relay (ETR) Driver # Mismatch requested State. Terminal Board 2	See 69-82 above
80-82	Econ Relay Driver # Mismatch Requested State. Terminal Board 2	See 69-82 above
83-96	Relay contact feedback does not match the requested state. The state of the command to the relay does not match the state of the relay contact feedback signal; the relay cannot be reliably driven until corrected	The relay contact or relay contact feedback monitor on the TREG/TREL/TRES terminal board has failed, or the cabling between VPRO and TREG/TREL/TRES is incorrect.
83-85	Trip Relay (ETR) Contact # Mismatch requested State. Terminal Board 1	See 83-96 above
86-88	Econ Relay Contact # Mismatch Requested State. Terminal Board 1	See 83-96 above
89	Servo Clamp Relay Driver Mismatch (K4CL) Requested State. Terminal Board 1	See 83-96 above
90	K25A Relay (Synch Check) Contact Mismatch Requested State. Terminal Board 1	The K25A relay contact feedback on the TREG/TREL/TRES board has failed, or the K25A relay on TTUR has failed, or the cabling between VPRO and TTUR is incorrect. The state of the command to the K25A relay does not match the state of the K25A relay contact feedback signal; cannot reliably drive the K25A relay until the problem is corrected. The signal path is from VPRO to TREG/TREL/TRES to TRPG/TRPL/TRPS to VTUR to TTUR.
91-93	Trip Relay (ETR) Contact # Mismatch Requested State. Terminal Board 2	See 83-96 above
94-96	Econ Relay Contact # Mismatch Requested State. Terminal Board 2	See 83-96 above
97	TREG/TREL/TRES J3 Solenoid Power Source is Missing. The P125 V dc source for driving the trip solenoids is not detected; cannot reliably drive the trip solenoids	The power detection monitor on the TREG1/TREL1/TRES1 board has failed, or there is a loss of P125 V dc through the J2 connector from TRPG/TRPL/TRPS board, or the cabling between VPRO and TREG1/TREL1/TRES1 or between TREG1/TREL1/TRES1 and TRPG/TRPL/TRPS is incorrect.
98	TREG/TREL/TRES J4 Solenoid Power Source is Missing. The P125 V dc source for driving the trip solenoids is not detected; cannot reliably drive the trip solenoids K4-K6	The power detection monitor on the TREG2/TREL2/TRES2 board has failed, or there is a loss of P125 V dc through the J2 connector from TRPG/TRPL/TRPS board, or the cabling between VPRO and TREG2/TREL2/TRES2 or between TREG2/TREL2/TRES2 and TRPG/TRPS/TRPL is incorrect. Also trip relays K4-K6 may be configured when there is no TREG2/TREL2/TRES2 board.
99-104	TREG/TREL/TRES Solenoid Voltage # Mismatch Requested State. The state of the trip solenoid # does not match the command logic of the voted ETR # on TREG/TREL/TRES, and the voted primary trip relay (PTR) # on TRPG/TRPL/TRPS, the ETR cannot be reliably driven until corrected	The trip solenoid # voltage monitor on TREG/TREL/TRES has failed or ETR # driver failed, or PTR # driver failed. There may be a loss of 125 V dc through the J2 connector from TRPG/TRPL/TRPS, which has a separate diagnostic. See (105-107)
105	TREL/TRES, J3, Solenoid Power, Bus A, Absent. The voltage source for driving the solenoids is not detected on Bus A; cannot reliably drive these solenoids	Loss of power bus A through J2 connector from TRPL/TRPS
106	TREL/TRES, J3, Solenoid Power, Bus B, Absent. The voltage source for driving the solenoids is not detected on Bus B; cannot reliably drive these solenoids	Loss of power bus B through J2 connector from TRPL/TRPS

Fault	Fault Description	Possible Cause
107	TREL/TRES, J3, Solenoid Power, Bus C, Absent. The voltage source for driving the solenoids is not detected on Bus C; cannot reliably drive these solenoids	Loss of Power Bus C through J2 connector from TRPL/TRPS
108	Control Watchdog Trip Protection This alarm can only occur if Configuration -> ContWdogEn has been enabled. An alarm indicates that the signal space point -> ContWdog has not changed for 5 consecutive frames. The alarm will reset itself if changes are seen for 60 seconds.	Verify that the ContWdog is set up correctly in the toolbox and that the source of the signal is changing the value at least once a frame. Check Ethernet cable and connections.
109	Speed Difference Trip Protection This alarm can only occur if Configuration -> SpeedDifEnable has been enabled. An alarm indicates that the difference between the output signal Internal Points -> Speed1 and the first VPRO pulse rate speed is larger than the percentage Configuration -> OS_DIFF for more than 3 consecutive frames. The alarm will reset itself if the difference is within limits for 60 seconds.	Verify that the Speed1 signal is set up correctly in the toolbox and that the source of the signal reflects the VTUR pulse rate speed. Check Ethernet cable and connections.
110	Stale speed trip protection. This alarm can only occur if Configuration -> StaleSpdEn has been enabled. An alarm indicates that the signal Internal Points -> Speed1 has not changed for 5 consecutive frames. The alarm will reset itself if the speed dithers for 60 seconds.	Verify that the Speed1 signal is set up correctly in the toolbox and that the source of the signal reflects the VTUR pulse rate speed input. Check Ethernet cable and connections.
111-127	Reserved for future use	
128-319	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
320-339	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TPRO Emergency Protection

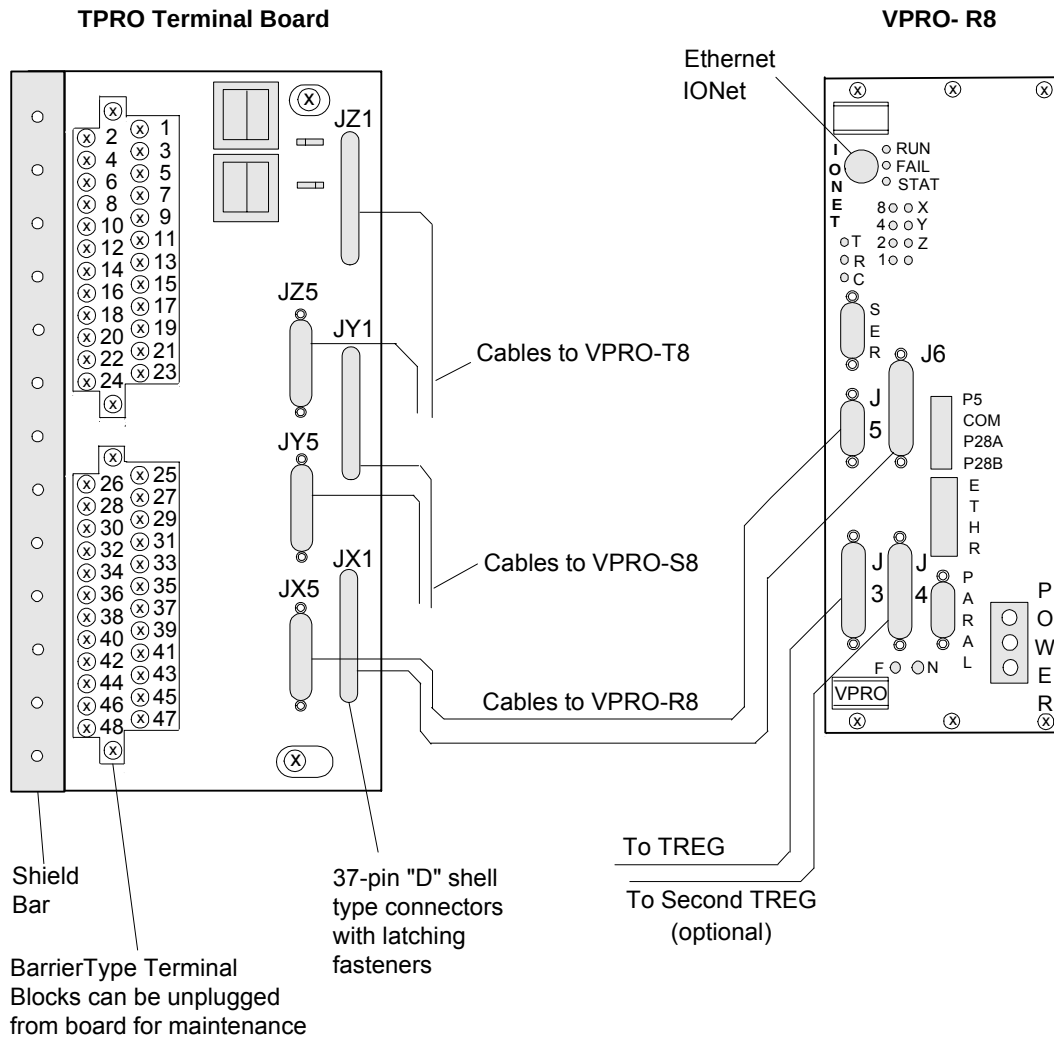
Functional Description

The Emergency Protection (TPRO) terminal board provides the VPRO with speed signals, temperature signals, generator voltage, and bus voltage as part of an independent emergency overspeed and synchronization protection system. The protection system consists of triple redundant VPRO boards in a module separate from the turbine control system, controlling the trip solenoids through TREx (TREG, or TREL, or TRES). TPRO supplies inputs to all three VPRO boards. The following figure shows the cabling to VPRO from the TPRO and TREx terminal boards.

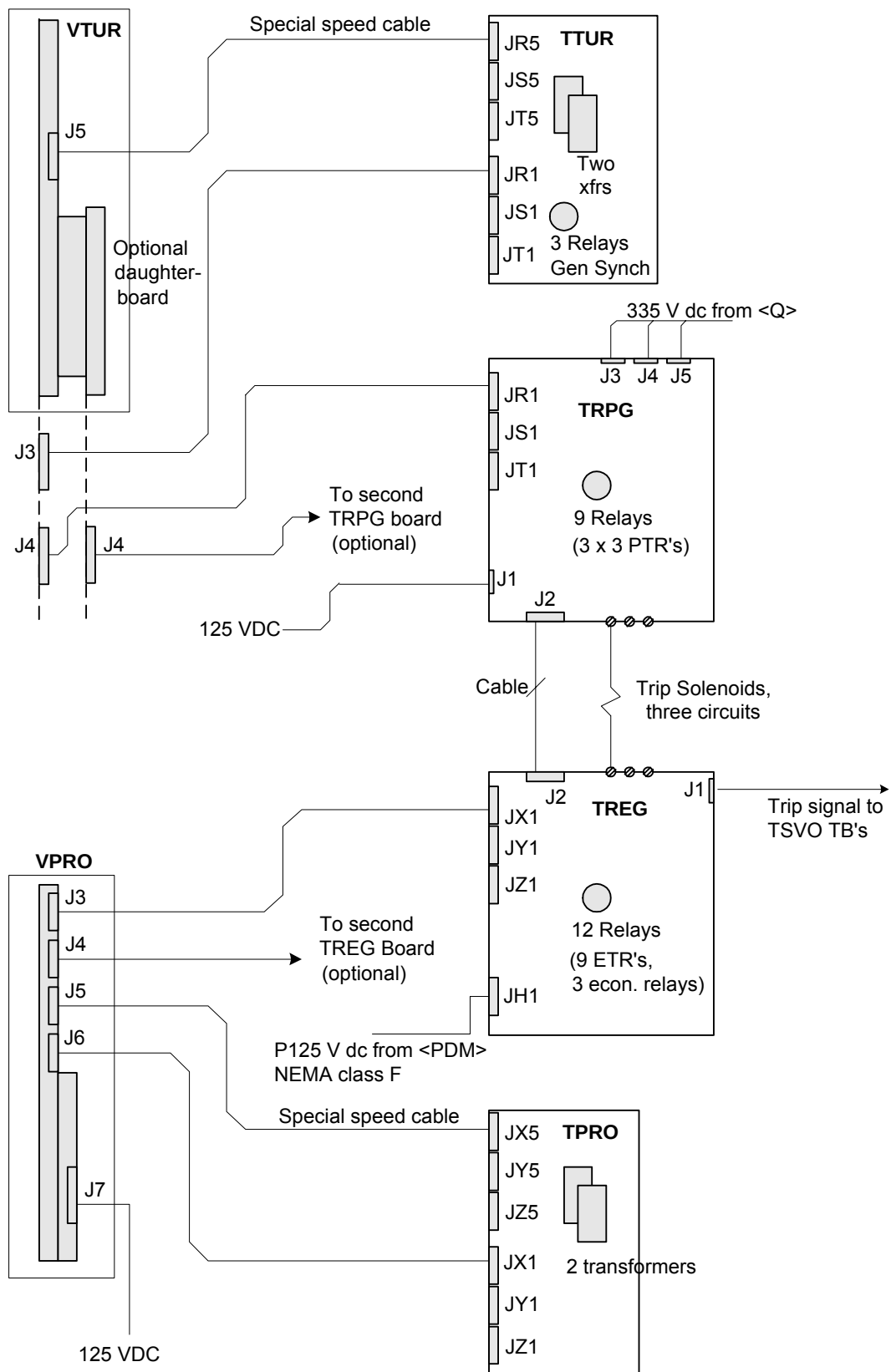
The VPRO board provides the emergency trip function. Up to three trip solenoids can be connected between the TREx and TRPx (TRPG, or TRPL, or TRPS) terminal boards. TREx provides the positive side of the 125 V dc to the solenoids and TRPx provides the negative side. Either board can trip the turbine. VPRO provides emergency overspeed protection and the emergency stop functions. It controls the 12 relays on TREG, nine of which form three groups of three to vote inputs controlling the three trip solenoids. A second TREG board may be driven from VPRO through J4.

Note TPRO does not work with the Mark* VIe I/O packs.

The following figure shows how the VTUR and VPRO boards share in a gas turbine protection scheme. Both detect turbine overspeed, and either one can independently trip the turbine using the relays on TRPG or TREG.



TPRO Terminal Board, VPRO Board, and Cabling

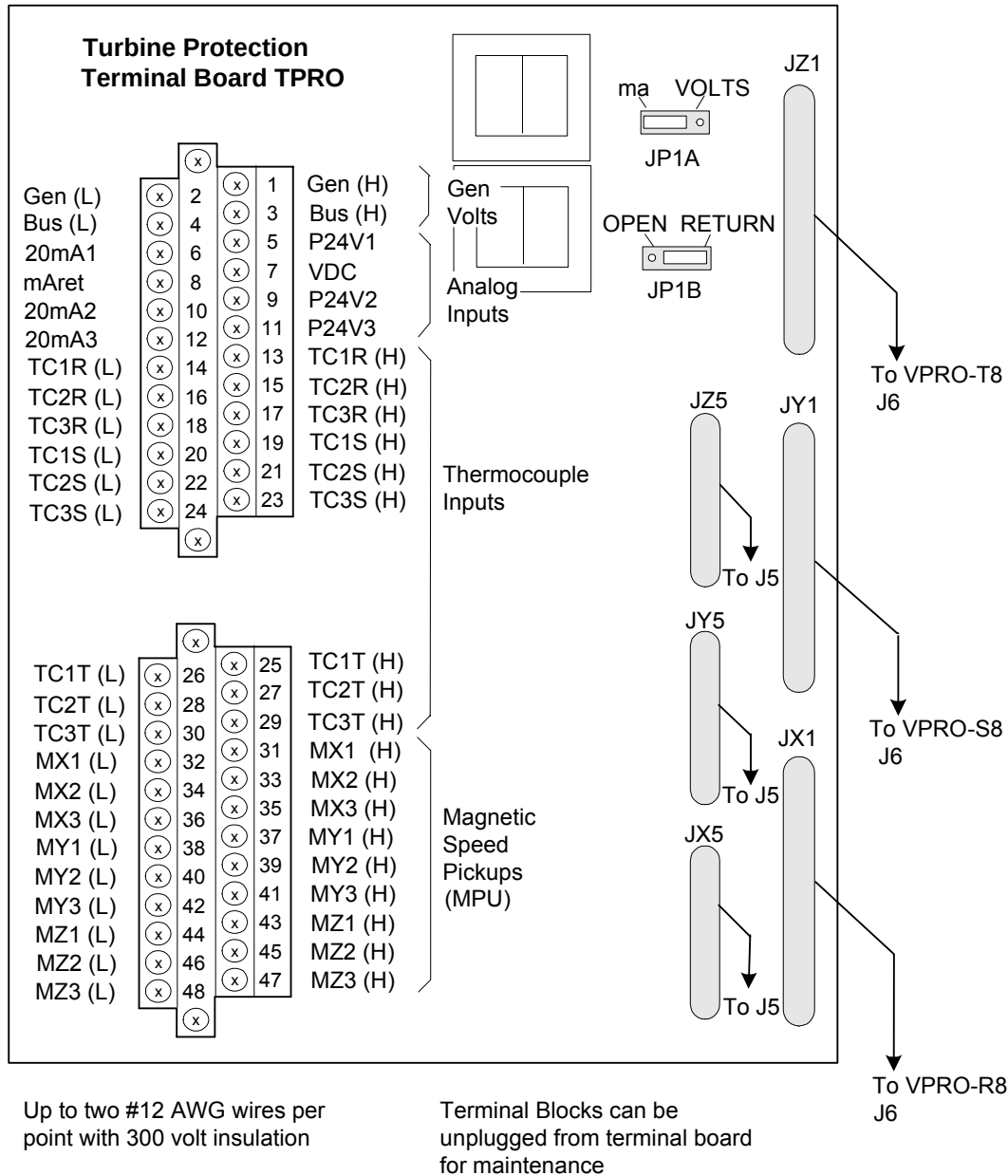


Turbine Control and Protection Boards, Gas Turbine Control Example

Installation

The generator and bus potential transformers, analog inputs, and thermocouples are wired to the first terminal block on TPRO. The magnetic speed pickups are wired to the second block. Jumpers JP1A and JP1B are set to give either a 4-20 mA or voltage input on the first of the three analog inputs.

The wiring connections are shown in the following figure. Two cables go to each of the three VPRO boards.



TPRO Wiring and Cabling

Operation

The main purpose of the TPRO is to supply speed signals to VPRO for the emergency overspeed (EOS) protection for the turbine. In addition, TPRO supplies generator signals for backup synchronization check protection, three analog current inputs, and nine thermocouple inputs, primarily for exhaust over-temperature protection on gas turbines. VPRO provides 28 V dc to TPRO to power the three analog input transmitters.

Speed Control and Overspeed Protection

Speed control and overspeed protection is implemented with six passive, magnetic speed pickups. The first three are monitored by the controller, which uses the median signal for speed control and the primary overspeed protection. The second three are separately connected to the three VPROs in the protection module. Provision is made for nine passive magnetic speed pickups or active pulse rate transducers (TTL type) on the TPRO terminal board, with three being monitored by each of the three VPROs.

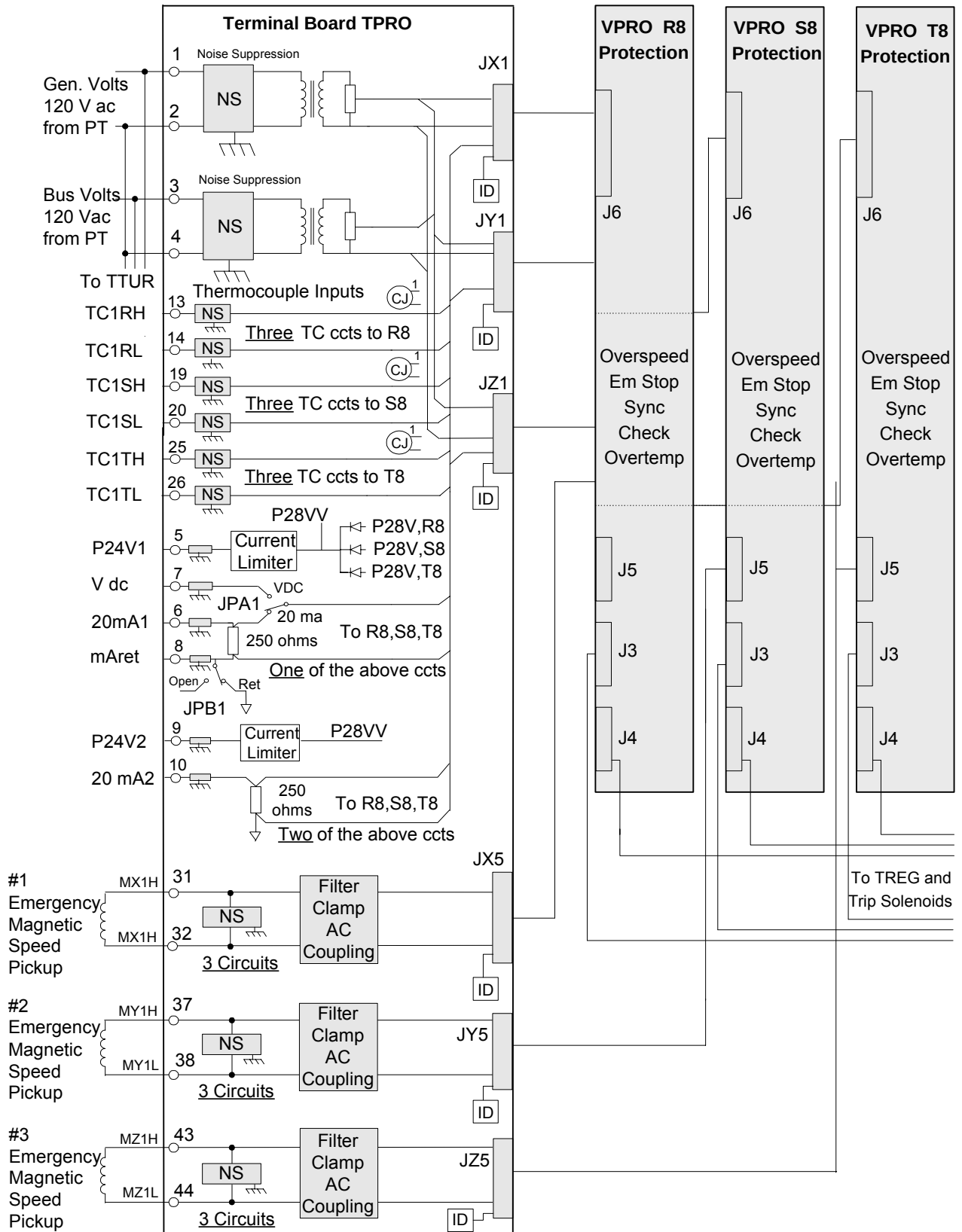
Backup Synch Check Protection

TPRO provides inputs to the protection module for backup synchronization check. The generator and bus voltages are supplied from two, single phase, potential transformers (PTs) secondary output supplying a nominal 115 V rms. The maximum cable length between the PTs and the turbine control is 100 meters of 18 AWG twisted, shielded wire. Each PT is magnetically isolated with a 1,500 V rms rated barrier and a circuit load less than 3 VA.

Each PT input is internally connected in parallel through TPRO to the three VPROs in the protection module. The triple redundant phase slip windows result in a voted logical output on the TREG terminal board, which drives the K25A relay. This relay's contacts are connected in series with the synch permissive relay (K25P) and the auto synch relay (K25) to insure that no false command is issued to close the generator breaker. Similarly, contacts from the K25A contact are connected in series with the contacts from remote, manual synchronizing equipment to insure no false commands.

Thermocouple and Analog Inputs

TPRO provides thermocouple and analog inputs to the protection module, primarily for gas turbine applications. Nine thermocouple inputs are monitored with three connected to each VPRO. These are generally used for backup exhaust over-temperature protection. Also, one ± 5 , 10 V dc, 4-20 mA input, and two 4-20 mA inputs can be connected to the TPRO terminal board, which feeds the inputs in parallel to the three VPROs.



TPRO Terminal Board and TMR VPROs

Specifications

Item	Specification
Number of Inputs	9 Passive proximity probes for speed pickups 1 Generator and 1 Bus Voltage 9 Thermocouples 1 4-20 mA current or voltage 2 4-20 mA current
Power Supply Voltage	Input supply 28 V dc for the analog sensors
Magnetic Pickup (MPU) Characteristics	Output resistance 200 ohms with inductance of 85 mH. Output generates 150 V p-p into 60 K ohms at the TPRO terminal block, with insufficient energy for a spark. The maximum short circuit current is approximately 100 mA. The system applies up to 400 ohm normal mode load to the input signal to reduce the voltage at the terminals.
MPU Cable	Sensors can be up to 300 m (984 ft) from the cabinet, assuming that shielded pair cable is used, with typical 70 nF single ended or 35 nF differential capacitance, and 15 ohms resistance.
MPU Pulse Rate Range	2 Hz to 20 kHz
MPU Input Circuit Sensitivity	Minimum signal is 27 mV pk at 2 Hz Minimum signal is 450 mV pk at 14 kHz
Generator and Bus Voltage Sensors	Two Single-Phase Potential Transformers, 115 V rms secondary. Voltage accuracy is 0.5% of rated Volts rms. Frequency Accuracy 0.05%. Phase Difference Measurement better than 1 degree. Allowable voltage range for synchronizing is 75 to 130 V rms. Each input has a load of less than 3 VA.
Thermocouple Inputs	Same specifications as for VTCC board
Analog Inputs	2 current inputs, 4-20 mA 1 current input with selection of 4-20 mA, or ± 5 V dc, or ± 10 V dc. Same specifications as for VAIC board.
Size	17.8 cm Wide x 33.02 cm High (7.0 in x 13 in)

Diagnostics

VPRO makes diagnostic checks on TPRO and its cables and input signals as follows:

- If high or low limits on analog inputs are exceeded a fault is created.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VPROR (or S, or T) occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy.

Terminal board connectors on TPRO have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VPRO and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Configuration of the terminal board is by means of jumpers. For location of these jumpers refer to the *Installation* diagram. The jumper choices are as follows:

- Jumper JPA1 selects either current input or voltage input
- Jumper JPB1 selects whether the return is connected to common or is left open

All other configuration is for VPRO and is done from the toolbox.

TREG Turbine Emergency Trip

Functional Description

The Gas Turbine Emergency Trip (TREG) terminal board provides power to three emergency trip solenoids and is controlled by the I/O controller. Up to three trip solenoids can be connected between the TREG and TRPG terminal boards. TREG provides the positive side of the dc power to the solenoids and TRPG provides the negative side. The I/O controller provides emergency overspeed protection, emergency stop functions, and controls the 12 relays on TREG, nine of which form three groups of three to vote inputs controlling the three trip solenoids.

There are a number of board types as follows:

- The H1A version is not used for new production and is replaced by H1B.
- H1B is the primary version for 125 V dc applications. Control power from the JX1, JY1, and JZ1 connectors are diode combined to create redundant power on the board for status feedback circuits and powering the economizing relays. Power separation is maintained for the trip relay circuits.
- H2B is used for 24 V dc applications. All other features are the same as H1B.
- H3B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JX1 connector.
- H4B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JY1 connector.
- H5B is a special version of H1B for use in systems with redundant TREG boards. Feedback circuit and economizing relay power is provided only by the JZ1 connector.

In redundant TREG applications, it is typical to find one H3B and one H4B board used together. It is important that system repairs be done with the correct board type to maintain the control power separation designed into these systems.

Mark VI Systems

In Mark* VI systems, the VPRO works with the TREG terminal board. Cables with molded plugs connect TREG to the VPRO module.

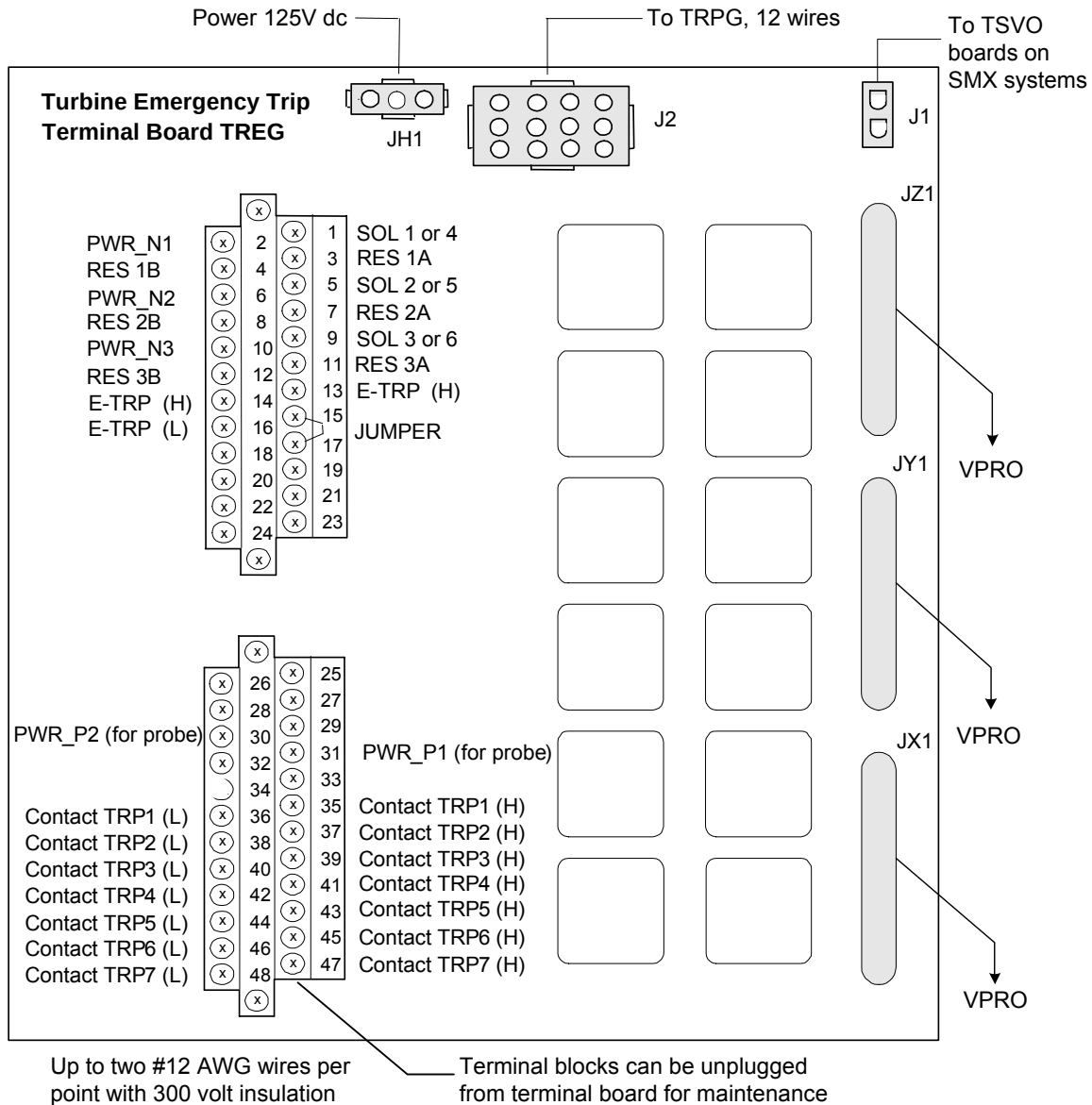
Mark VIe Systems

In Mark VIe systems, TREG is controlled by the PPRO pack on SPRO. The PPRO I/O packs plug into the D-type connectors on SPRO. Cables with molded plugs connect TREG to the SPRO board.

Installation

The three trip solenoids, economizing resistors, and the emergency stop are wired directly to the first I/O terminal block. Up to seven trip interlocks can be wired to the second terminal block. The wiring connections are shown in the following figure.

Note TREGH2B is a 24 V dc version of the terminal board.



TREG Terminal Board Wiring

Operation

TREG is entirely controlled by the VPRO protection module, and the only connections to the control modules are the J2 power cable and through the trip solenoids. In simplex systems a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

Control of Trip Solenoids

Both TRPG and TREG control the trip solenoids so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. The nine trip relay coils on TREG are supplied with 28 V dc from the I/O controller. The trip solenoids are supplied with 125 V dc through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

Note The solenoid circuit has a metal oxide varistor (MOV) for current suppression and a 10 Ω , 70 W economizing resistor.

A separately fused 125 V dc feeder is provided from the turbine control for the solenoids, which energize in the run mode and de-energize in the trip mode. Diagnostics monitor each 125 V dc feeder from the power distribution module at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Two series contacts from each emergency trip relay (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each primary trip relay (PTR1,2,3 in TRPG) are connected to the negative 125 V dc feeder for each solenoid. An economizing relay (KE1, 2, 3) is supplied for each solenoid with a normally closed contact in parallel with the current limiting resistor. These relays are used to reduce the current load after the solenoids are energized. The ETR and KE relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The 28 V dc bus is current limited and used for power to an external manual emergency trip contact, shown as E-STOP. Three master trip relays (K4X, K4Y, K4Z) disconnect the 28 V dc bus from the ETR, and KE relay coils if a manual emergency trip occurs. Any trip that originates in either the protection module (such as EOS) or the TREG (such as a manual trip) will cause each of the three protection module sections to transmit a trip command over the IONet to the control module, and may be used to identify the source of the trip.

In addition, the K4CL servo clamp relay will energize and send a contact feedback directly from the TREG terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

Note The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

Specifications

Item	Specification
Number of trip solenoids	Three solenoids per TREG (total of six per I/O controller)
Trip solenoid rating	H1 - 125 V dc standard with 1 A draw H2 - 24 V dc is alternate with 1 A draw
Trip solenoid circuits	Circuits rated for NEMA class E creepage and clearance Circuits can clear a 15 A fuse with all circuits fully loaded
Solenoid inductance	Solenoid maximum L/R time constant is 0.1 second
Suppression	MOV across the solenoid
Relay outputs	Three economizer relay outputs, two second delay to energize Driver to breaker relay K25A on TTUR Servo clamp relay on TSVO
Solenoid control relay contacts	Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A Bus voltage can vary from 70 to 145 V dc
Trip inputs	Seven trip interlocks to the I/O controller protection module, 125/24 V dc One emergency stop hard wired trip interlock, 24 V dc
Trip interlock excitation	H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc
Trip interlock current	H1 for 125 V dc applications: Circuits draw 2.5 mA (50 Ω) H2 for 24 V dc applications: Circuits draw 2.5 mA (10 Ω)
Trip interlock isolation	Optical isolation to 1500 V on all inputs
Trip interlock filter	Hardware filter, 4 ms
Trip interlock ac voltage rejection	60 V rms @ 50/60 Hz at 125 V dc excitation
Size	17.8 cm wide x 33.02 cm, high (7.0 in x 13.0 in)

Diagnostics

The I/O controller runs diagnostics on the TREG board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, economizer relay driver and contact feedbacks, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value then a fault is created.

TREG connectors JX1, JY1, and JZ1 have their own ID device that is interrogated by I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O board and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no switches on the terminal board.

Note A jumper must be placed across terminals 15 and 17 if the second emergency stop input is not required.

TRES Turbine Emergency Trip

Functional Description

The Small Steam Turbine Emergency Trip (TRES) terminal board is used for the emergency overspeed protection for small/medium size steam turbines. TRES is controlled by the VPRO protection module, and provides power to three emergency trip solenoids, which can be connected between the TRES and TRPS terminal boards. TRES provides the positive side of the 125 V dc to the solenoids and TRPS provides the negative side. The VPRO provides emergency overspeed protection, emergency stop functions, and controls the three relays on TRES, which control the three trip solenoids.

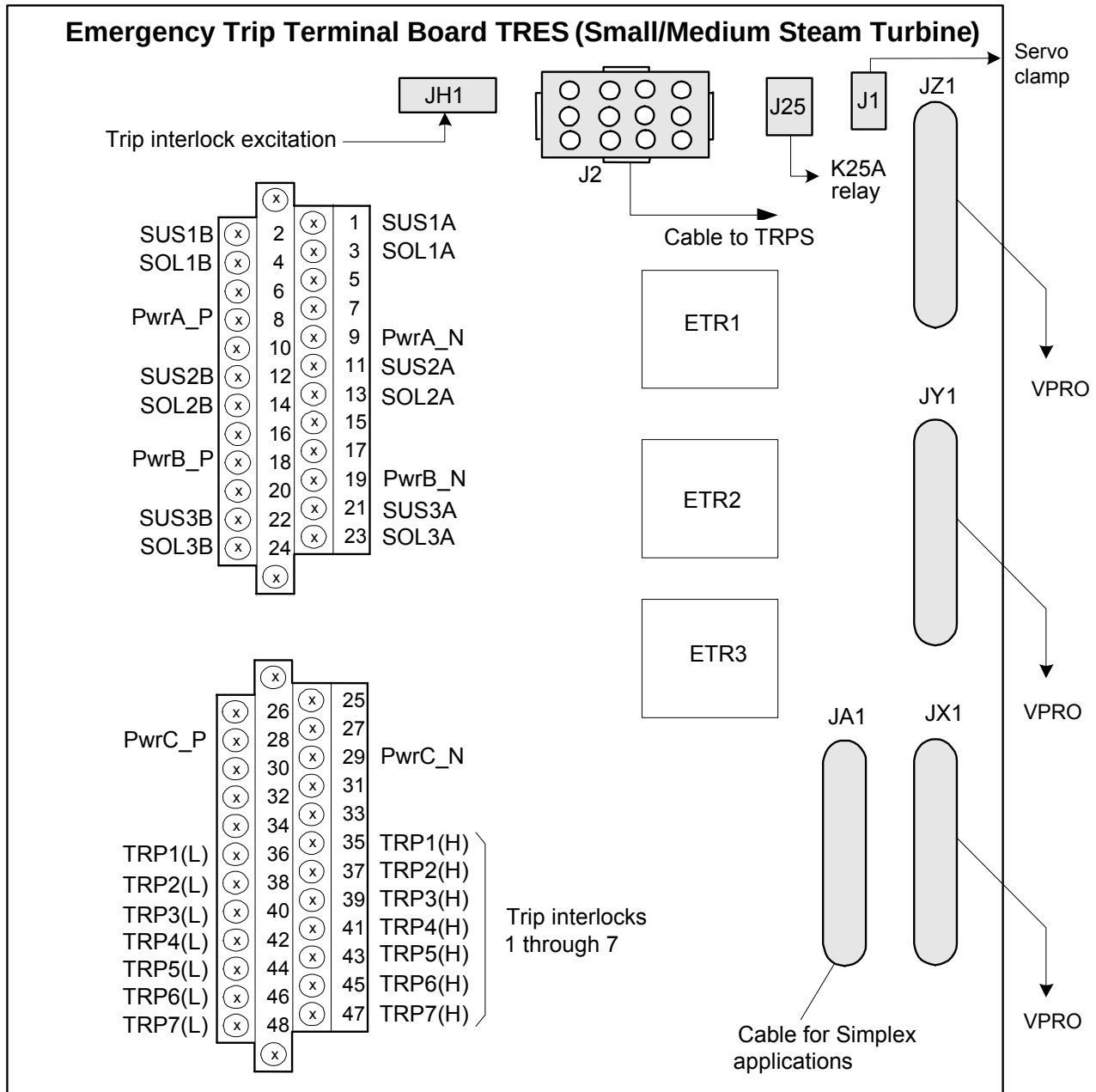
- TRES has both simplex and TMR form.
- There are seven dry contact inputs for trip interlocks.
- TRES has no economizing relays.
- There are no emergency stop inputs.

In the TRES, the seven dry contact inputs excitation and signal are monitored and fanned to the protection module. The board includes the synch check relay driver, K25A, and associated monitoring, the same as on TREG, and the servo clamp relay driver, K4CL, and its associated monitoring. A second TRES board cannot be driven from the protection module.

Installation

The three trip solenoids are wired to the first I/O terminal block. Up to seven trip interlocks are wired to the second terminal block. The wiring connections are shown in the following figure.

Connector J2 carries three power buses from TRPS, and JH1 carries the excitation voltage for the seven trip interlocks.



TRES Terminal Board Wiring

Operation

The VSVO protection module controls TRES. In simplex systems, a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

Control of Trip Solenoids

Both TREL and TRES control the trip solenoids 1 and 2 so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. ETR3 is set up to supply power to trip solenoid #3. The nine trip relay coils on TRES are supplied with 28 V dc from the I/O controller. The trip solenoids are supplied with 125 V dc (or 24 V dc) through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

Note The solenoid circuit has an MOV for current suppression on TREL.

A separately fused 125 V dc feeder is provided from the PDM for the solenoids. Diagnostics monitor each 125 V dc feeder from the PDM at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Note A normally closed contact from each relay is used to sense the relay status for diagnostics

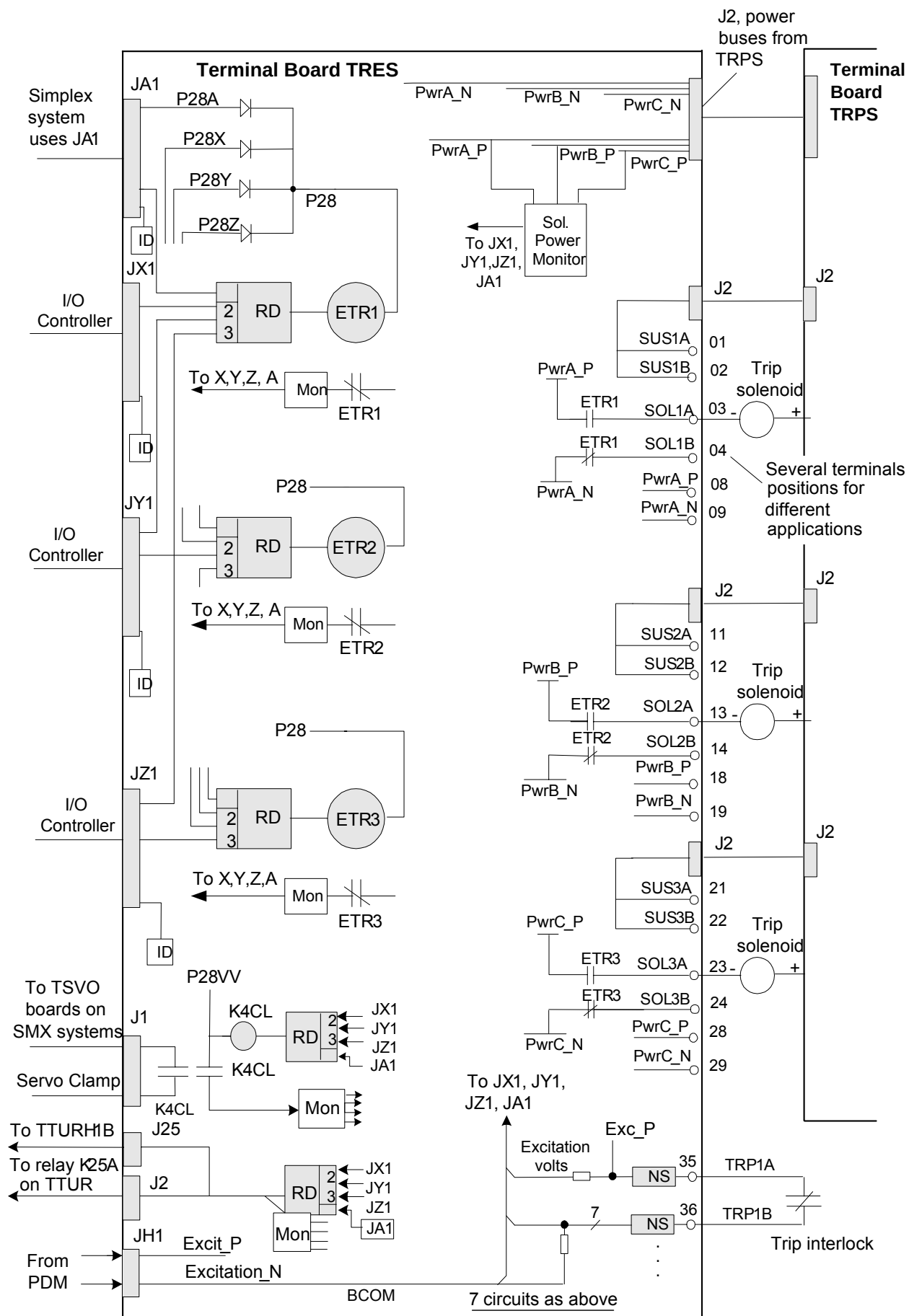
Two series contacts from each of the emergency trip relays (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each of the primary trip relays are connected to the negative 125 V dc feeder for each solenoid. The ETR relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The K4CL servo clamp relay will energize and send a contact feedback directly from the TRES terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

Note The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

Solenoid Trip Tests

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time, either through the PTR relays from the controller, or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.



TRES Terminal Board, Trip Interlocks, and Trip Solenoids

Specifications

Item	Specification
Number of trip solenoids	Three solenoids per TRES
Trip solenoid rating	125 V dc standard with 1 A draw 24 V dc is alternate with 3 A draw
Trip solenoid circuits	Circuits rated for NEMA class E creepage and clearance Circuits can clear a 15 A fuse with all circuits fully loaded
Solenoid inductance	Solenoid maximum L/R time constant is 0.1 sec
Suppression	MOV on TRPS across the solenoid
Relay Outputs	Driver to breaker relay K25A on TTUR Servo clamp relay on TSVO
Solenoid control relay contacts	Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A. Bus voltage can vary from 70 to 145 V dc.
Trip inputs	Seven trip interlocks to VPRO protection module
Trip interlock excitation	H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc
Trip interlock current	H1 for 125 V dc applications: Circuits draw 2.5 mA (50 Ω) H2 for 24 V dc applications: Circuits draw 2.5 mA (10 Ω)
Trip interlock isolation	Optical isolation to 1500 V on all inputs
Trip interlock filter	Hardware filter, 4 ms
Trip interlock ac voltage rejection	60 V rms @ 50/60 Hz at 125 V dc excitation
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)

Diagnostics

The I/O controller runs diagnostics on the TRES board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value, a fault is created.

TRES connectors JA1, JX1, JY1, and JZ1 have their own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

TREL Turbine Emergency Trip

Functional Description

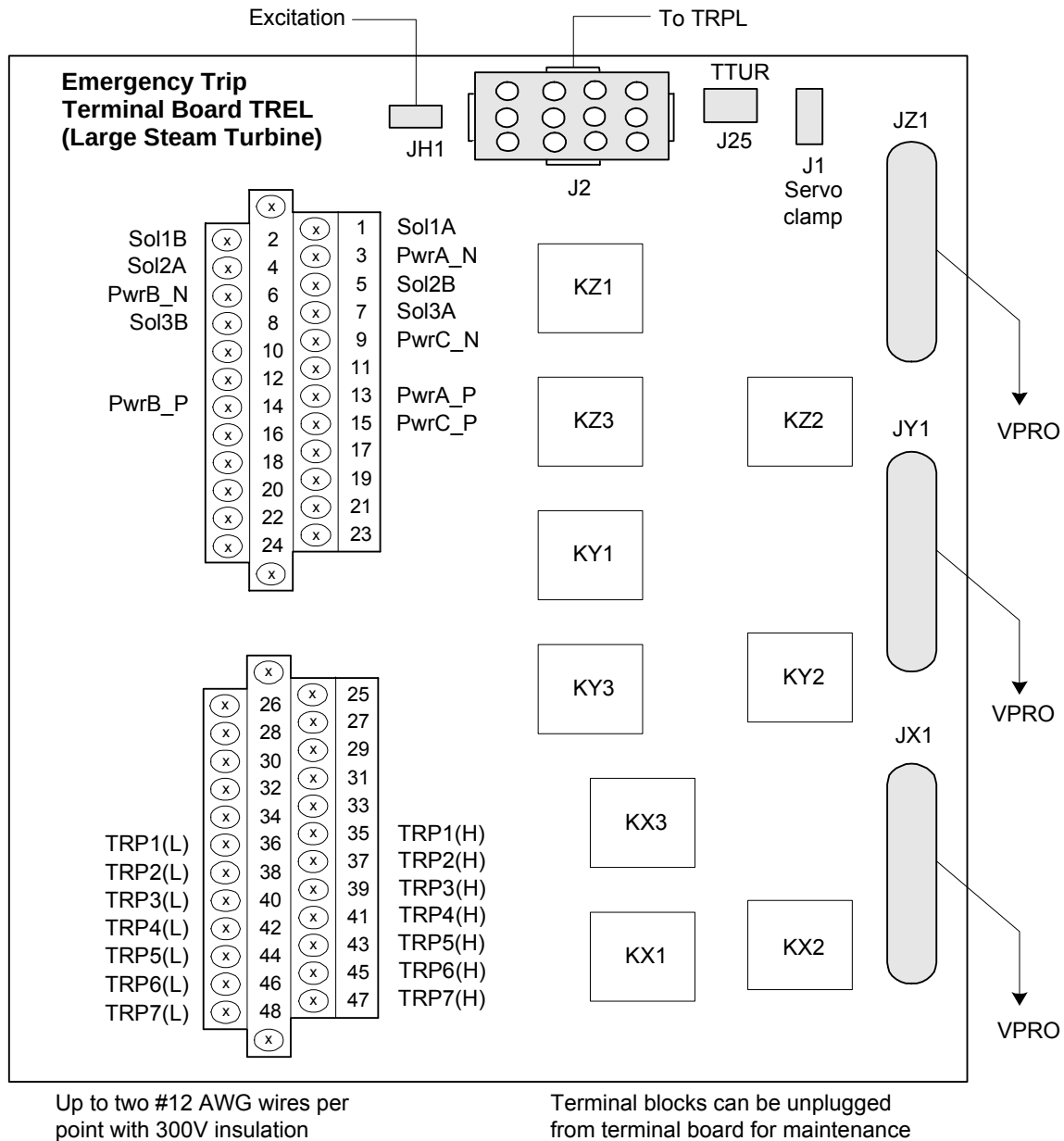
The Large Steam Turbine Emergency Trip (TREL) terminal board is used for the emergency overspeed protection for large steam turbines. TREL is controlled by the VPRO in the protection module, and provides power to three emergency trip solenoids, which can be connected between the TREL and TRPL terminal boards. TREL provides the positive side of the 125 V dc to the solenoids and TRPL provides the negative side. I/O controller provides emergency overspeed protection, emergency stop functions, and controls the nine relays on TREL, which form three groups of three to vote inputs controlling the three trip solenoids. The three groups are called ETR (emergency trip) 1, 2, and 3.

- TREL is only available in TMR form.
- TREL has no economizing relay as with TREG.
- TREL has no E-STOP function as with TREG.

A second TREL board may be driven from the protection module.

Installation

The three trip solenoids are wired to the first I/O terminal block. Up to seven trip interlocks are wired to the second terminal block. The wiring connections are shown in the following figure. Connector J2 carries three power buses from TRPL, and JH1 carries the excitation voltage for the seven trip interlocks.



TREL Terminal Board Wiring

Operation

TREL is entirely controlled by the VPRO protection module, and the only connections to the turbine control are the J2 power cable and the trip solenoids. In simplex systems, a third cable carries a trip signal from J1 to the TSVO terminal board, providing a servo valve clamp function upon turbine trip.

Control of Trip Solenoids

Both TRPL and TREL control the trip solenoids 1 and 2 so that either one can remove power and actuate the hydraulics to close the steam or fuel valves. ETR3 is set up to supply power to trip solenoid #3. The nine trip relay coils on TREL are supplied with 28 V dc from I/O controller. The trip solenoids are supplied with 125 V dc (or 24 V dc) through plug J2, and draw up to 1 A with a 0.1 second L/R time constant.

Note The solenoid circuit has an MOV for current suppression on TRPL.

A separately fused 125 V dc feeder is provided from the PDM to the solenoids. Diagnostics monitor each 125 V dc feeder from the PDM at its point of entry on the terminal board to verify the fuse integrity and the cable connection.

Note A normally closed contact from each relay is used to sense the relay status for diagnostics.

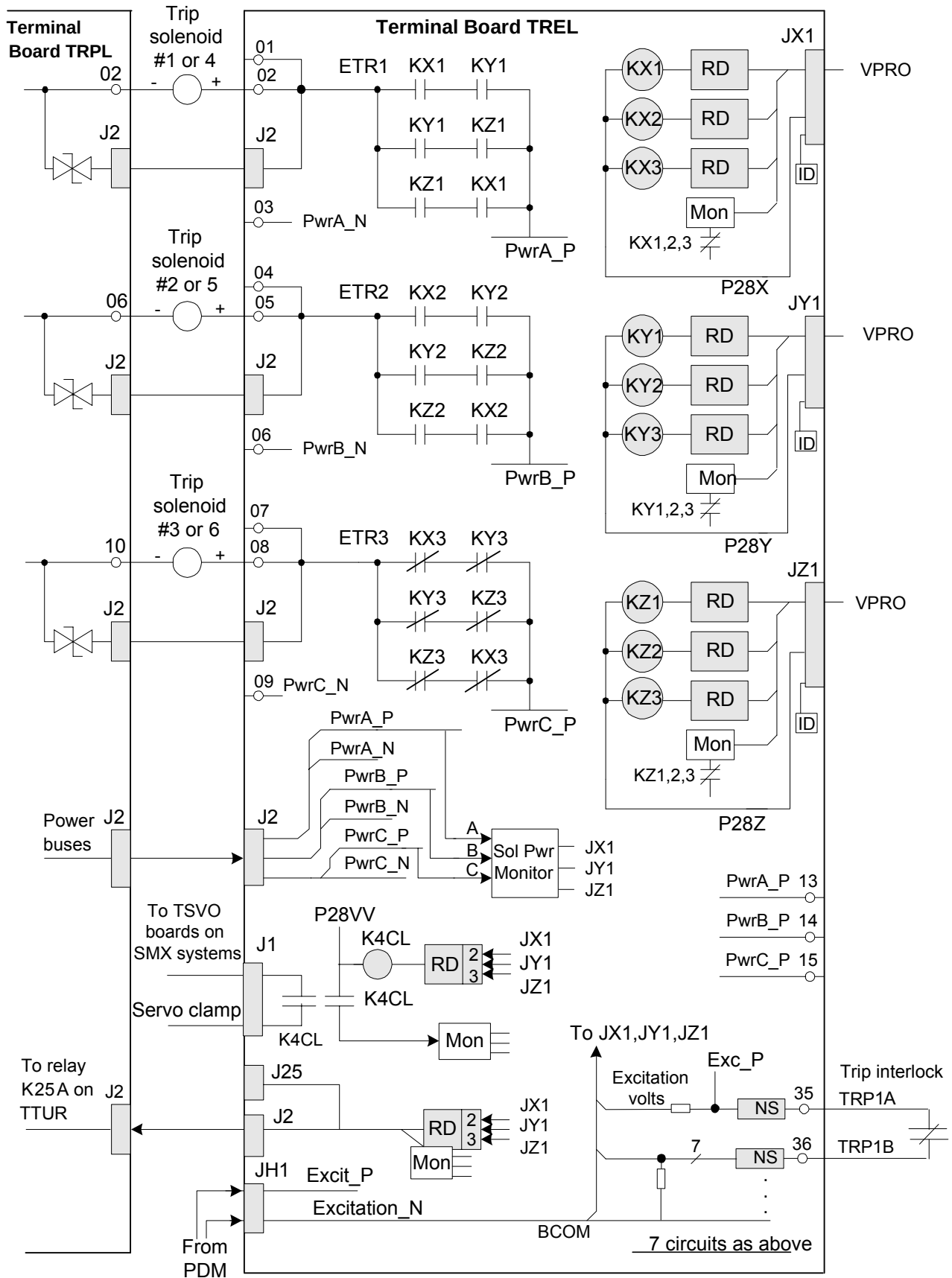
Two series contacts from each of the emergency trip relays (ETR1, 2, 3) are connected to the positive 125 V dc feeder for each solenoid, and two series contacts from each of the primary trip relays are connected to the negative 125 V dc feeder for each solenoid. The ETR relay coils are powered from a 28 V dc source from the I/O controller. Each I/O controller in each of the R8, S8, and T8 sections supplies an independent 28 V dc source.

The K4CL servo clamp relay will energize and send a contact feedback directly from the TREL terminal board to the TSVO servo terminal board. TSVO disconnects the servo current source from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high.

Note The primary and emergency overspeed systems will trip the hydraulic trip solenoids independent of this circuit.

Solenoid Trip Tests

Application software in the controller is used to initiate tests of the trip solenoids. Online tests allow each of the trip solenoids to be manually tripped one at a time, either through the PTR relays from the controller, or through the ETR relays from the protection module. A contact from each solenoid circuit is wired back as a contact input to give a positive indication that the solenoid has tripped. Primary and emergency offline overspeed tests are provided too for verification of actual trips due to software simulated trip overspeed conditions.



TREL Terminal Board, Trip Interlocks, and Trip Solenoids

Specifications

Item	Specification
Number of trip solenoids	Three solenoids per TREL (total of six per I/O controller)
Trip solenoid rating	H1 - 125 V dc standard with 1 A draw H2 - 24 V dc is alternate with 3 A draw
Trip solenoid circuits	Circuits rated for NEMA class E creepage and clearance Circuits can clear a 15 A fuse with all circuits fully loaded
Solenoid inductance	Solenoid maximum L/R time constant is 0.1 sec
Suppression	MOV on TRPL across the solenoid
Relay Outputs	Driver to breaker relay K25A on TTUR. Servo clamp relay on TSVO
Solenoid control relay contacts	Contacts are rated to interrupt inductive solenoid loads at 125 V dc, 1 A. Bus voltage can vary from 70 to 145 V dc
Trip inputs	Seven trip interlocks to the I/O controller protection module, 125/24 V dc
Trip interlock excitation	H1 - Nominal 125 V dc, floating, ranging from 100 to 145 V dc H2 - Nominal 24 V dc, floating, ranging from 18.5 to 32 V dc
Trip interlock current	H1 for 125 V dc applications: Circuits draw 2.5 mA (50 Ω) H2 for 24 V dc applications: Circuits draw 2.5 mA (10 Ω)
Trip interlock isolation	Optical isolation to 1500 V on all inputs
Trip interlock filter	Hardware filter, 4 ms
Trip interlock ac voltage rejection	60 V rms @ 50/60 Hz at 125 V dc excitation
Size	17.8 cm wide x 33.02 cm high (7.0 in x 13.0 in)

Diagnostics

The protection module runs diagnostics on the TREL board and connected devices. The diagnostics cover the trip relay driver and contact feedbacks, solenoid voltage, K25A relay driver and coil, servo clamp relay driver and contact feedback, and the solenoid voltage source. If any of these do not agree with the desired value, a fault is created.

TREL connectors JX1, JY1, and JZ1 have their own ID device that is interrogated by the I/O controller. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by the I/O controller and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

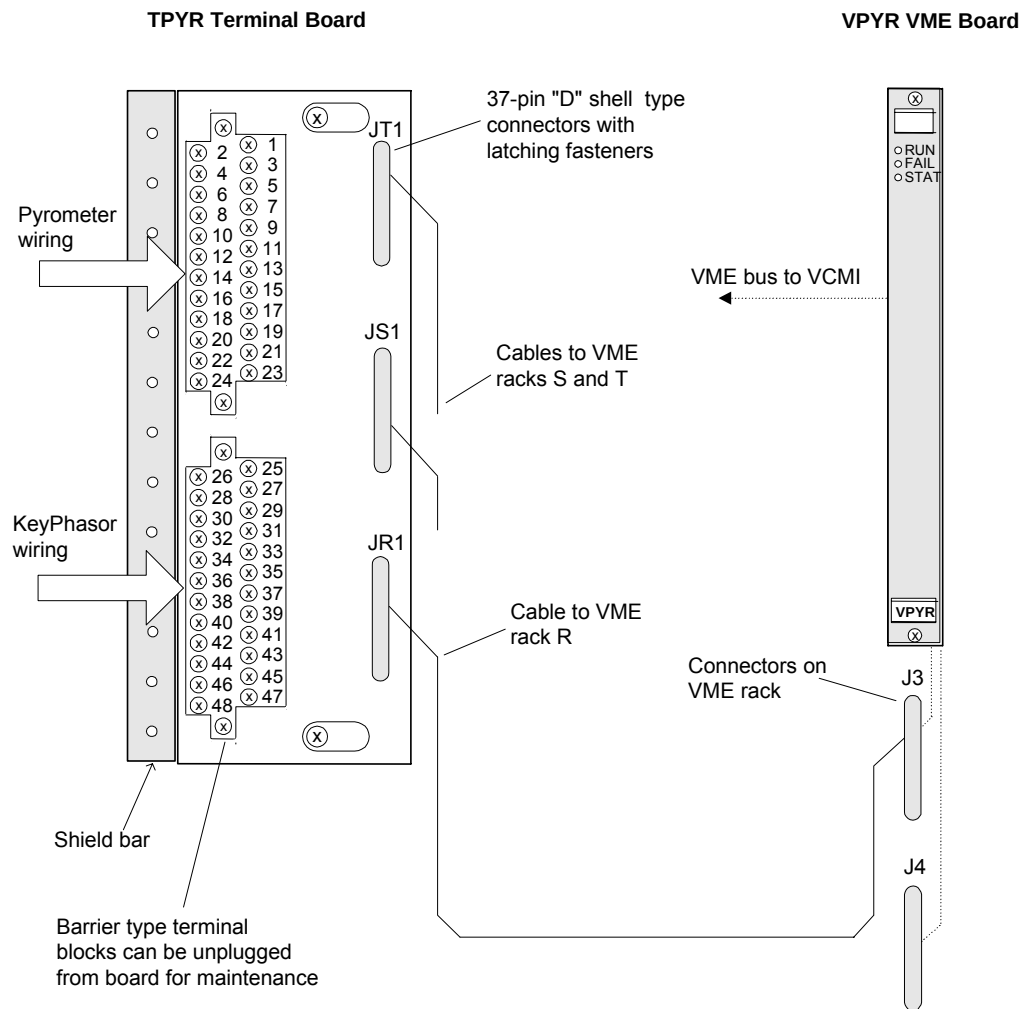
Notes

VPYR Pyrometer Board

VPYR Pyrometer Input

Functional Description

The Pyrometer Input (VPYR) board provides a dynamic temperature profile of the rotating turbine blades and computes temperature conditions that can lead to a trip. Two infrared turbine blade temperature measurement system (TBTMS) thermometers, known as pyrometers, and two Keyphasor[®] Proximator[®] probes for shaft reference are wired to the TPYR terminal board. Dedicated analog-to-digital converters on VPYR provide sampling rates up to 200,000 samples per second for burst data from two of the temperature channels. Fast temperature data is available for display and offline evaluation. TPYR has simplex and TMR capability as shown in the following figure.



Pyrometer Terminal Board, Processor, and Cabling

Installation

➤ To install the VPYR board

- 1 Power down the VME processor rack.
- 2 Slide in the VPYR board and push the top and bottom levers in with your hands to seat its edge connectors.
- 3 Tighten the captive screws at the top and bottom of the front panel. These screws hold the board firmly in place and enhance the board front ground integrity. The screws should not be used to actually seat the board.

Note Cable connections to the TPYR terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to *Diagnostics* section in this document.

You may need to update the VPYR firmware to the latest level. For instructions, refer to *GEH-6403, Control System Toolbox for the Mark VI Turbine Controller*.

Operation

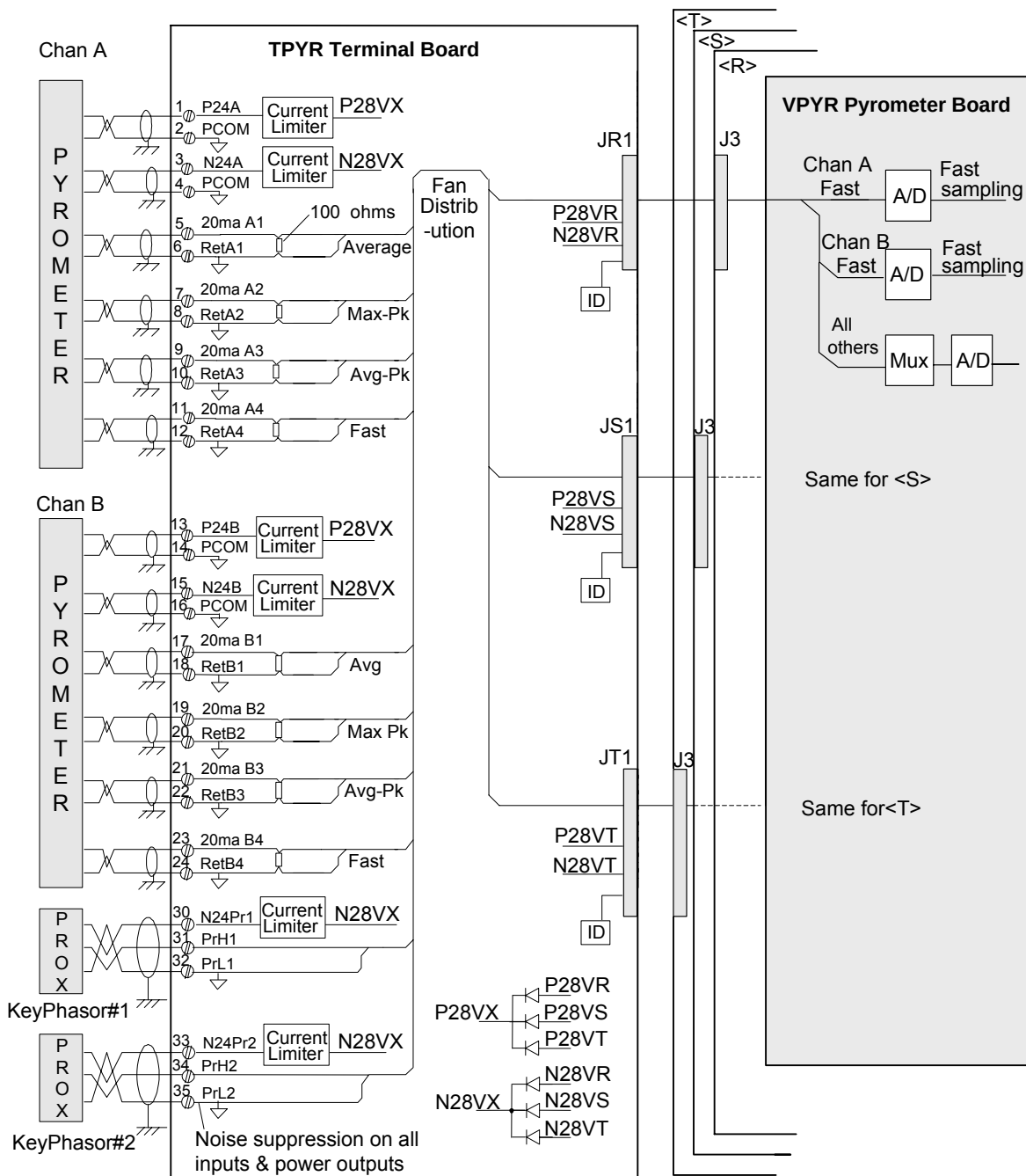
Analog signals from TPYR are cabled to the VPYR processor board where signal sampling and conversion take place. VPYR calculates the temperature profiles and runs turbine protection algorithms using both pyrometer signals. If a trip is indicated and the signals are validated, VPYR issues the trip signal.

Optical Pyrometer Measurements

Two infrared pyrometers dynamically measure the temperature profile of the rotating turbine blades. Each pyrometer is powered by a +24 V dc and a -24 V dc source on the terminal board, diode selected from voltages supplied by the three VPYR boards. Four 4-20 mA signals are returned from each pyrometer, representing the following blade measurements:

- Average temperature
- Maximum peak temperature
- Average peak temperature
- Fast dynamic profile, with 30 kHz bandpass, providing the full signature.

Each 4-20 mA input generates a voltage across a resistor. The signal is sent to VPYR where it is multiplexed and converted. A dedicated A/D converter samples the fast input (#4) at up to 200,000 samples per second. VPYR can be configured for different numbers of turbine buckets, with up to 30 temperature samples per bucket.



VPYR Processor Board and Terminal Board

Keyphasor Inputs

Two Keyphasor probes are used for shaft position reference, with one used as a backup. These probes and associated circuitry are identical to those used with VVIB/TVIB. They sense a shaft keyway or pedestal to provide a time stamp.

Turbine Protection Algorithm

The protection algorithms run every Burst Period. The Burst of *Fast* data is collected concurrently from the two pyrometers. The start of each Burst of Fast data is synchronized with the selected Keyphasor probe. Each burst is continuous and has a nominal length of three revolutions as determined from the probe. The Keyphasor time-stamps, associated with this burst (four stamps) are included in the data. The turbine RPM is also passed to the VPYR card through signal space as a backup to the Keyphasor RPM value.

The algorithm provides seven buffers to store the fast pyrometer temperature data. The buffers store the raw A/D data that is loaded into a buffer automatically through the VPYR's DMA controller. Each buffer stores one burst of data for pyrometer channel A, one burst of data for pyrometer channel B, and one header that describes the sampling details, conversion factors, and rate limits used. The seven buffers allow five buffers to be captured or frozen for a trip function (Trip_minus4, Trip_minus3, Trip_minus2, Trip_minus1 and Trip_List data), one user or manually operated capture list, and the last buffer for gathering sampled data for the protection algorithms.

The pyrometer algorithm takes the latest data from the capture buffers and determines the bucket span (pyrometer samples) that is used for the protection algorithm. BuckOffsetA/B defines the delay in percent of Bucket Period starting from the Keyphasor input to the start of the bucket temperatures that is used in the protection algorithm. BuckSpanA/B defines the percent of the Bucket Period that is used in calculating the bucket temperature signature for the protection algorithm.

The average temperature per burst, the maximum temperature per bucket signature, and the minimum temperature per bucket signature are calculated based on the bucket signature defined by the configuration constants. The average temperature per burst is the average temperature over the bucket signature for 3.1 revolutions of data (1 burst). The maximum temperature is stored for each bucket signature for 3.1 revolutions of data. The minimum temperature is stored for each bucket signature for 3.1 revolutions of data.

A median select is performed on each bucket signature over the three revolutions of data for both the maximum temperature per bucket and the minimum temperature per bucket, as shown in the following figure. This results in a filtered maximum for each bucket over the 3 revolutions of data and a filtered minimum for each bucket over the 3 revolutions of data.

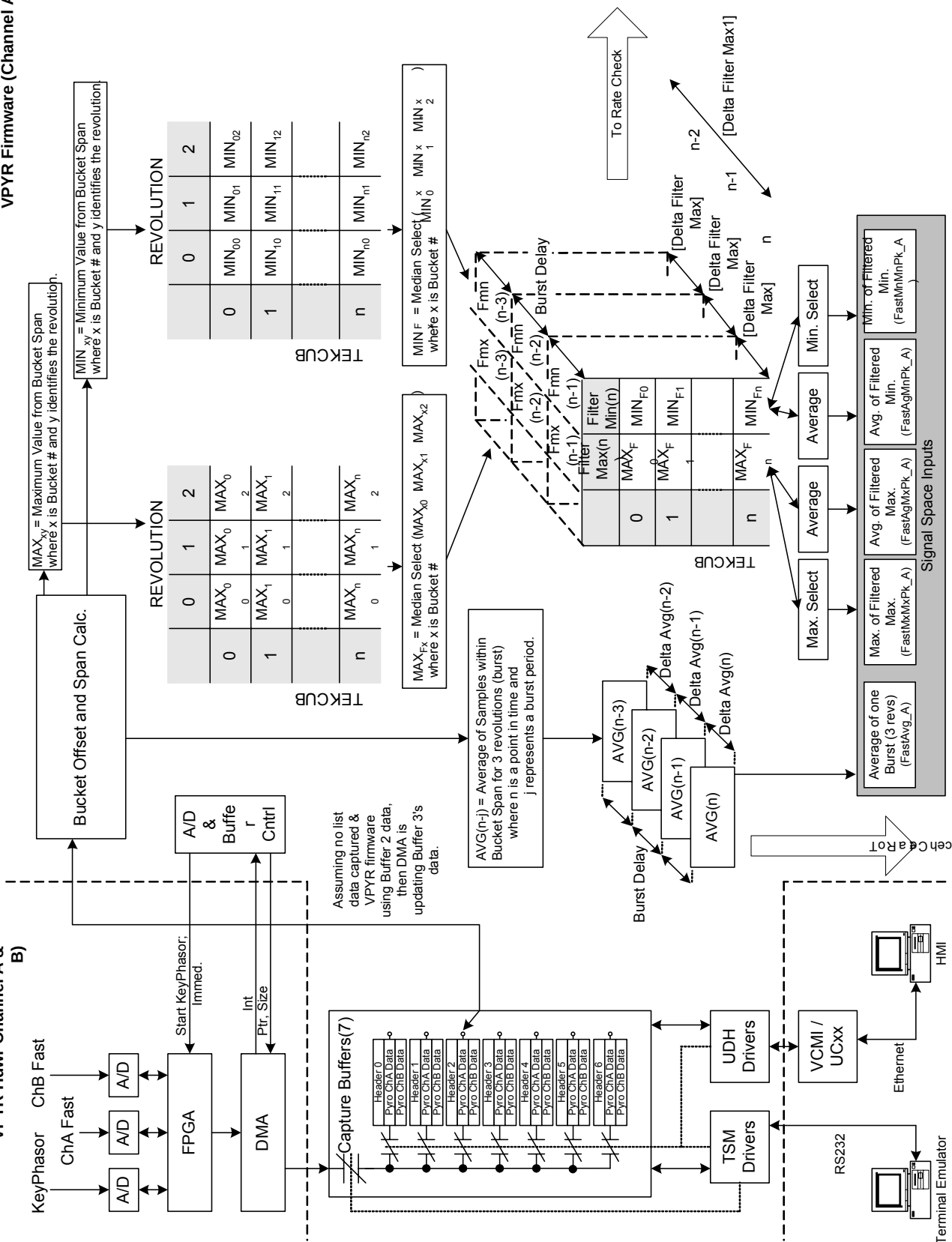
The algorithm performs a maximum select from all the bucket filtered maximums and stores the value in the signal space variable, FastMxMxPk_A/B. The algorithm also performs a minimum select from all the bucket filtered minimums and stores the results in FastMnMnPk_A/B. The algorithm also provides an average of all the filtered maximums, FastAgMxPk_A/B, and calculates the average of all the filtered minimums, FastAgMnPk_A/B.

The following block diagram illustrates the algorithms used to calculate the following from the Pyrometer Channel A and B fast sampled temperature data:

- Maximum of the filtered maximum Turbine Blade Temperature per bucket
- Average of the filtered maximum Turbine Blade Temperature per bucket
- Average of the filtered minimum Turbine Blade Temperature per bucket
- Minimum of the filtered minimum Turbine Blade Temperature per bucket

VPYR Hdw'r Channel A & B)

VPYR Firmware (Channel A)



The rate limit comparator uses the Delta-Delta matrix and compares this against one of two limits. The Delta-Delta matrix is the difference in the rate of change of the filtered maximum temperatures from one burst to another and the rate of change of the average temperature from one burst to the next on a per bucket basis. The limit used is determined by the signal space variable, Rate1 Limit Select for Channel A/B, Rate1_LSel_A/B. If Rate1_LSel_A/B equals *FROM_APPLICATION*, then the signal space variable, Rate1_Lmt_A/B, is used. The application software sets the value used. At initialization the VPYR firmware sets Rate1_Lmt_A/B = Fn1. If Rate1_LSel_A/B equals *FROM_VPYR*, then Fn1 is used. Fn1 is defined as

$$Fn = \text{SetptR1B\_A/B} + \text{SetptR1\_A} * \text{AVG}(n-1)$$

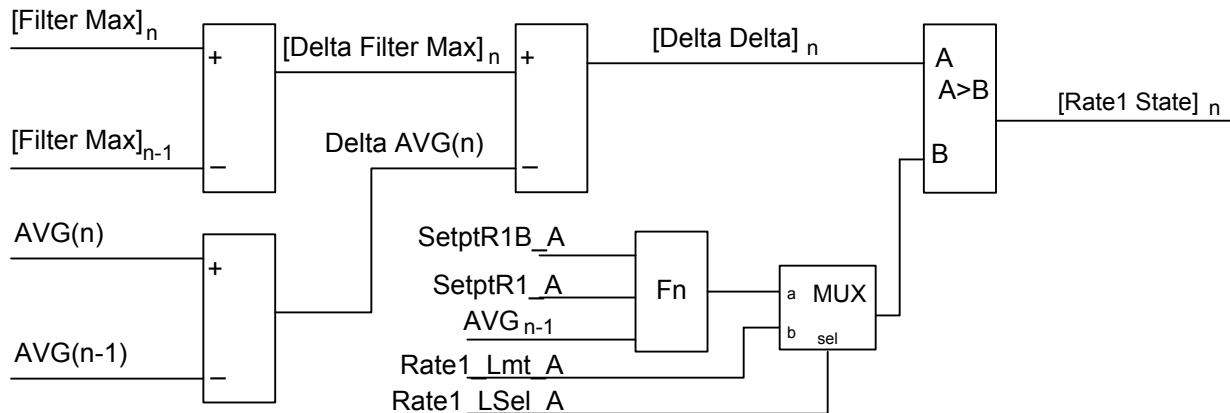
where SetptR1B_A/B is the set point bias for Rate1, _A for channel A & _B for chB,

SetptR1_A/B is the set point gain for Rate1.

The set point bias and gain are both configuration constants in the VPYR. Rate2, Rate3, and the Distance calculations are performed similarly. The pyrometer rate limit checks of the protection algorithm are shown in the following two figures.

Rate Calc:

where SetptRxx_x are IO configurable constants.

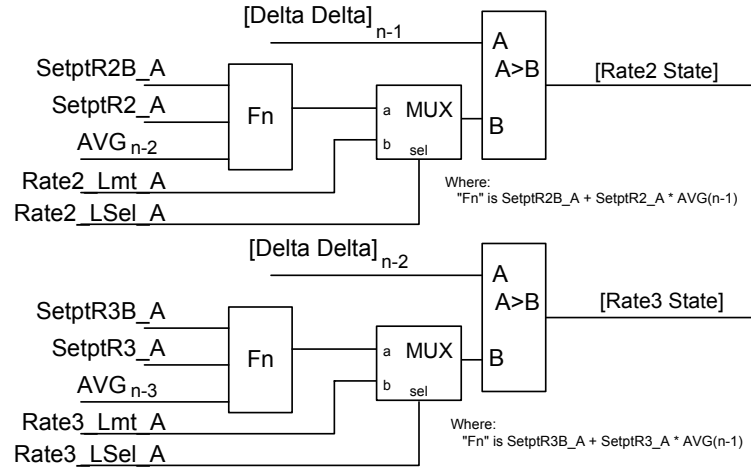


Where:

"Fn" is $\text{SetptR1B\_A} + \text{SetptR1\_A} * \text{AVG}(n-1)$

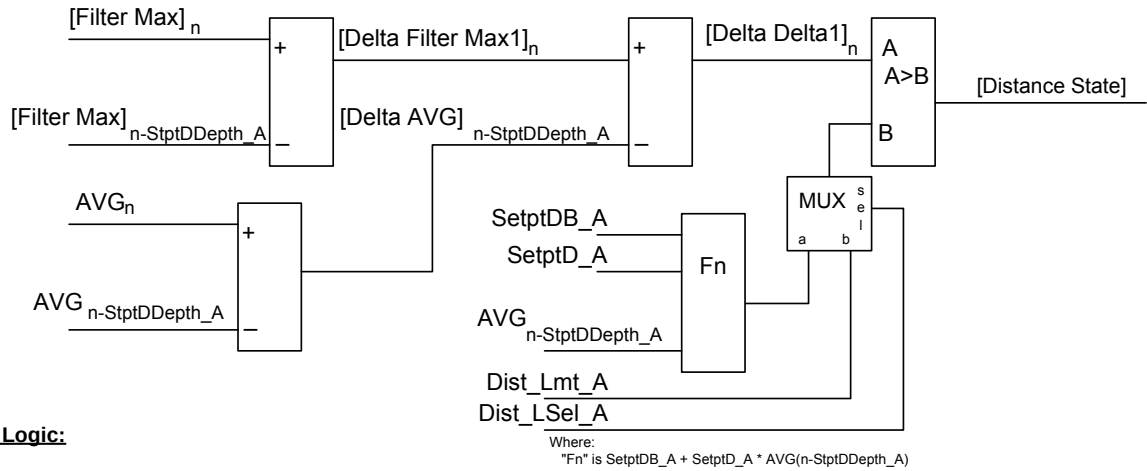
Mark VI Pyrometer Rate Check Portion of Protection Algorithm

Rate Calc Cont'd:



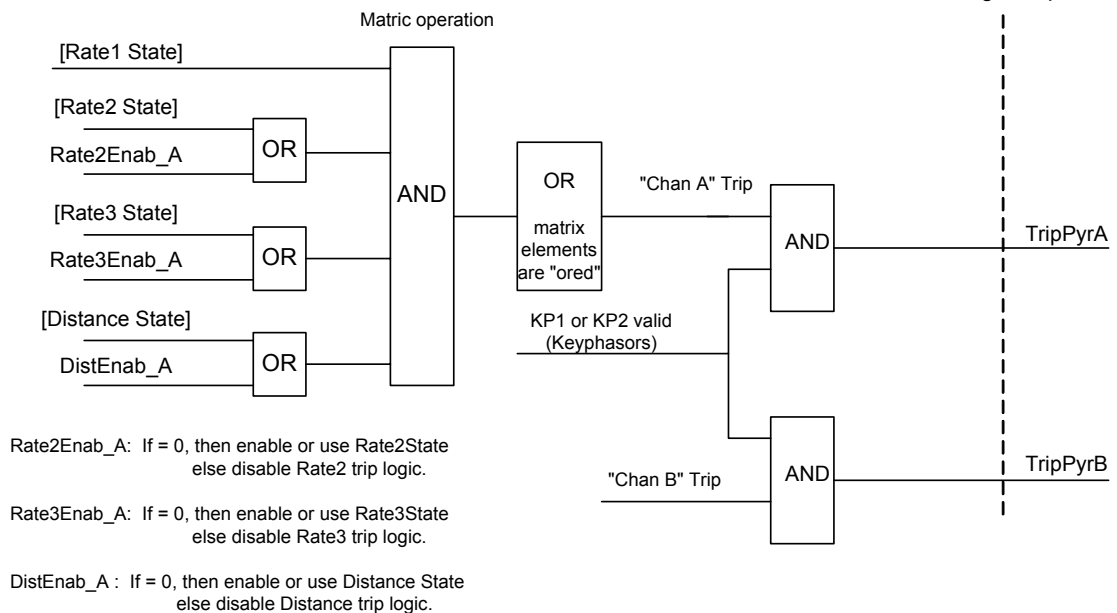
Distance Calc:

where SetptDx_A and StptDDepth_A are configurable constant



Trip Logic:

where RatexEnab_A are IO Configuration constants used as disable switches



Mark VI Pyrometer Rate/Distance Check Portion of Protection Algorithm

Data Historian Upload of Captured Lists

The Data Historian is used to upload captured lists from VPYR. For a TMR system configuration, the Data Historian uploads the captured lists from VPYR that is designated the UDH communicator. If the user wants the Data Historian to upload captured lists from each of the three VPYRs, then the user must configure the VPYRs as simplex.

VPYR provides two types of captured lists. VPYR runs protection algorithms examining the rate of temperature rise on the turbine blades. If the rate of rise is too high, then the protection algorithm flags the application software through the board point, TripPyrA or TripPyrB, which indicates a rate limit trip for either Channel A and B pyrometer. The application software in the controller detects the rate limit trip and, based on the application code sequencing, either requests a list capture for the trip information or does not. The VPYR captures five individual lists of approximately 12,000 samples or less of temperature data for each channel. The lists are identified as Trip_minus4, Trip_minus3, Trip_minus2, Trip_minus1, and TripList. Trip_minus1 stores the actual event that caused the trip indication. Each list includes a header describing the data captured and the data.

The second type of list capture is a user requested capture. The user capture request is generated in the controller application software in two different ways. First, the user can manually request a pyrometer temperature data capture through the HMI screen. Secondly, the application code periodically pings the VPYR(s) with a request based on a User Capture Timer set up through an HMI screen. When the board point, User Capture Request (UserCapReq), is set True by the application software, the VPYR(s) capture a single list of temperature data for both Channel A and Channel B pyrometers.

The Data Historian uses the voted board point, Trip Captured List (TripCapList), to determine when the trip list(s) are available by the VPYR for upload. The Data Historian uses the voted board point, User Captured List (UserCapList), for a User list upload. When the Boolean TripCapList or UserCapList equal True, the Data Historian checks the Main Header parameter, ListNumber. For I/O boards with multiple lists to be uploaded the parameter, ListNumber, indicates the number of the list that is ready to be uploaded.

Application Software State Diagram

Normally, the application software is in the *No Pyro Fault Detected* state. A pyrometer trip detection is determined by checking the EGD read variables, TripPyrA and TripPyrB. If either of these variables are True, then the application software transitions to the *Pyrometer Fault Detected* state where the EGD write variable, LogTrigger, is set True.

VPYR freezes the five lists, Trip_minus4, Trip_minus3, Trip_minus2, Trip_minus1, and TripList per the request, LogTrigger = True, from the application software. Next, VPYR prepares the Trip_minus4 for upload by the Data Historian. The EGD variable, TripCapList is set True by VPYR after the Trip_minus4 upload prep work has been completed. The application software transitions to the *Data Historian Uploading* state on the detection of TripCapList = True.

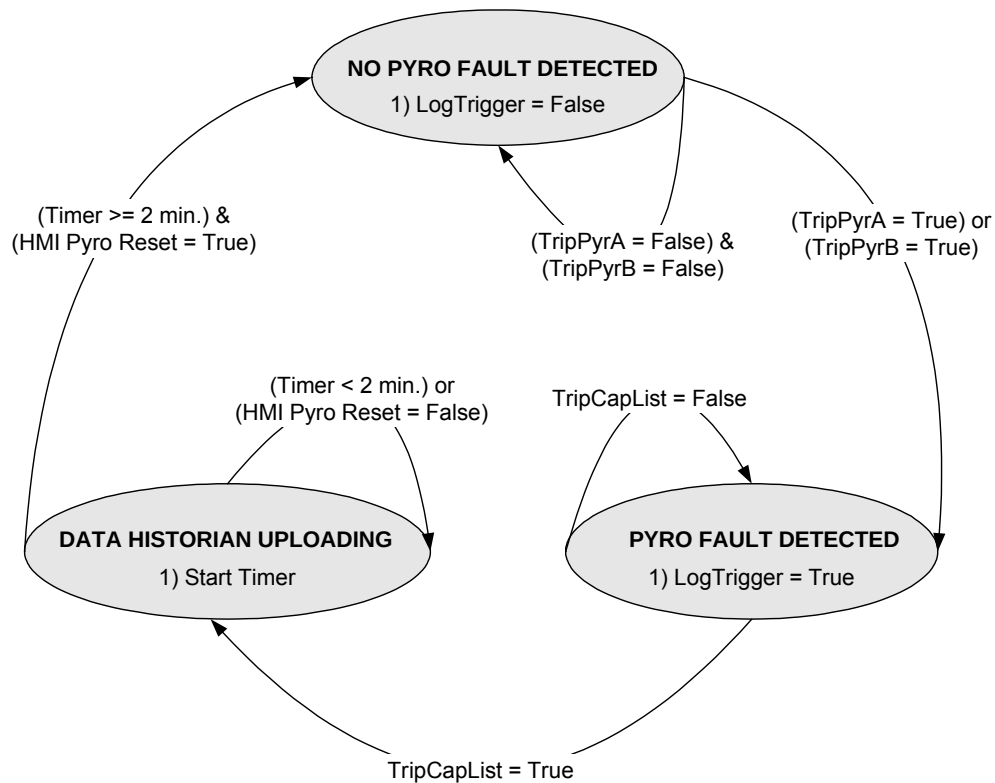
The application software starts a timer in the *Data Historian Uploading* state. To allow enough time for the Data Historian to upload the 5 lists, a minimum 2 minutes delay is required before the HMI Pyrometer Reset button is recognized.



Warning

Resetting the EGD variable, LogTrigger, to False before the two minute delay is complete will corrupt the uploaded data.

The following figure shows how the controller application software handles the detection of a pyrometer trip.



Record Storage in the Data Historian Archive

At least 450 Mbytes of disk space is required to store the Data Historian Archive for Operator or User Captured lists from six VPYR boards (TMR system – boards configured as Simplex) at a maximum rate of one upload per day for two years.

Archive Folder Layout

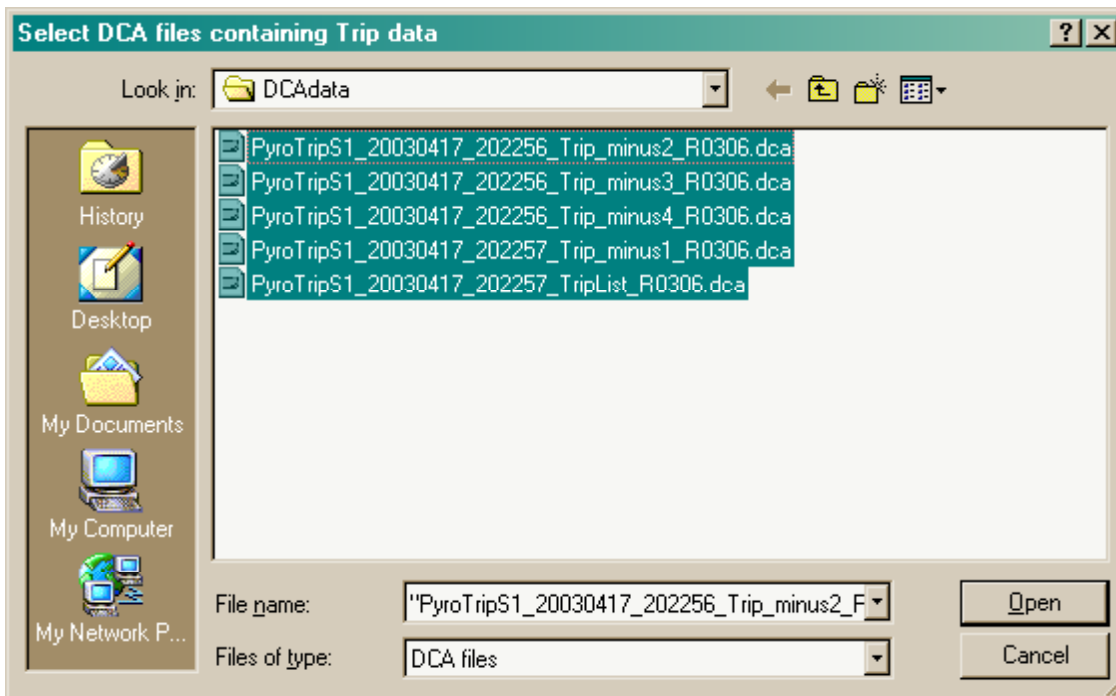
The folder structure for the Mark* VI I/O boards follows the Data Historian standard. In addition, the main header uploaded from the I/O board provides a subfolder name under the date folder. The naming convention for the file format is:

<collection-name_date_time_controller_rack#_slot#_list-name_A>.dca

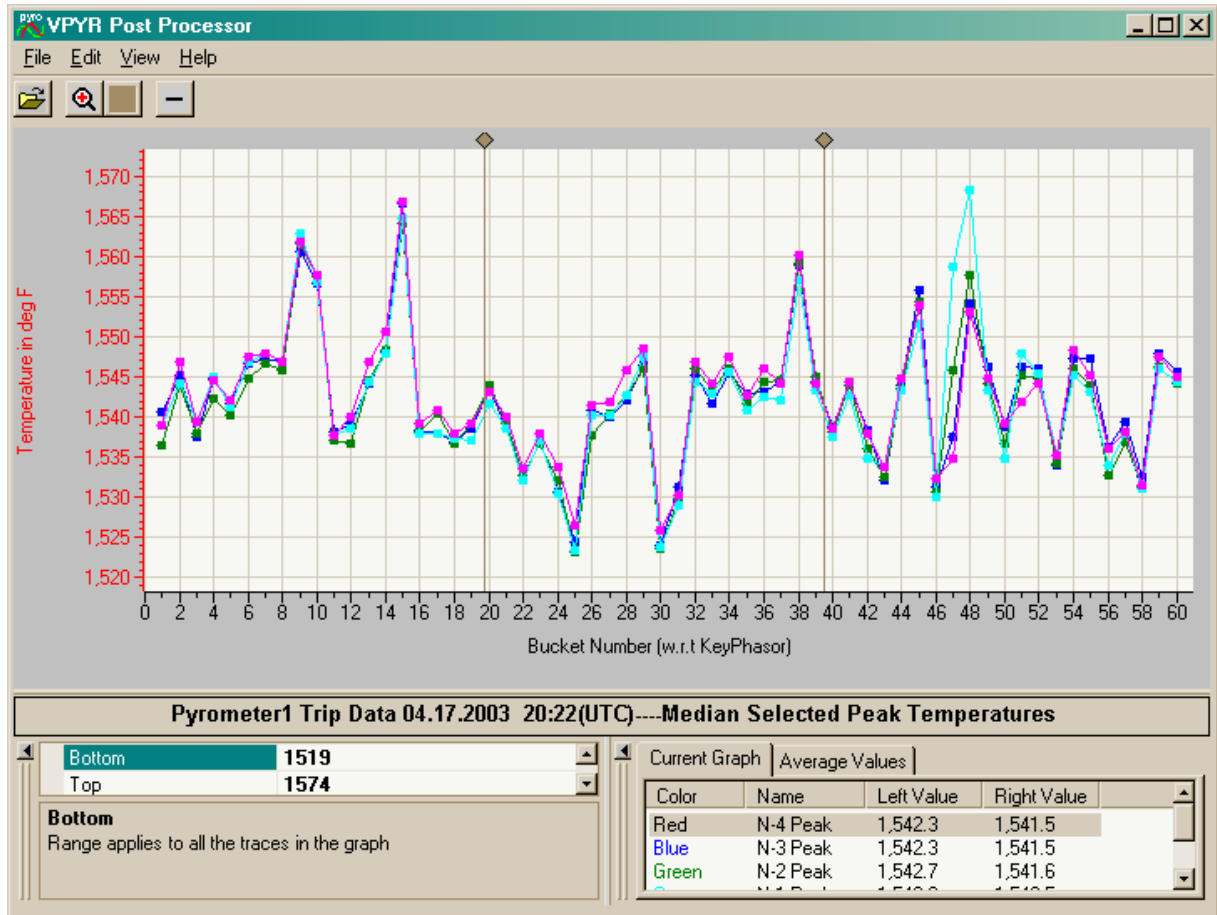
File	Description
collection-name	This is used as the character field for Mark VI I/O board name (VPYR)
date	Date format YYMMDD
time	Time format HHMMSS Note: The time is defined as the trigger time provided in the Main Header. If I/O board does not provide, then Data Historian will use its computer time.
controller	This defines the R, S or T controller
rack#	This defines the rack number
slot#	This defines the slot number
list-name	This defines the Mark VI I/O list name. Note ListName is provided in the main header. If list-name is not provided, then an alpha character will be appends to the file name to insure a unique file name for each list.

Pyrometer Viewer

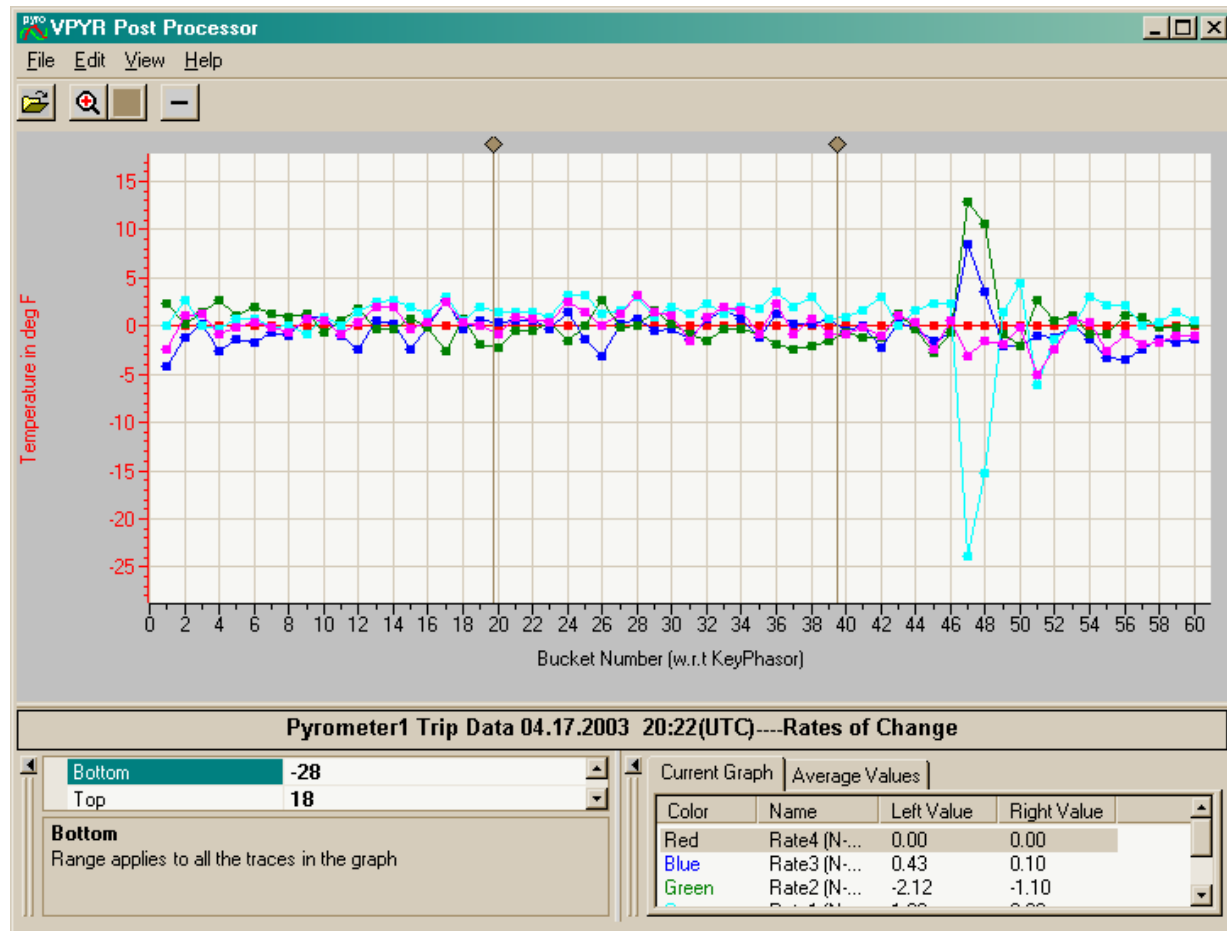
The Pyrometer Viewer is used to upload the data captured by the Data Historian. The Viewer is a separate application from the toolbox and is loaded onto the HMI computer or even the field engineer's computer. The user selects the five dca files associated with the trip as shown in the following figure.



The Pyrometer Viewer uses the raw temperature data from each dca file and re-calculates the median peak temperatures for each bucket as shown in the following figure.



The rate of change data per each burst is also provided as shown in the following figure.



Specifications

Item	Specification
Number of inputs	2 pyrometers, each with 4 analog 4–20 mA current signals 2 Keyphasor probes, each with –0.5 to –20 V dc inputs
Current inputs from pyrometers	4–20 mA across a 100 ohm resistor. Common mode rejection: Dc up to ± 5 V dc, CMRR of 80 dB Ac up to ± 5 Volt peak, CMRR of 60 dB Measurement accuracy of $\pm 0.1\%$ full scale, 14-bit resolution. Bandwidth of 0 to 100 Hz on 6 slow inputs using multiplexed A/D converter. Bandwidth of 0 to 30,000 Hz on two fast inputs using dedicated A/D converters, sampling at 200,000 per sec.
Keyphasor inputs	Input voltage range of –0.5 to –20 V dc CMR of 5 V, CMRR of 50 dB at 50/60 Hz Accuracy 2% of full scale (0.2 V dc) Dc level detection typically 0.2 V/mil sensitivity Speed measurement 2 to 5,610 RPM with accuracy of 0.1% of reading
Device excitation	Pyrometers have individual power supplies, current limited: P24V source is diode selected, +22 to +30 V dc, 0.175 A N24V source is diode selected, -22 to -30 V dc, 0.175 A
Measurement parameters	Rated RPM up to 5,100 RPM Number of buckets per stage, up to 92 Number of samples per bucket, up to 30 Fast inputs sampled in bursts covering three revolutions, at twice per second
Size	26.04 cm high x 1.99 cm, wide x 18.73 cm, deep (10.25 x 0.782 x 7.375)

Diagnostics

Three LEDs at the top of the VPYR front panel provide status information. The normal RUN condition is a flashing green, FAIL is a solid red. The third LED is STATUS and is normally off but shows a steady orange if a diagnostic alarm condition exists in the board. VPYR makes diagnostic checks including:

- System limit checking on the temperature inputs and the Keyphasor gap signals can create faults.
- The two pyrometer inputs are compared against configuration limits to determine if they are tracking, and the fast data is compared with other inputs to check validity.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VPYR occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy.
- Terminal board connectors JR1, JS1, and JT1 have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VPYR and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Module Parameter	Description	Choices
Calibration		
System limits	Enables or disables all system limit checking	Enable, disable
Min_MA_Input	Minimum MA for healthy 4-20 mA input	0 to 21
Max_MA_Input	Maximum MA for healthy 4-20 mA input	0 to 21
RPMrated	Rated turbine RPM	300 to 10,000
BuckSamples	Minimum samples per bucket at 110 percent speed	10 to 30
BuckOffset_A	Offset from key to the first bucket, % bucket, pyrometer A	0 to 100
BuckSpan_A	Percent of bucket to include in protection algorithm, pyrometer A	0 to 100
BuckNumb_A	Number of buckets, pyrometer A	30 to 92
Burst_Period	Burst Period for Pyr A & B. Note: Value here must match what is in the controller application software.	480 to 5000
SetptR1_A	Setpoint, rate 1, pyrometer A	-1 to 1
SetptR1B_A	Setpoint, rate 1, bias, average temp, pyrometer A	0 to 50
SetptR2_A	Setpoint, rate 2, pyrometer A	-1 to 1
SetptR2B_A	Setpoint, rate 2, bias, average temp, pyrometer A	0 to 50
SetptR3_A	Setpoint, rate 3, pyrometer A	-1 to 1
SetptR3B_A	Setpoint, rate 3, bias, average temp, pyrometer A	0 to 50
SetptD_A	Setpoint distance, pyrometer A	-1 to 1
SetptDB_A	Setpoint distance bias, average temp, pyrometer A	0 to 50
SetptDDepth_A	Setpoint, depth of the distance measurement, pyrometer A	1 to 3
Rate2Enab_A	Enable, temperature rate 2, pyrometer A	Enable, disable
Rate3Enab_A	Enable, temperature rate 3, pyrometer A	Enable, disable
DistEnab_A	Enable temperature rate 3, pyrometer A	Enable, disable
	Same configuration for channel B pyrometer	
J3:IS200TPYRH1A	Terminal board 1 connected to VPYR through J3	Connected, not connected
SlowAvg_A	Slow, average temperature, pyrometer A - board point	Point edit (input FLOAT)
Input use		Used, unused
Low_Input	Input MA at low value	0 to 21
Low_Value	Input value in engineering units at low MA	-3.4e+038 to 3.4e+038
High_Input	Input MA at high value	0 to 21
High_Value	Input value in engineering units at high MA	-3.4e+038 to 3.4e+038
TMR_Diff	Difference limit for voted TMR inputs in % of (high value/low value)	0 to 100
SlowMXPk_A	Slow, maximum peak temperature, pyrometer A (configuration similar to above) - board point	Point edit (input FLOAT)
SlowAvgPk_A	Slow, average peak temp, pyrometer A - board point	Point edit (input FLOAT)
FastAvg_A	Fast, average temp, pyrometer A - board point	Point edit (input FLOAT)
SlowAvg_B	Slow, Average Temperature, Pyr B - board point	Point Edit (Input FLOAT)
SlowMXPk_B	Slow, Max Peak Temperature, Pyr B - board point	Point Edit (Input FLOAT)
SlowAvgPk_B	Slow, average peak temperature, Pyr B - board pt.	Point Edit (Input FLOAT)
FastAvg_B	Fast, average temperature, Pyr B - board point	Point Edit (Input FLOAT)
GAP_KPH1	Air Gap, keyPhasor #1 - board point	Point Edit (Input FLOAT)
VIB-Type	Configurable item	Used, Not used
VIB_Scale	Volts/mil	0 to 2

Module Parameter	Description	Choices
KPH_Thrshld	Voltage difference from gap voltage where Keyphasor Trigger	1 to 5
KPH_Type	Type of Pulse Generator	Slot, Pedestal
SysLim	System Limits 1 and 2, and TMR same as above	Standard Choices
GAP_KPH2	Air Gap, keyPhasor #2, config. Same as above - board point	Point Edit (Input FLOAT)

Board Points (Signals)	Description – Point Edit (Enter Signal Name)	Direction	Type
L3DIAG_VPYR1	Board diagnostic	Input	BIT
L3DIAG_VPYR2	Board diagnostic	Input	BIT
L3DIAG_VPYR3	Board diagnostic	Input	BIT
ProtAlgRun_A	Protection Algorithm is running for Pyr Ch. A	Input	BIT
ProtAlgRun_B	Protection Algorithm is running for Pyr Ch. B	Input	BIT
TripCapList	Trip Capture List is ready for upload	Input	BIT
UserCapList	User Capture List is ready for upload	Input	BIT
Rate1_LSel_A	Rate1 Logic Select for Channel A	Output	BIT
Rate2_LSel_A	Rate2 Logic Select for Channel A	Output	BIT
Rate3_LSel_A	Rate3 Logic Select for Channel A	Output	BIT
Dist_LSel_A	Distance Logic Select for Channel A	Output	BIT
Rate1_LSel_B	Rate1 Logic Select for Channel B	Output	BIT
Rate2_LSel_B	Rate2 Logic Select for Channel B	Output	BIT
Rate3_LSel_B	Rate3 Logic Select for Channel B	Output	BIT
Dist_LSel_B	Distance Logic Select for Channel B	Output	BIT
TripPyrA	Bucket temperature rate trip, pyrometer A	Input	BIT
TripPyrB	Bucket temperature rate trip, pyrometer B	Input	BIT
KeyPh1Act	Keyphasor 1 Active	Input	BIT
KeyPh2Act	Keyphasor 2 Active	Input	BIT
SysLim1KP1	System Limit	Input	BIT
SysLim2KP1	System Limit	Input	BIT
SysLim1KP2	System Limit	Input	BIT
SysLim2KP2	System Limit	Input	BIT
FastMxMxPk_A	Fast, Max of the Max Peaks Temp, Pyr A	Input	FLOAT
FastAgMxPk_A	Fast, Average of the Max Peaks Temp, Pyr A	Input	FLOAT
FastMnMnPk_A	Fast, Min of the Min Peaks Temp, Pyr A	Input	FLOAT
FastAgMnPk_A	Fast, Average of the Min Peaks, Pyr A	Input	FLOAT
FastMxMxPk_B	Fast, Max of the Max Peaks Temp, Pyr B	Input	FLOAT
FastAgMxPk_B	Fast, Average of the Max Peaks Temp, Pyr B	Input	FLOAT
FastMnMnPk_B	Fast, Min of the Min Peaks Temp, Pyr B	Input	FLOAT
FastAgMnPk_B	Fast, Average of the Min Peaks, Pyr B	Input	FLOAT
RPM_KPH1	RPM Keyphasor #1	Input	FLOAT
RPM_KPH2	RPM Keyphasor #2	Input	FLOAT
Rate1_Lmt_A	Rate1 Limit value for Channel A pyro.	Output	FLOAT
Rate2_Lmt_A	Rate2 Limit value for Channel A pyro.	Output	FLOAT
Rate3_Lmt_A	Rate3 Limit value for Channel A pyro.	Output	FLOAT
Dist_Lmt_A	Distance Limit value for Channel A pyro.	Output	FLOAT
Rate1_Lmt_B	Rate1 Limit value for Channel B pyro.	Output	FLOAT
Rate2_Lmt_B	Rate2 Limit value for Channel B pyro.	Output	FLOAT
Rate3_Lmt_B	Rate3 Limit value for Channel B pyro.	Output	FLOAT
Dist_Lmt_B	Distance Limit value for Channel B pyro.	Output	FLOAT

Board Points (Signals)	Description – Point Edit (Enter Signal Name)	Direction	Type
TripBuckIx_A	Index of the first Bucket causing trip, Pyr A	Input	FLOAT
TripBuckNb_A	Number of Buckets causing trip, Pyr A	Input	FLOAT
TripBuckIx_B	Index of the first Bucket causing trip, Pyr B	Input	FLOAT
TripBuckNb_B	Number of Buckets causing trip, Pyr B	Input	FLOAT
LogTrigger	When true, records freeze, two before, one after	Output	BIT
ResetLists	Reset Captured Lists	Output	BIT
UserCapReq	User Capture List request from controller	Output	BIT
PollStrobe	Strobe to keep each TMR based Pyro in synch	Output	BIT
TurbRPM	Turbine Speed in RPM	Output	FLOAT

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration.
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32&38	Milliamp input associated with the slow average temperature is unhealthy. Pyro## SLOW AVG TEMP unhealthy	Specified pyrometer's average output is faulty, or VPYR or TPYR is faulty.
33&39	Pyro## Slow Max Pk Temp unhealthy. Milliamp input associated with the slow maximum peak temperature is unhealthy	Specified pyrometer's maximum output is faulty, or VPYR or TPYR is faulty.
34&40	Pyro## Slow Average Peak Temp. Milliamp input associated with the slow average peak temperature is unhealthy	Specified pyrometer's peak output is faulty, or VPYR or TPYR is faulty.
35&41	Pyro##Fast Temp Unhealthy. Milliamp input associated with the fast temperature is unhealthy	Specified pyrometer's fast output is faulty, or VPYR or TPYR is faulty.
36&42	Pyro## Fast Cal Reference out of limits. The fast calibration reference is out of limits	VPYR is faulty
37&43	Pyro## Fast Cal Null out of limits. The fast calibration null is out of limits	VPYR is faulty
44	Slow Cal Reference out of limits. The slow calibration reference is out of limits	VPYR is faulty
45	Slow Cal Null out of limits. The slow calibration null is out of limits	VPYR is faulty
128-191	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
224-247	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

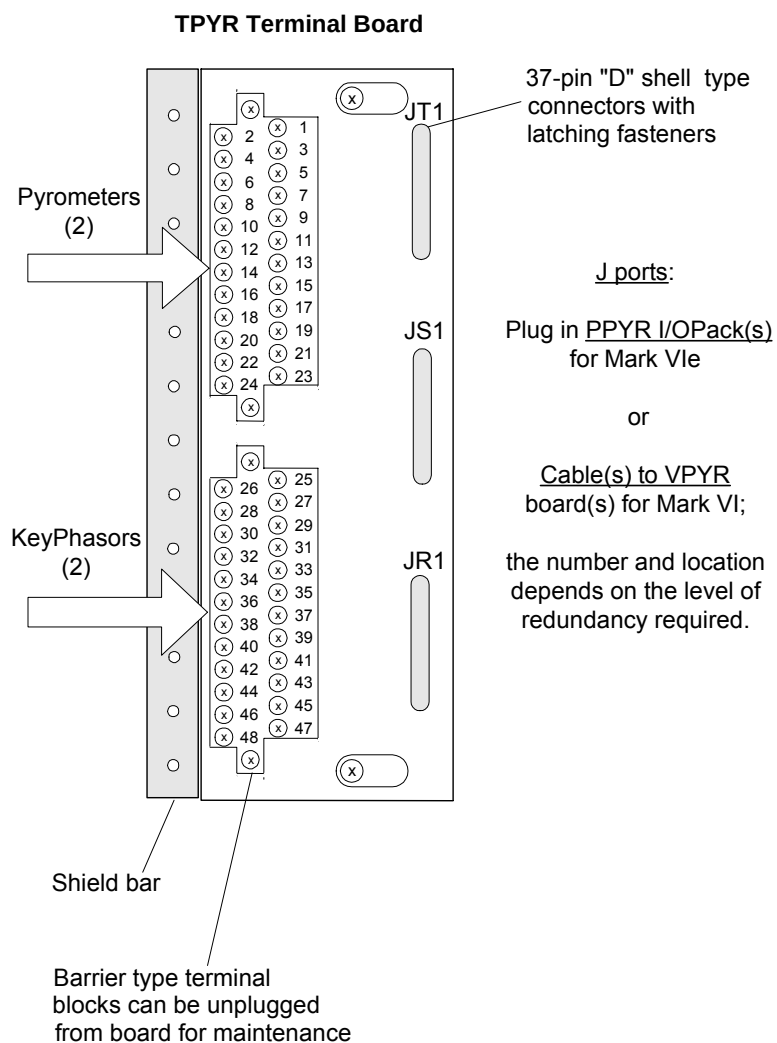
TPYR Pyrometer Input

Functional Description

The Pyrometer Input (TPYR) terminal board is wired to two pyrometers and to two Keyphasor[®] Proximitors[®] probes for shaft reference. The resulting 10 voltage signals are cabled to the VPYR board, which samples them at up to 200,000 samples per second.

Three DC-37 connectors on TPYR connect to three VPYRs. Connections can be simplex on a single connector (JR1), or TMR using all three connectors. In TMR applications, the input signals are fanned to the three connectors for the R, S, and T controls.

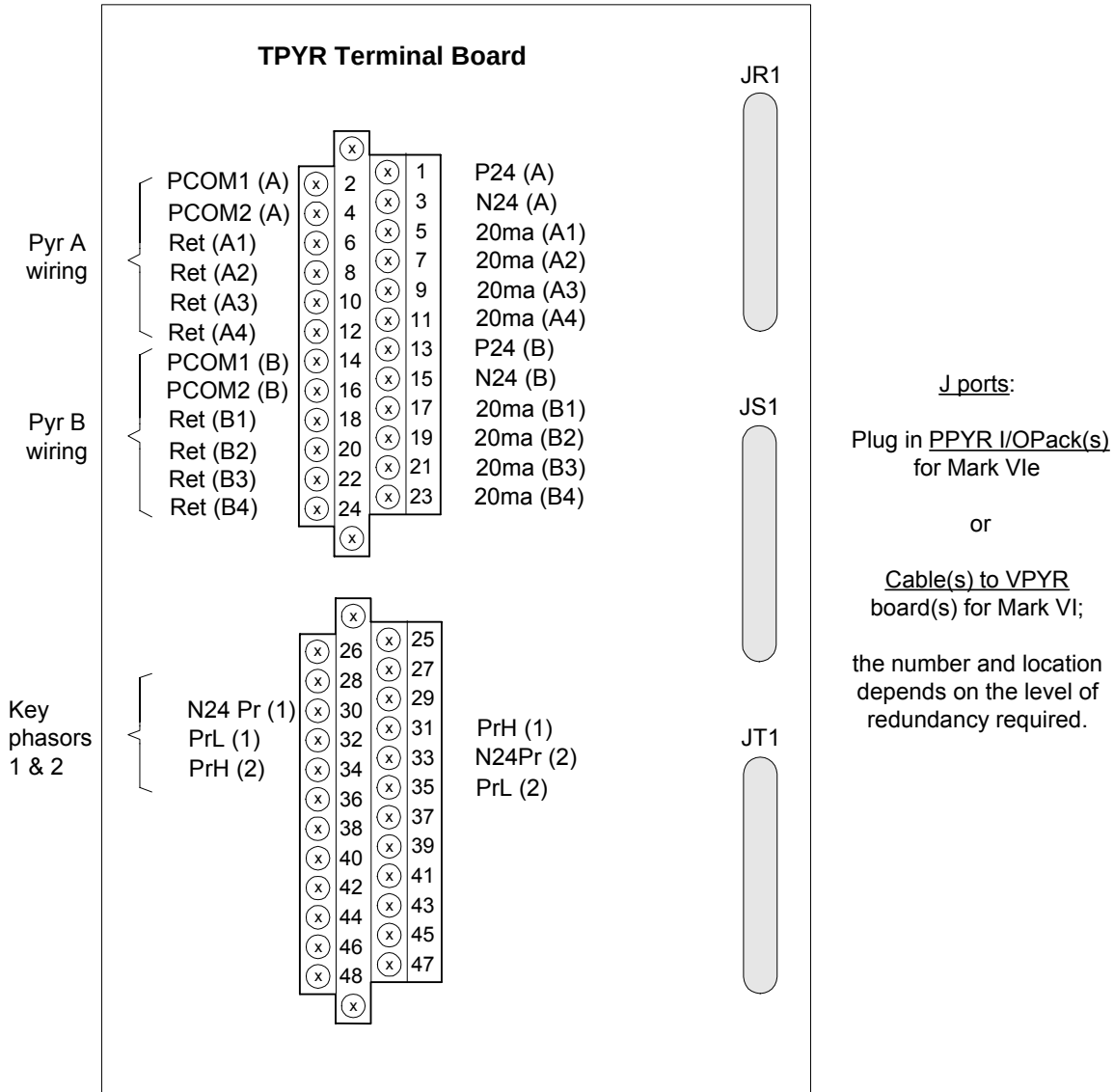
In the Mark* VI system, TPYR works with the VPYR I/O board and supports simplex and TMR applications. With TMR systems, TPYR connects to three VPYR boards with three cables.



Pyrometer Terminal Board

Installation

Connect the wires for the two optical pyrometer inputs directly to the first terminal block. Connect the wires for the two Keyphasor probes directly to the second terminal block. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block. 28 V dc power for the sensors comes in from the R, S, and T VPYR through the JR1, JS1, and JT1 connectors. The following figure shows TPYR wiring and cabling.

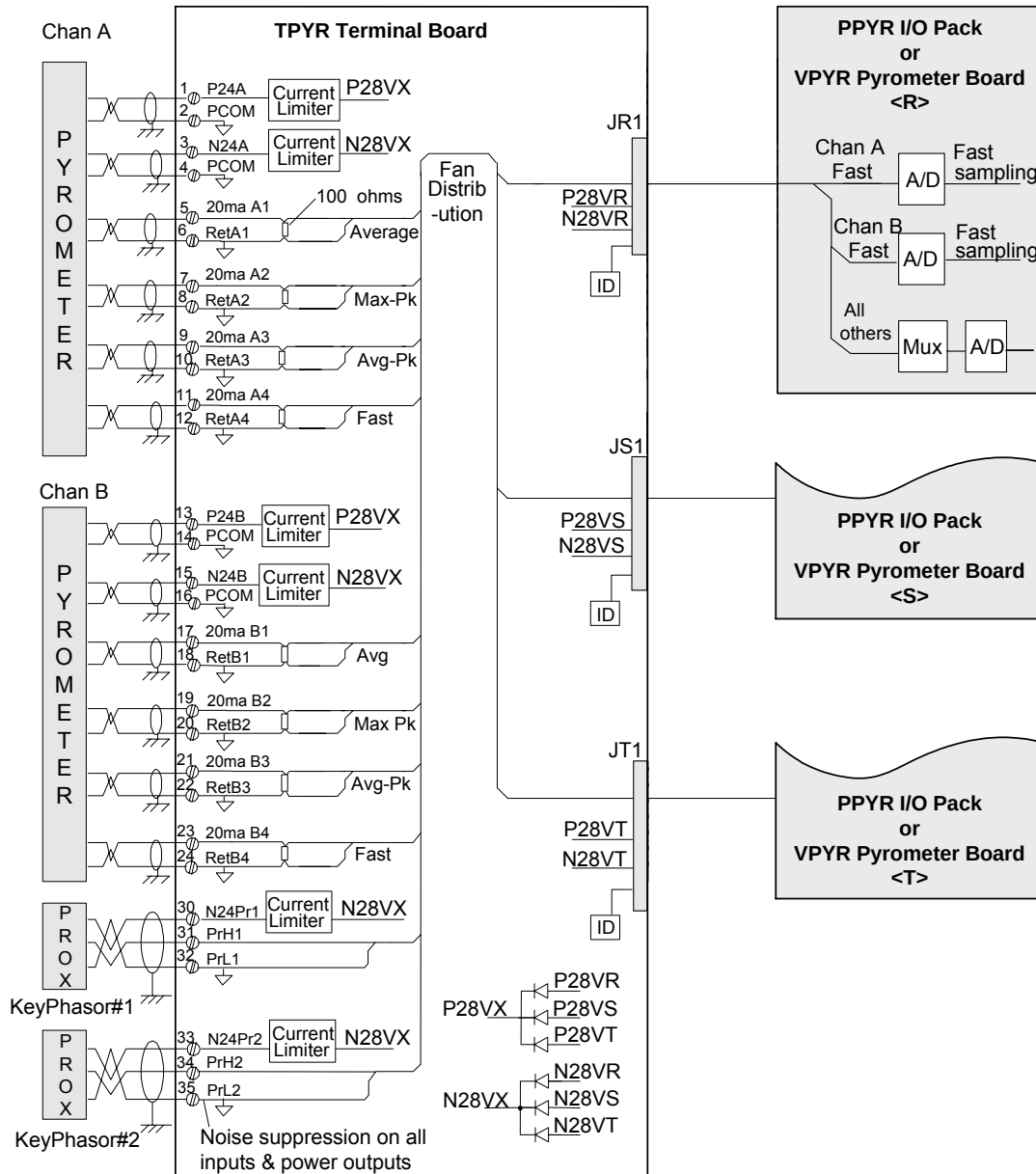


Terminal Blocks can be unplugged from terminal board for maintenance

TPYR Terminal Board Wiring and Cabling

Operation

Analog signals from TPYR are cabled to the VPYR board. The following figure shows the pyrometer monitoring circuit.



TPYR Terminal Board and I/O Boards

Optical Pyrometer Measurements

Two infrared pyrometers dynamically measure the temperature profile of the rotating turbine blades. Each pyrometer is powered by a +24 V dc and a -24 V dc source, diode selected on TPYR from voltages supplied by the three VPYRs. Four 4-20 mA signals are returned from each pyrometer, representing the following blade measurements:

- Average temperature
- Maximum peak temperature
- Average peak temperature
- Fast dynamic profile, with 30 kHz bandpass, providing the full signature.

Each 4-20 mA input generates a voltage across a resistor. The signal is sent to VPYR where it is multiplexed and converted. VPYR can be configured for different numbers of turbine buckets, with up to 30 temperature samples per bucket.

Keyphasor Inputs

Two Keyphasor probes are used for shaft position reference, with one used as a backup. These probes and associated circuitry are identical to those used with VVIB/TVIB. They sense a shaft keyway or pedestal to provide a time stamp (angle reference for blade identification).

Specifications

Item	Specification
Number of inputs	2 pyrometers, each with 4 analog 4–20 mA current signals 2 Keyphasor probes, each with –0.5 to –20 V dc inputs
Current inputs from pyrometers	4-20 mA across a 100 ohm resistor. Common mode rejection: Dc up to ± 5 V dc, CMRR of 80 dB Ac up to ± 5 Volt peak, CMRR of 60 dB
Keyphasor inputs	Input voltage range of -0.5 to -20 V dc. CMR of 5 V, CMRR of 50 dB at 50/60 Hz
Device excitation (outputs)	Each Pyrometers has individual power supplies, current limited: P24V source is diode selected, +22 to +30 V dc, 0.175 A N24V source is diode selected, -22 to -30 V dc, 0.175 A
Size	10.16 cm wide x 33.02 cm high (4.0 in x 13 in)

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- There is system limit checking on the temperature inputs and the Keyphasor gap signals, and these can create faults.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VPYR occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy.
- Terminal board connectors JR1, JS1, and JT1 have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by the I/O board and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

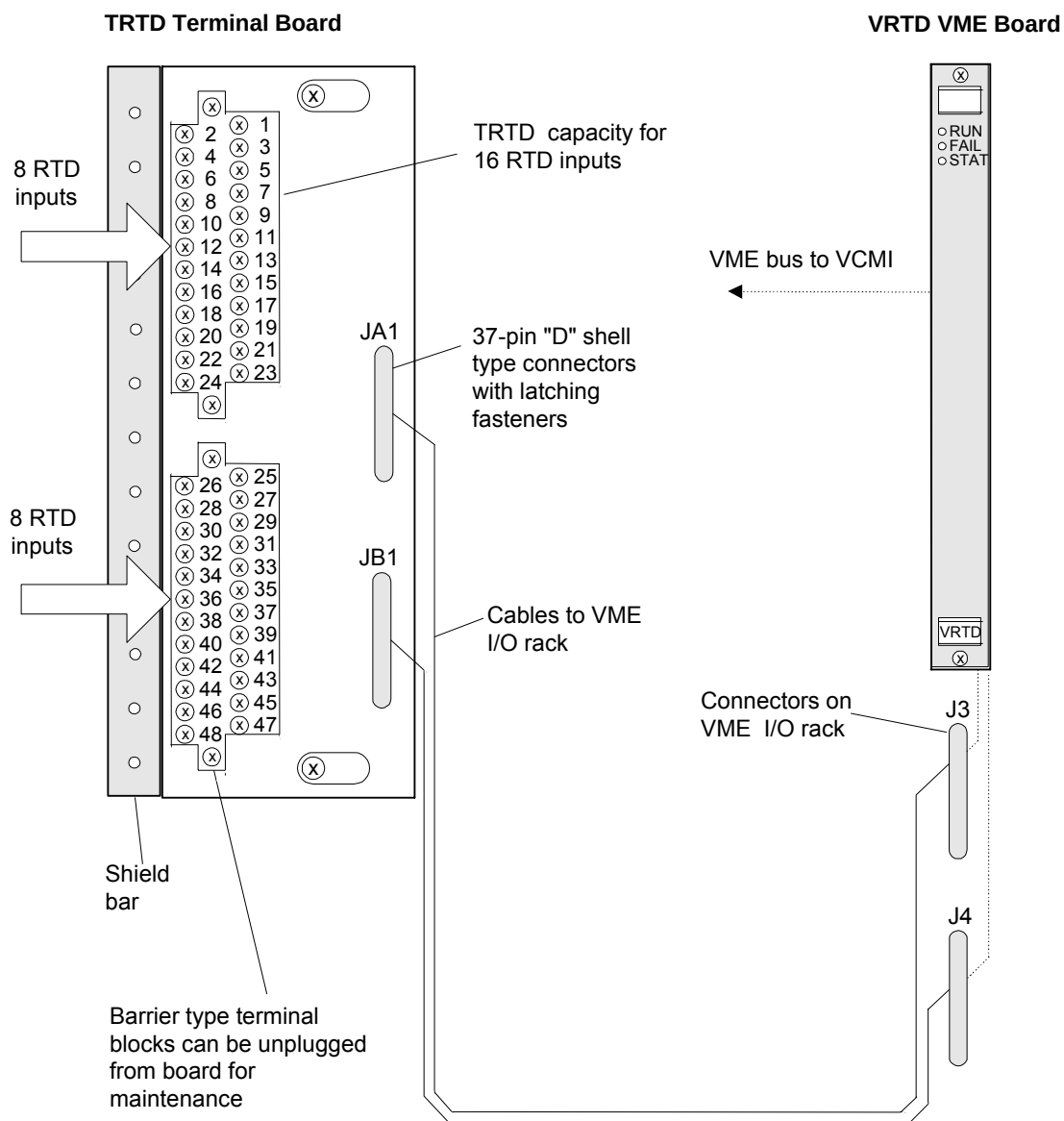
VRTD RTD Input

VRTD RTD Input

Functional Description

The Resistance Temperature Device (RTD) Input (VRTD) board accepts 16, three-wire RTD inputs. These inputs are wired to a RTD terminal board (TRTD or DRTD). Cables with molded fitting connect the terminal board to the VME rack where the VRTD processor board is located.

VRTD excites the RTDs and the resulting signals return to the VRTD. VRTD converts the inputs to digital temperature values and transfers them over the VME backplane to the VCMI, and then to the controller.



RTD Input Terminal Board, I/O Board, and Cabling

Installation

➤ To install the V-type board

- 1 Power down the VME processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel

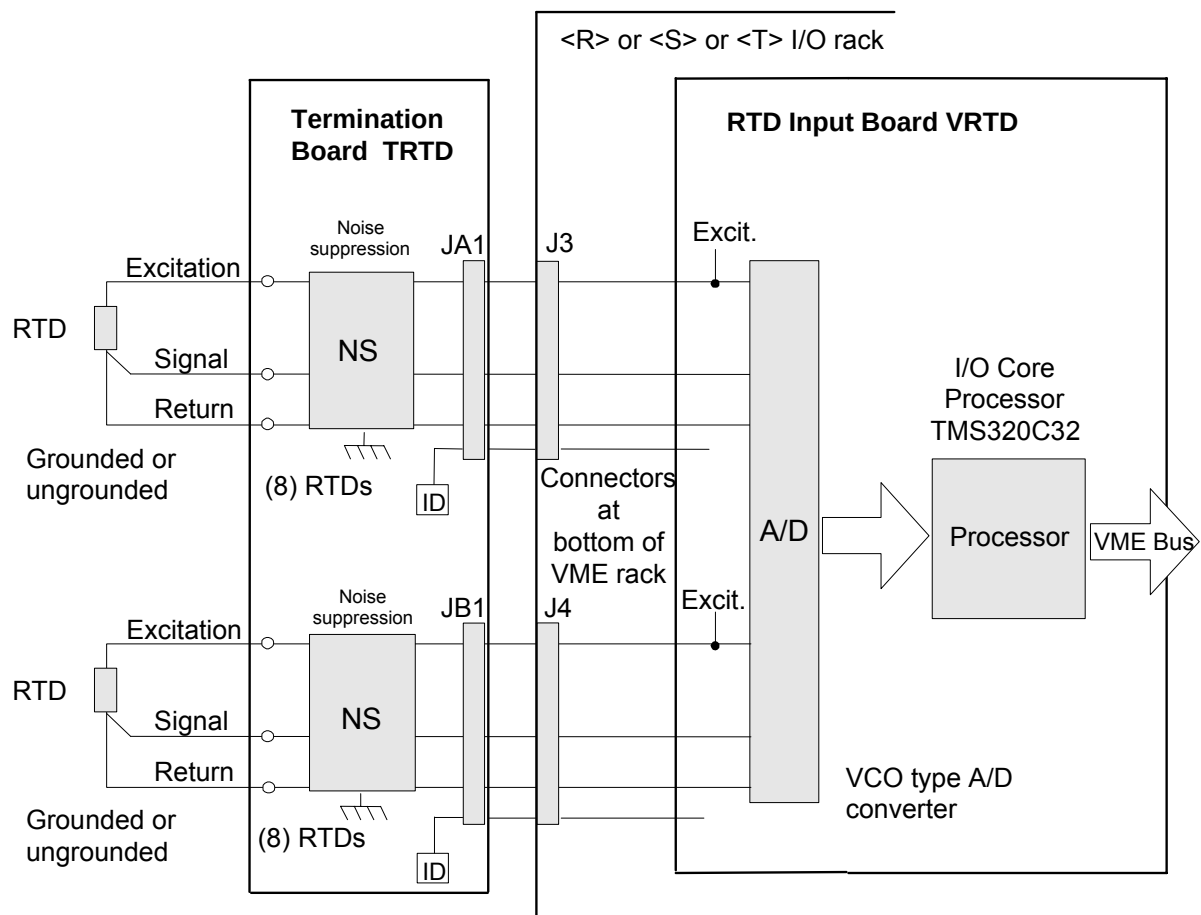
Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the section on diagnostics in this document.

Operation

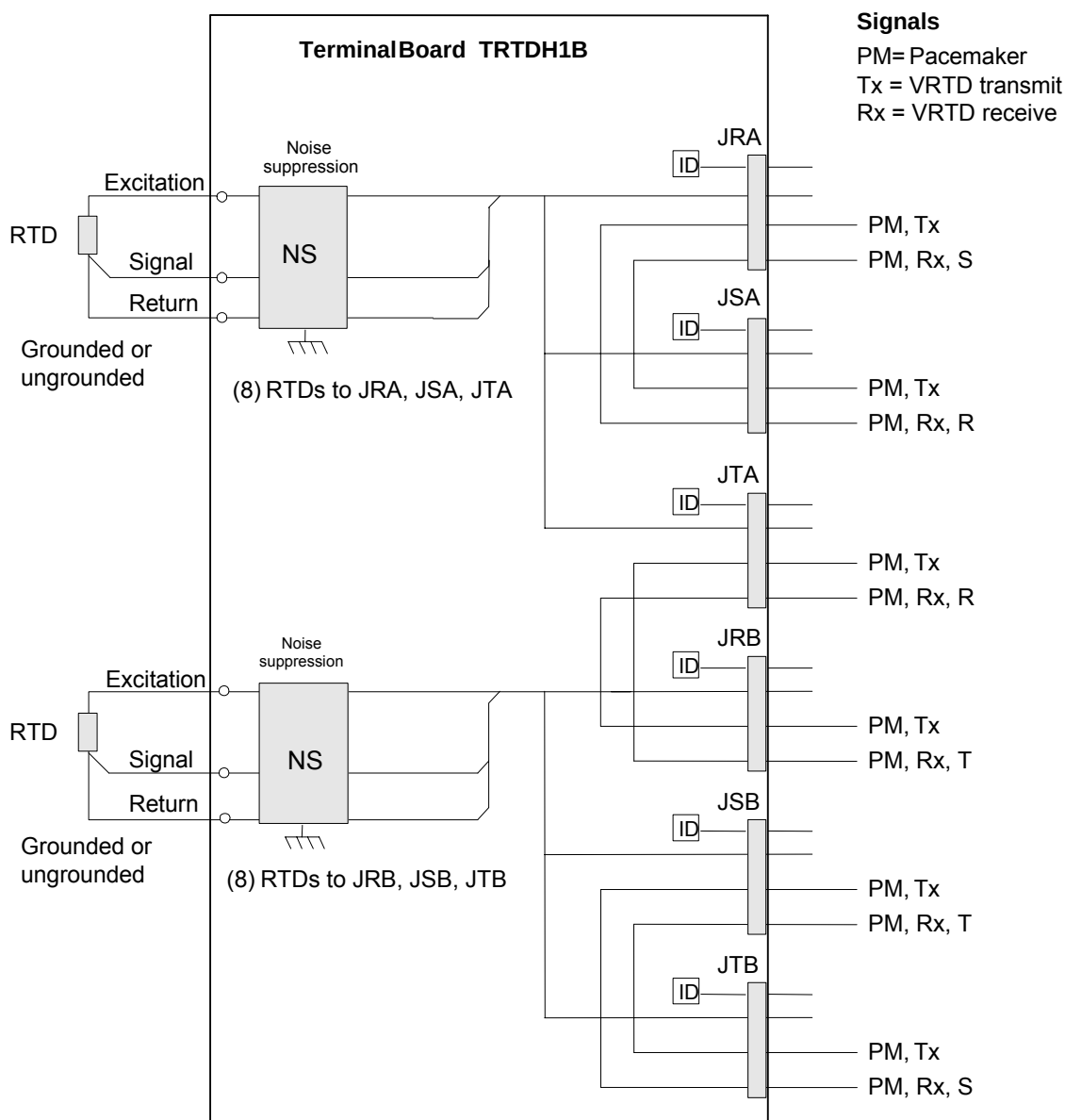
VRTD supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD through the terminal board. The resulting signal returns to VRTD. The VCO type A/D converter uses voltage to frequency converters and sampling counters. The converter samples each signal and the excitation current four times per second for normal mode scanning and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Software in the digital signal processor performs the linearization for the selection of 15 RTD types.

RTD open and short circuits are detected by out of range values. An RTD that is determined to be outside the hardware limits is removed from the scanned inputs to prevent adverse effects on other input channels. Repaired channels are reinstated automatically in 20 seconds or can be manually reinstated.

In triple modular redundant (TMR) configuration, TRTDH1B provides redundant RTD inputs by fanning the inputs to three VRTD boards in the R, S, and T racks. All RTD signals have high frequency decoupling to ground at signal entry. RTD multiplexing is coordinated by redundant pacemakers so that the loss of a single cable or VRTD does not cause the loss of any RTD signals in the control database. VRTD boards in R, S, and T read RTDs simultaneously. The RTDs read by each VRTD differ by two RTDs, such that when R reads RTD3, S reads RTD5, and T reads RTD7, and so on. This ensures that the same RTD is not excited by two VRTDs simultaneously and hence produce bad readings.



RTD Inputs and Signal Processing, Simplex System



RTD Inputs and Connections to three VRTD Processors in TMR System

Specifications

Item	Specification
Number of channels	16 channels per VRTD board
RTD types	10, 100, and 200 Ω platinum 10 Ω copper 120 Ω nickel
Span	0.3532 to 4.054 V
A/D converter resolution	14-bit resolution
Scan Time	Normal scan 250 ms (4 Hz) Fast scan 40 ms (25 Hz)
Power consumption	Less than 12 W
Measurement accuracy	See Tables

Item	Specification
Common mode rejection	Ac common mode rejection 60 dB @ 50/60 Hz Dc common mode rejection 80 dB
Common mode voltage range	±5 V
Normal mode rejection	Rejection of up to 250 mV rms is 60 dB @ 50/60 Hz system frequency for normal scan
Maximum lead resistance	15 Ω maximum two way cable resistance
Fault detection	High/low (hardware) limit check High/low (software) system limit check Failed ID chip

RTD Accuracy

RTD Type	Group Gain	Accuracy at 400 °F
120 Ω nickel	120 Ω nickel	2 °F
200 Ω platinum	Normal_ 1.0	2 °F
100 Ω platinum	Normal_ 1.0	4 °F
100 Ω platinum -51 to 240°C (- 60 °F to 400 °F)	Gain_ 2.0	2 °F
10 Ω copper	10 Ω Cu_10	10 °F

RTD Types and Ranges

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

RTD Type	Name/Standard	Range °C	Range °F
10 Ω copper	MINCO_CA GE 10 Ω Copper	-51 to +260	-60 to +500
100 Ω platinum	SAMA 100	-51 to +593	-60 to +1100
100 Ω platinum	DIN 43760	-51 to +700	-60 to +1292
	IEC-751		
	MINCO_PD		
	MINCO_PE		
	PT100_DIN		
100 Ω platinum	MINCO_PA	-51 to +700	-60 to +1292
	IPTS-68		
	PT100_PURE		
100 Ω platinum	MINCO_PB	-51 to +700	-60 to +1292
	Rosemount 104		
	PT100_USIND		
120 Ω nickel	MINCO_NA	-51 to +249	-60 to +480
	N 120		
200 Ω platinum	PT 200	-51 to +204	-60 to +400

Diagnostics

Three LEDs at the top of the VRTD front panel provide status information. The normal RUN condition is a flashing green and FAIL is a solid red. The third LED is normally off, but shows a steady orange if a diagnostic alarm condition exists in the board. Diagnostic checks include the following:

- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG_VRTD, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets the out of limit signals. In TMR systems, limit logic signals are voted and the resulting composite diagnostic is present in each controller.
- The resistance of each RTD is checked and compared with the correct value, and if high or low, a fault is created.
- Each connector has its own ID device, which is interrogated by the I/O processor board. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the connector location. If a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Note The following information is extracted from the toolbox and represents a sample of the configuration information for this board. Refer to the actual configuration file within the toolbox for specific information.

Module Parameter	Description	Choices
Configuration		
System limits	Enable or disable all system limit checking	Enable, disable
Auto reset	Enable or disable restoring of RTDs removed from scan	Enable, disable
Group A rate	Sampling rate and system frequency filter for first group of 8 inputs	4 Hz, 50 Hz filter 4 Hz, 60 Hz filter 25 Hz
Group A gain	Gain 2.0 is for higher accuracy if ohms <190, first group of 8 inputs	Normal_1.0 Gain_2.0 10 ohm Cu_10.0
Group B rate	Sampling rate and system frequency filter for second group of 8 inputs	4 Hz, 50 Hz filter 4 Hz, 60 Hz filter 25 Hz
Group B gain	Gain 2.0 is for higher accuracy if ohms <190, second group of 8 inputs	Normal_1.0 Gain_2.0 10 ohm Cu_10.0
J3J4:IS200TRTDH1C	Terminal board	Connected, not connected
RTD1	First of 16 RTDs - Board point signal	Point edit (input FLOAT)

Module Parameter	Description	Choices	
RTDRTD type	RTDs linearizations supported by VRTD;VRTD select RTDRTD or Ohms Input (unused inputs are removed from scanning)	Unused CU10 PT100_DIN PT100_PURE PT100_USIND N120 MINCO_PIA PT200 Ohms	MINCO_CA MINCO_PD MINCO_PA MINCO_PB MINCO_NA PT100_SAMA MINCO_PK
SysLim1 Enable	Enables or disables a temperature limit for each RTD,RTD can be used to create an alarm	Enable, disable	
SysLim1 Latch	Determines whether the limit condition will latch or unlatch for each RTD;RTD reset used to unlatch.	Latch, unlatch	
SysLim1 Type	Limit occurs when the temperature is greater than or equal ($\geq$), or less than or equal to ($\leq$) a preset value.	Greater than or equal Less than or equal	
System Limit 1	Enter the desired value of the limit temperature, Deg F or Ohms	-60 to 1,300	
SysLim2 Enable	Enables or disables a temperature limit which can be used to create an alarm	Enable, disable	
SysLim2 Latch	Determines whether the limit condition will latch or unlatch; reset used to unlatch.	Latch, unlatch	
SysLim2 Type	Limit occurs when the temperature is greater than or equal ($\geq$), or less than or equal to ($\leq$) a preset value.	Greater than or equal Less than or equal	
System Limit 2	Enter the desired value of the limit temperature, Deg F or Ohms	-60 to 1,300	
TMR Diff Limt	Limit condition occurs if 3 temperatures in R,S,T differ by more than a preset value; this creates a voting alarm condition.	-60 to 1,300	

Board Point Signals	Description-Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VRTD1	Board diagnostic	Input	BIT
L3DIAG_VRTD2	Board diagnostic	Input	BIT
L3DIAG_VRTD3	Board diagnostic	Input	BIT
SysLim1RTD1	System limit 1	Input	BIT
:	:	Input	BIT
SysLim1RTD16	System limit 1	Input	BIT
SysLim2RTD1	System limit 2	Input	BIT
:	:	Input	BIT
SysLim2RTD16	System limit 2	Input	BIT

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration.
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: []; Tre: []. The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: []; Tre: [] The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32- 47	RTD [] high voltage reading, Counts are Y	An RTD wiring/cabling open, or an open on the VRTD board, or a VRTD hardware problem (such as multiplexer), or the RTD device has failed.
48- 63	RTD [] low voltage reading, Counts are Y	An RTD wiring/cabling short, or a short on the VRTD board, or a VRTD hardware problem (such as multiplexer), or the RTD device has failed.
64- 79	RTD [] high current reading, Counts are Y	The current source on the VRTD is bad, or the measurement device has failed.
80- 95	RTD [] low current reading, Counts are Y	An RTD wiring/cabling open, or an open on the VRTD board, or a VRTD hardware problem (such as multiplexer), or the RTD device has failed.
96- 111	RTD [] Resistance calc high, it is Y Ohms. RTD [] has a higher value than the table and the value is Y	The wrong type of RTD has been configured or selected by default, or there are high resistance values created by faults 32 or 35, or both 32 and 35.
112- 127	RTD [] Resistance calc low, it is Y Ohms. TRD [] has a lower value than the table and the value is Y	The wrong type of RTD has been configured or selected by default, or there are low resistance values created by faults 33 or 34, or both 33 and 34.
128- 151	Voltage Circuits for RTDs, or Current Circuits for RTDs have Reference raw counts high or low, or Null raw counts high or low	Internal VRTD problems such as a damaged reference voltage circuit, or a bad current reference source, or the voltage/current null multiplexer is damaged.
152	Failed one Clock Validity Test, scanner still running. In TMR mode, the firmware tests whether the three TMR boards are synchronized and will stop scanning inputs under certain conditions	VME board, terminal board, or cable could be defective.
153	Failed one Phase Validity Test, scanner still running. In TMR mode, the firmware tests whether the three TMR boards are synchronized and will stop scanning inputs under certain conditions	VME board, terminal board, or cable could be defective.

Fault	Fault Description	Possible Cause
154	Failed both Clock Validity Tests, scanner shutdown. In TMR mode, the firmware tests whether the three TMR boards are synchronized and will stop scanning inputs under certain conditions	VME board, terminal board, or cable could be defective.
155	Terminal Board connection(s) wrong. Cables crossed between <R>, <S>, and <T>	Check cable connections.
156	25 Hz Scan not Allowed in TMR Mode, please reconfigure	Configuration error. Choose scan of 4 Hz_50 Hz Fltr or 4 Hz_60 Hz Fltr.
160-255	Logic Signal [] Voting mismatch. The identified signal from this board disagrees with the voted value.	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
256-271	Input Signal [] Voting mismatch, Local [], Voted []. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TRTD RTD Input

Functional Description

The RTD Input (TRTD) terminal board accepts 16, three-wire RTD inputs. These inputs are wired to two barrier type terminal blocks. The inputs have noise suppression circuitry to protect against surge and high frequency noise. TRTD communicates with one or more I/O processors, which convert the inputs to digital temperature values and transfer them to the controller.

There are four versions of TRTD as follows:

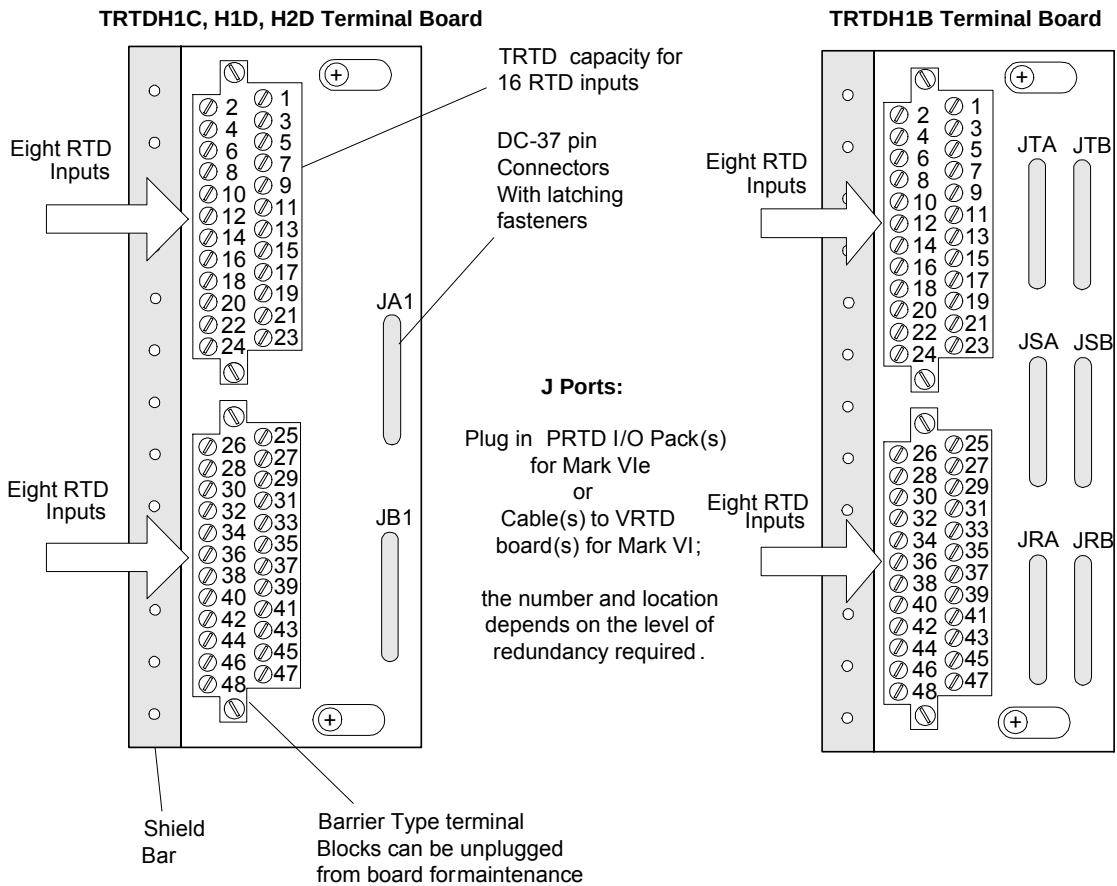
- TRTDH1B is a TMR version that fans out the signals to three VRTD boards using six DC-type connectors.
- TRTDH1C is a simplex board with two DC-type connectors for VRTD.
- TRTDH1D is a simplex board with two DC-type connectors for PRTD, normal scan.
- TRTDH2D is a simplex board with two DC-type connectors for PRTD, fast scan.

Mark VI Systems

In the Mark* VI system, TRTDH1B and TRTDH1C works with the VRTD processor and supports simplex and TMR applications. One TRTDH1C connects to the VRTD with two cables. In TMR systems, TRTDH1B connects to three VRTD processors with six cables.

Mark VIe Systems

In the Mark VIe system, TRTDH1D and TRTDH2D works with the PRTD I/O pack and support simplex applications only. Two PRTD packs plug into the TRTD for a total of 16 inputs.



RTD Input Terminal Boards

Installation

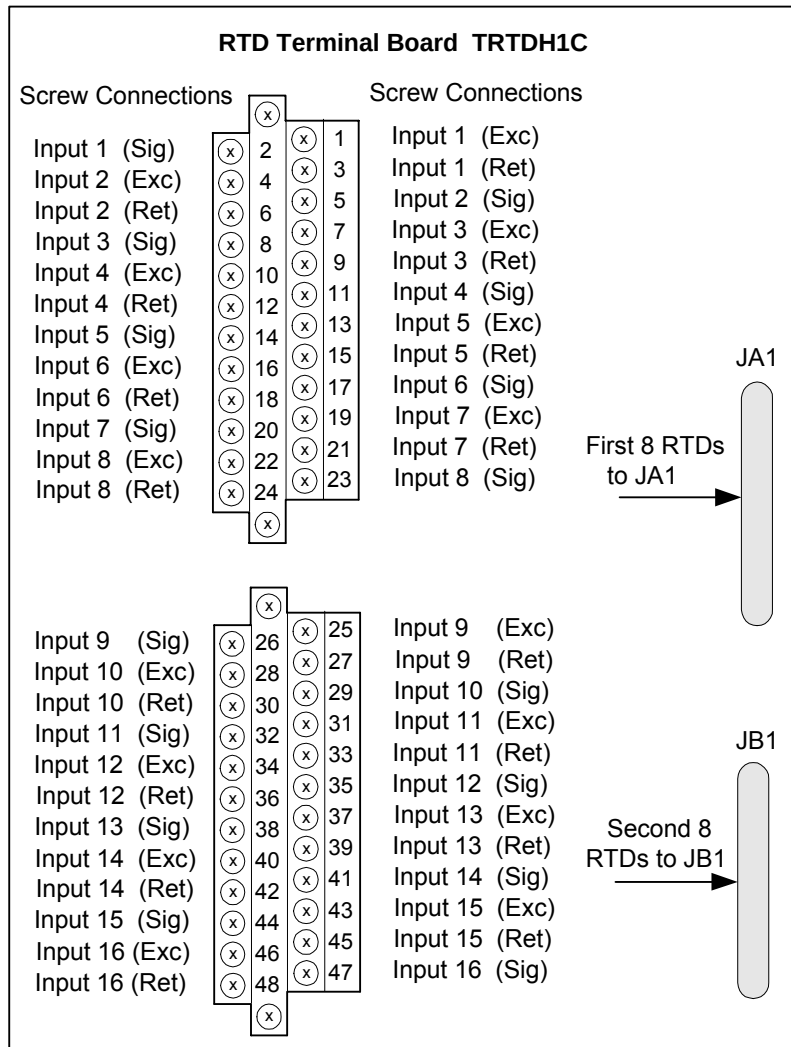
Connect the wires for the 16 RTDs directly to the two terminal blocks on the terminal board. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located immediately to the left of each terminal block.



Caution

For CE mark applications, double-shielded wire must be used. All shields must be terminated at the shield terminal strip. Do not terminate shields located at the end device.

In a TMR Mark VI system, TRTDH1B provides redundant RTD inputs by fanning the inputs to three VRTD boards in the R, S, and T racks. The inputs meet the same environmental, resolution, suppression, and function requirements and codes as the TRTDH1C terminal board; however, the fast scan is not available.



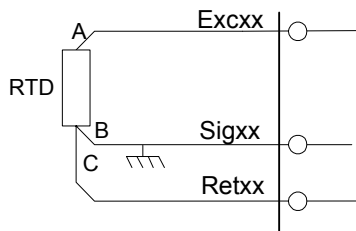
J-Port Connections

Plug in PRTD I/O Pack(s) for Mark VIe

or

Cable to VRTD I/O board(s) for Mark VI;

The number and location depends on the number of inputs required.



Application Note:

- Optional Ground: connect the B wire to ground;
- RTD Group wiring, that is sharing the B wire; tie the B wires together at the RTDs, tie the Sigxx signals together at the TRTD terminal board, and interconnect with one wire.

TRTDH1C RTD Terminal Board Wiring

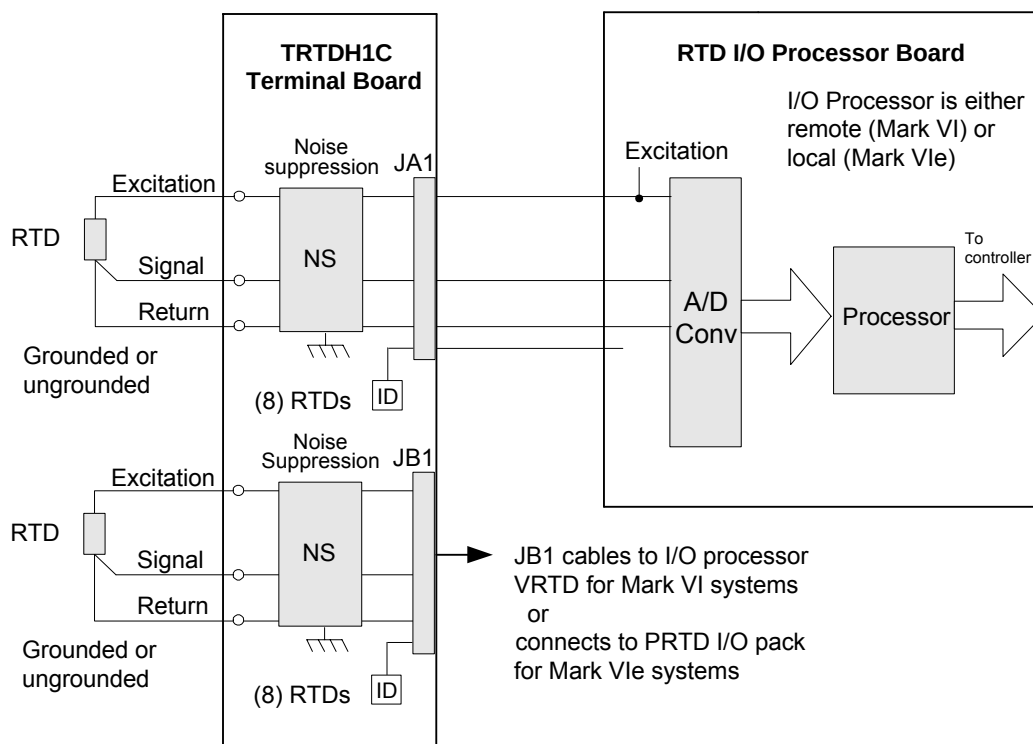
Operation

TRTD supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The 16 RTDs can be located up to 300 m (984 ft) from the turbine control cabinet with a maximum two-way cable resistance of 15 Ω .

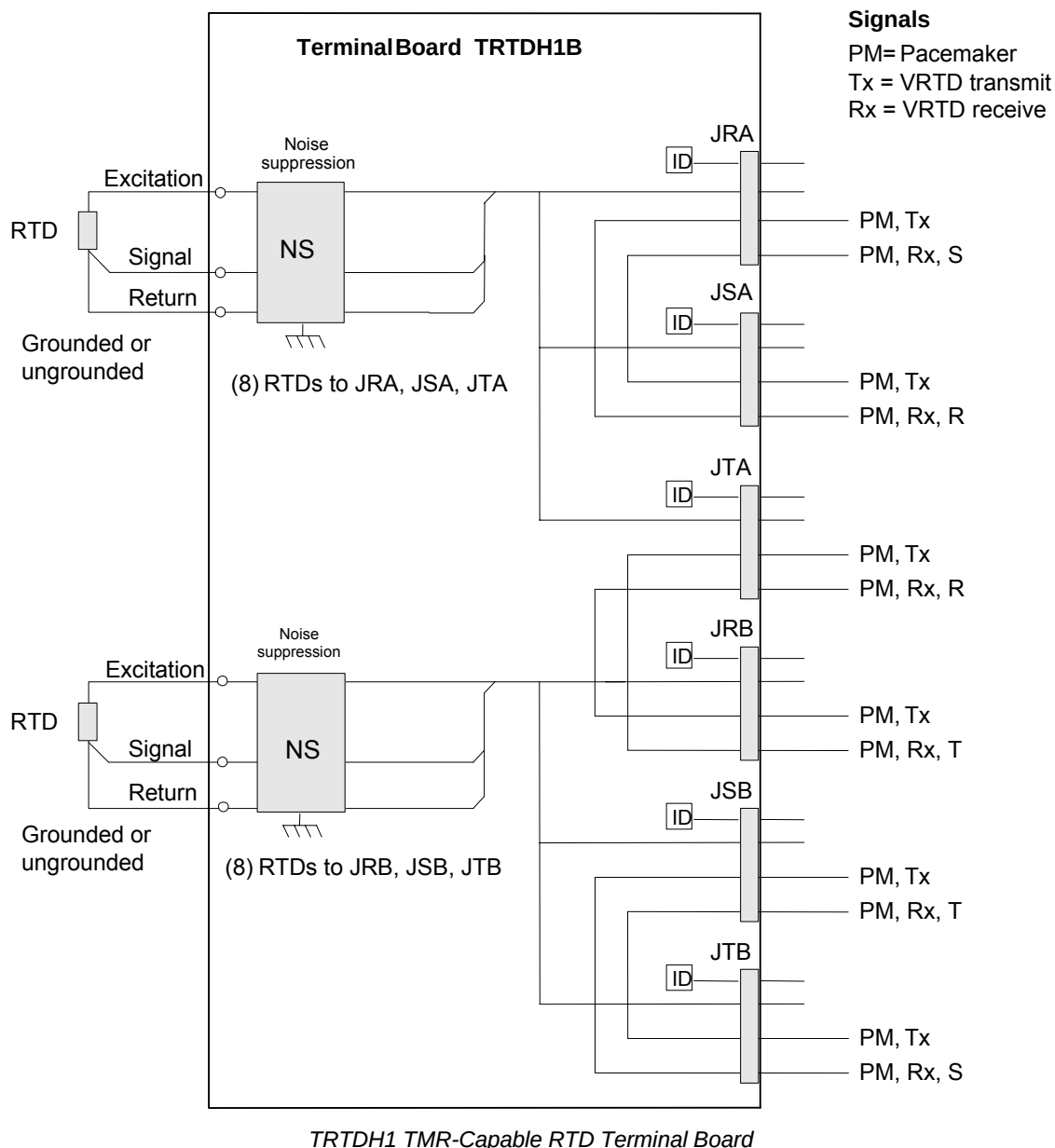
The A/D converter in the I/O processor samples each signal and the excitation current four times per second for normal mode scanning and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Software performs the linearization for the selection of 15 RTD types.

RTD open and short circuits are detected by out-of-range values. An RTD that is determined to be outside the hardware limits is removed from the scanned inputs to prevent adverse effects on other input channels. Repaired channels are reinstated automatically in 20 seconds or can be manually reinstated.

All RTD signals have high-frequency decoupling to ground at signal entry. RTD multiplexing in the I/O processor is coordinated by redundant pacemakers so that the loss of a single cable or I/O processor does not cause the loss of any RTD signals in the control database.



TRTD (Simplex) Inputs and Signal Processing



Specifications

Item	Specification
Number of channels	Eight channels per terminal board
RTD types	10, 100, and 200 Ω platinum 10 Ω copper 120 Ω nickel
Span	0.3532 to 4.054 V
Maximum lead resistance	15 Ω maximum two-way cable resistance
Fault detection	High/low (hardware) limit check High/low (software) system limit check Failed ID chip

RTD Accuracy

RTD Type	Group Gain	Accuracy at 400 °F
120 Ω nickel	120 Ω nickel	2 °F
200 Ω platinum	Normal_ 1.0	2 °F
100 Ω platinum	Normal_ 1.0	4 °F
100 Ω platinum -51 to 240°C (- 60 °F to 400 °F)	Gain_ 2.0	2 °F
10 Ω copper	10 Ω Cu_10	10 °F

RTD Types and Ranges

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

RTD Type	Name/Standard	Range °C	Range °F
10 Ω copper	MINCO_CA GE 10 Ω Copper	-51 to +260	-60 to +500
100 Ω platinum	SAMA 100	-51 to +593	-60 to +1100
100 Ω platinum	DIN 43760	-51 to +700	-60 to +1292
	IEC-751		
	MINCO_PD		
	MINCO_PE		
	PT100_DIN		
100 Ω platinum	MINCO_PA	-51 to +700	-60 to +1292
	IPTS-68		
	PT100_PURE		
100 Ω platinum	MINCO_PB	-51 to +700	-60 to +1292
	Rosemount 104		
	PT100_USIND		
120 Ω nickel	MINCO_NA	-51 to +249	-60 to +480
	N 120		
200 Ω platinum	PT 200	-51 to +204	-60 to +400

Diagnostics

Diagnostic checks include the following:

- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG_XXXX, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets the out of limit signals. In TMR systems, limit logic signals are voted and the resulting composite diagnostic is present in each controller.
- The resistance of each RTD is checked and compared with the correct value, and if high or low, a fault is created.
- Each connector has its own ID device, which is interrogated by the I/O processor board. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the connector location. If a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

DRTD Simplex RTD Input

Functional Description

The Simplex RTD Input (DRTD) terminal board is a compact RTD terminal board designed for DIN-rail mounting. The board has eight RTD inputs and connects to the VRTD processor board with a single cable. This cable is identical to those used on the larger TRTD terminal board. The terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space. Two DRTD boards can be connected to VRTD for a total of 16 temperature inputs. Only a simplex version of the board is available.

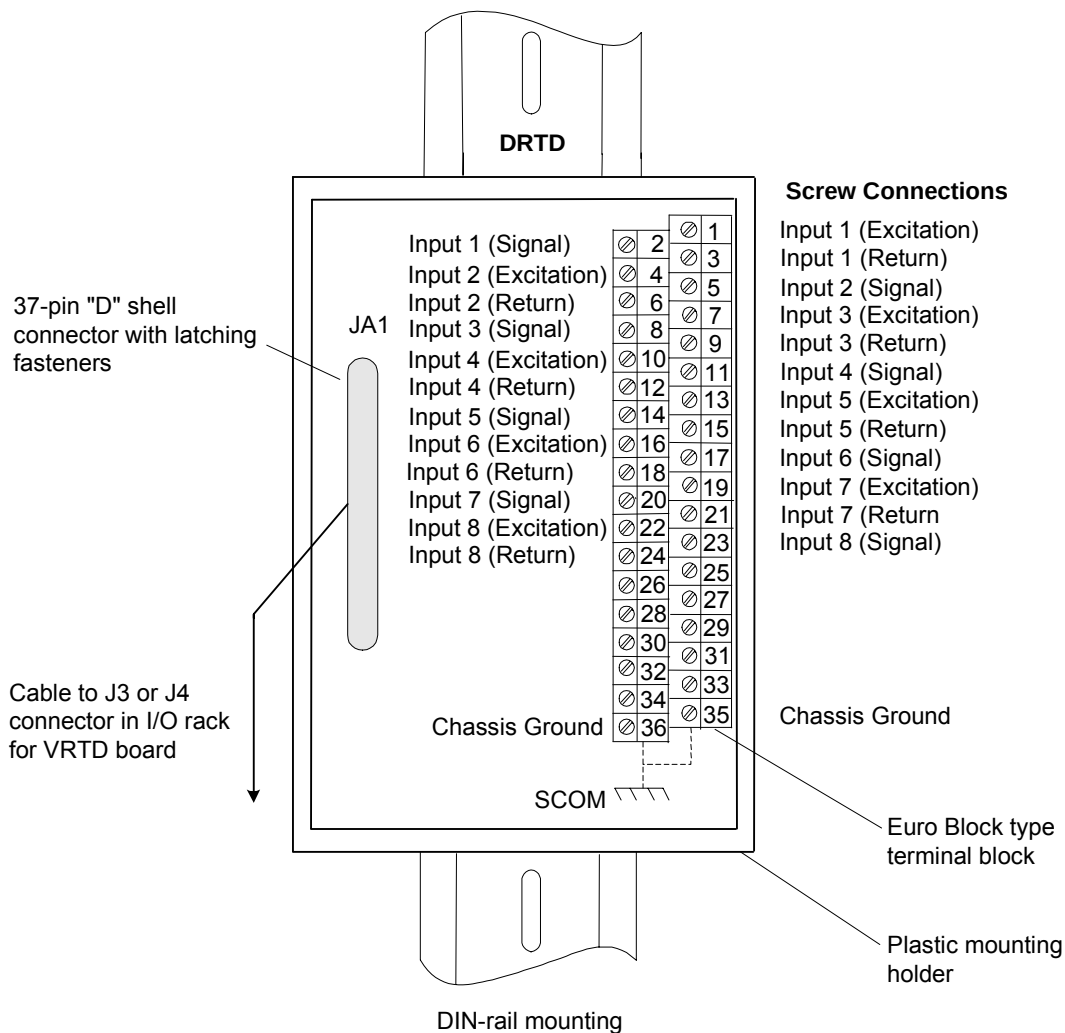
Note The DRTD board does not work with the PRTD I/O pack.

Installation

Note There is no shield terminal strip with this design.

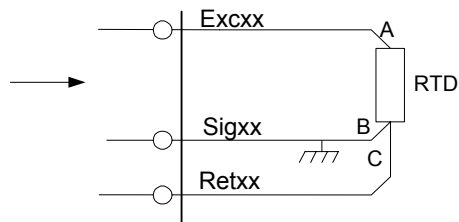
Mount the plastic holder on the DIN-rail and slide the DRTD board into place. Connect the wires for the eight RTDs directly to the terminal block. The Euro-Block type terminal block has 36 terminals and is permanently mounted on the terminal board. Typically #18 AWG wires (shielded twisted triplet) are used. Terminals 25 through 34 are spares. Two screws, 35 and 36, are provided for the SCOM (ground) connection, which should be as short a distance as possible.

Note SCOM must be connected to ground.



Application Notes:

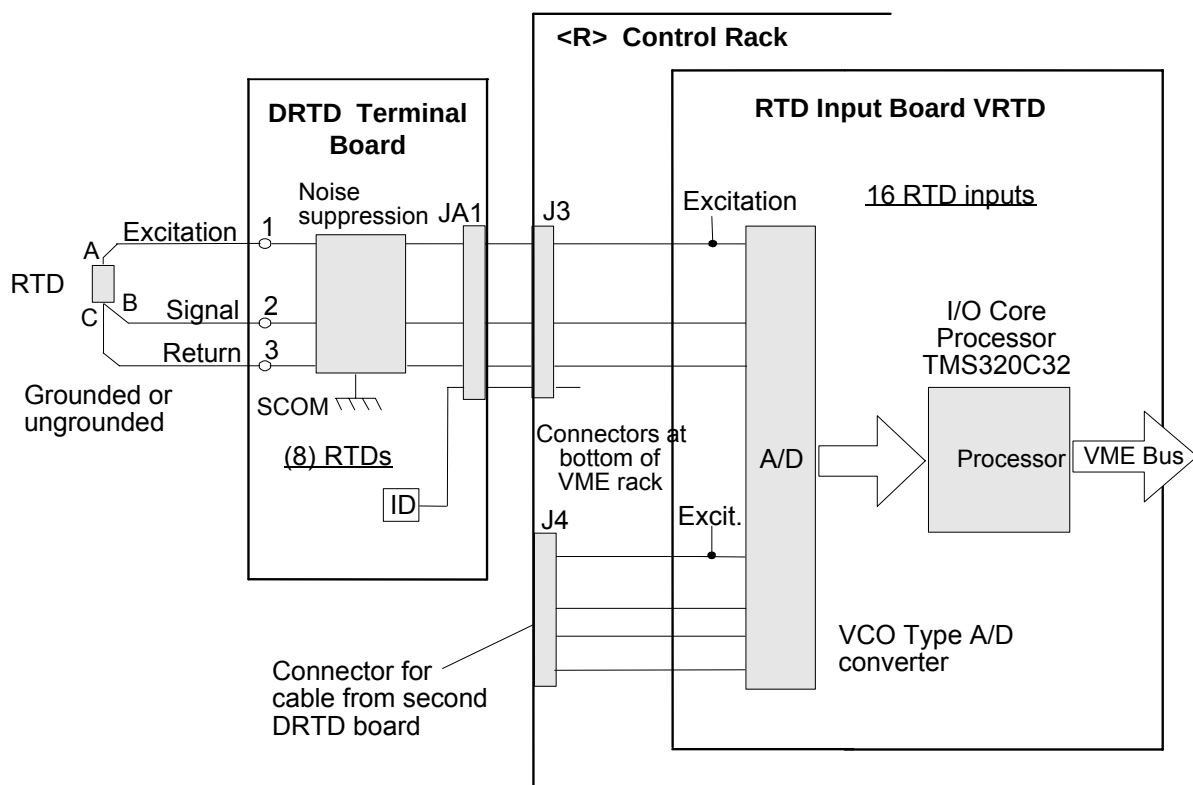
- Optional Ground: connect the "B" wire to ground;
- RTD Group wiring, that is sharing the "B" wire; tie the "B" wires together at the RTDs, tie the "Sigxx" signals together at the TRTD termination board, and interconnect with one wire.



DRTD Board Wiring and Cabling

Operation

The noise suppression on DRTD is similar to that on TRTD. High-density Euro-Block type terminal blocks are permanently mounted to the board, with two screw connections for the ground connection (SCOM). An on-board ID chip identifies the board to VRTD for system diagnostic purposes.



DRTD Board and VRTD Input Board

DRTD supplies a 10 mA dc multiplexed (not continuous) excitation current to each RTD, which can be grounded or ungrounded. The eight RTDs can be located up to 300 meters (984 feet) from the turbine control cabinet with a maximum two-way cable resistance of 15 Ω .

VRTD's VCO type A/D converter uses voltage to frequency converters and sampling counters. The converter samples each signal and the excitation current four times per second for normal mode scanning and 25 times per second for fast mode scanning, using a time sample interval related to the power system frequency. Software in the digital signal processor performs the linearization for the selection of 15 RTD types.

RTD open and short circuits are detected by out of range values. An RTD that is determined to be outside the hardware limits is removed from the scanned inputs to prevent adverse effects on other input channels. Repaired channels are reinstated automatically in 20 seconds or can be manually reinstated.

Specifications

Item	Specification
Number of channels	Eight channels per terminal board
RTD types	10, 100, and 200 Ω platinum 10 Ω copper 120 Ω nickel
Span	0.3532 to 4.054 V
Maximum lead resistance	15 Ω maximum two-way cable resistance
Fault detection	High/low (hardware) limit check High/low (software) system limit check Failed ID chip

RTD Types and Ranges

RTD inputs are supported over a full-scale input range of 0.3532 to 4.054 V. The following table shows the types of RTD used and the temperature ranges.

RTD Type	Name/Standard	Range °C	Range °F
10 Ω copper	MINCO_CA GE 10 Ω Copper	-51 to +260	-60 to +500
100 Ω platinum	SAMA 100	-51 to +593	-60 to +1100
100 Ω platinum	DIN 43760 IEC-751 MINCO_PD MINCO_PE PT100_DIN	-51 to +700	-60 to +1292
100 Ω platinum	MINCO_PA IPTS-68 PT100_PURE	-51 to +700	-60 to +1292
100 Ω platinum	MINCO_PB Rosemount 104 PT100_USIND	-51 to +700	-60 to +1292
120 Ω nickel	MINCO_NA N 120	-51 to +249	-60 to +480
200 Ω platinum	PT 200	-51 to +204	-60 to +400

Diagnostics

Diagnostic checks include the following:

- Each RTD type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the input's hardware limits is set, it creates a composite diagnostic alarm, L3DIAG_XXXX, referring to the entire board. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each RTD input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets the out of limit signals. In TMR systems, limit logic signals are voted and the resulting composite diagnostic is present in each controller.
- The resistance of each RTD is checked and compared with the correct value, and if high or low, a fault is created.
- Each connector has its own ID device, which is interrogated by the I/O processor board. The terminal board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the connector location. If a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

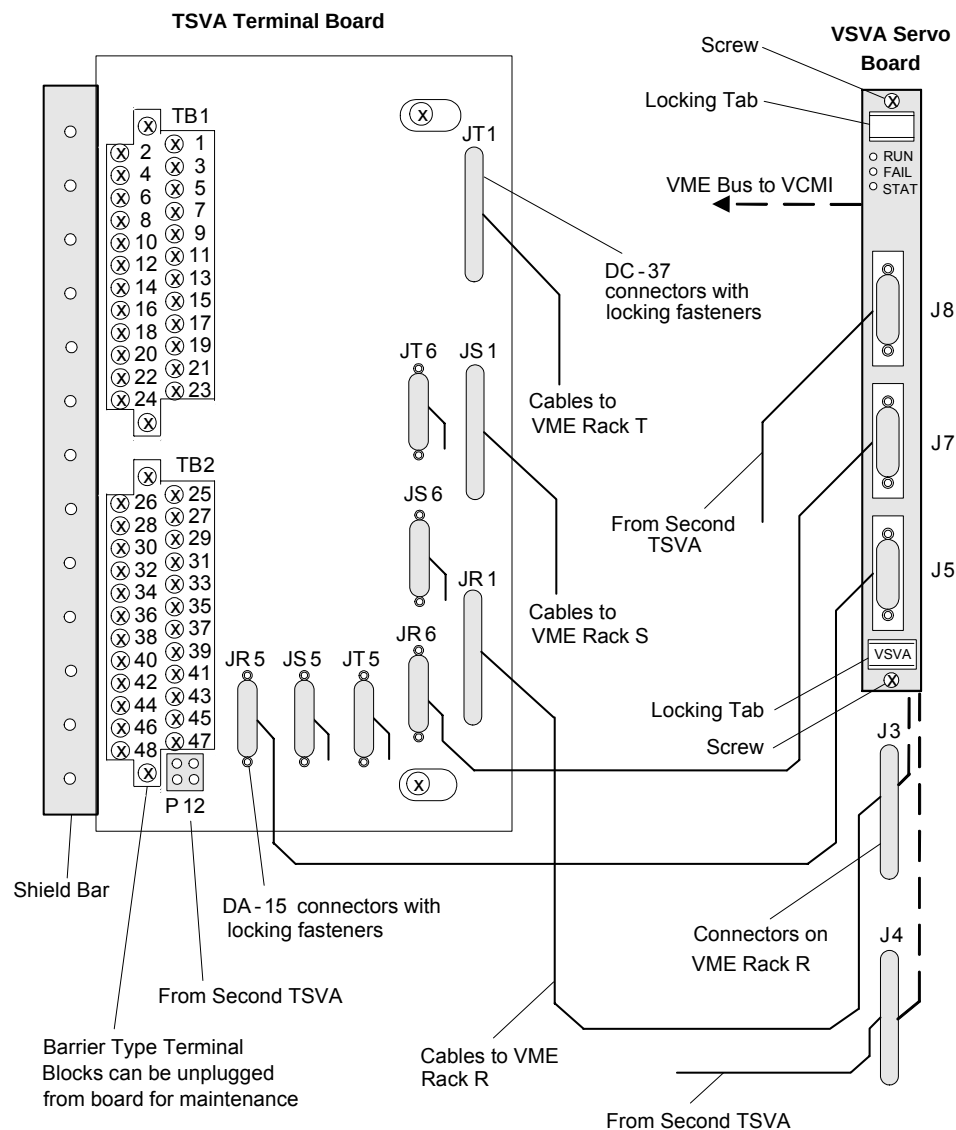
Notes

VSVA Servo Control

VSVA Servo Control

Functional Description

The Servo Control (VSVA) board controls up to four electro-hydraulic servo valves that start the steam/fuel valves. These four channels are divided between two TSVA terminal boards. The VSVA/TSVA boards provide triple modular redundancy (TMR) control solution for retrofit applications where 3-coil servo valves are not present. Valve position is measured with linear variable differential transformers (LVDT) or alinear variable differential reluctance (LVDR) sensor. Applications allowing dual coil servo valve and using either single or dual LVDT/LVDR sensors are supported.



VSVA Processor Board, TSVA Terminal Board and Interconnect Cabling

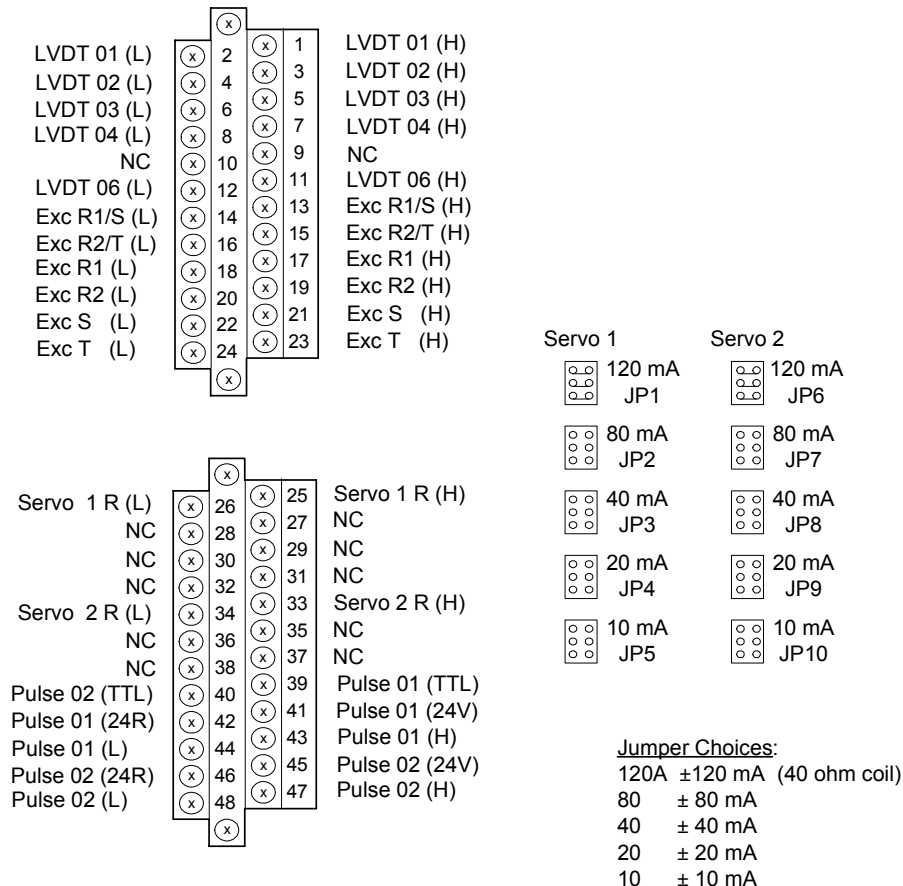
Installation

➤ To install the V-type board

- 1 Power down the controller by turning off the power supply.
- 2 Loosen the top and bottom screws on the existing servo board, or cover plate.
- 3 Remove existing board (by pushing up on top extraction tab and pushing down on lower extraction tab) or remove cover plate.
- 4 Ensure the board is in the top and bottom tracks.
- 5 Fully inset the board by pushing in at the top and bottom.
- 6 Lock the board in place by pushing down on the top and bottom locking tabs.
- 7 Tighten the top and bottom screws.
- 8 Power up the controller by turning on the power supply.

Note Sensors and servo valves are wired directly to two removable barrier type terminal blocks mounted on each terminal board. Each block is held down with two screws, and has 24 terminals accepting up to two #12 AWG wires each. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block.

**Combined Servo Output/LVDT Terminal Board
TSVAH1A**



Up to two #12 AWG wires per
point with 300 volt insulation

Terminal blocks can be unplugged
from terminal board for maintenance

TSVA Terminal Board

Operation

The VSVA servo board contains I/O signal conditioning electronics along with a microprocessor providing four channels of servo loop control with bi-directional servo current outputs. Valve position is typically measured with either four wire LVDT or three wire LVDR Sensors. Ten LVDT/LVDR position inputs, two pulse rate inputs and four LVDT/LVDR excitation source outputs are supported on the VSVA/TSVA boards.

The VSVA/TSVA boards provide a TMR servo control solution using fanned in and out control and feedback signals needed to support retrofits of older simplex control applications which commonly have dual coil servo valves. The two coils are either tied in parallel or split, and have either one or two LVDT/LVDR position feedback sensors per valve.

One, two or three LVDT/LVDR valve position inputs can be assigned to a servo control loop from 10 LVDT/LVDR inputs available for all four servo loops. Two Pulse Rate inputs could be assigned for servo control loop applications requiring flow rate measurement feedback.

The pulse rate inputs can be used for turbine speed control. It is important to ensure that speed input signals meet the VSVA board input sensitivity-versus-frequency specification and that they fall within a 2 Hz to 12 kHz frequency band.

VSVA boards located in the R, S and T VME racks provide individual (local) servo current outputs that are combined on the TSVA terminal board to produce a TMR output. A current sense resistor in series with the total servo current output is located on the TSVA board providing total current feedback to the VSVA current regulator circuits. As long as any two of the three VSVA boards are online and operating without faults, the combined servo output loop will continue to function, allowing online replacement of any one of the three VSVA boards. Refer to the figures for VSVA/TSVA inputs and outputs.

Each VSVA servo control loop output is equipped with an individual suicide relay under firmware control. It opens the output current signal to the TSVA terminal board during rack power off, during system startup, for over-current faults, and for out-of-range position feedback faults.

Inputs, outputs, and critical internal VSVA board functions are continuously monitored online for out-of-limit conditions. The VSVA servo board generates diagnostic alarms. It sends associated fault messages to the operator interface as fault conditions are detected. Green, red, and yellow LEDs on the VSVA front panel display the board-operating status.

Redundant one-bit serial communication busses allow the R, S, and T VSVA boards to share critical status parameters. The decision to suicide servo current loop outputs, select LVDT/LVDR excitation switchover sources, and check all three boards are using the same parameters is continuously shared between VSVA boards over the serial busses.

The TSVA terminal board contains two removable I/O terminal blocks. The terminal screws, each capable of accepting two #12 AWG wires, provide the interface I/O customer sensor wiring. Each TSVA supports two servo control loop outputs plus associated I/O feedback sensors. Signals are fanned in and out on the TSVA board to and from the three VSVA (R, S, and T) boards. LVDT/LVDR inputs, excitation outputs, pulse rate inputs and servo loop outputs are voltage-clamped and passively filtered (suppressed) on the TSVA board. Servo cable lengths, up to 300 m (984 ft), are supported with a maximum two-way cable resistance of 15 Ω .

Three TMR VSVA boards are connected to either one or two TSVA terminal boards using cables, with DC-37 pin connectors on each end, between the JR1, JS1, and JT1 connectors and the R, S, or T rack J3 or J4 backplane connectors. VSVA front panel connectors, J7 and J8, supply feed back signals. They are connected to the TSVA board JR6, JS6 or JT6 receptacles using twisted shielded pair cables with DA-15 connectors. J7 and J3 must connect to one of the TSVA boards, while J8 and J4 connect to the second TSVA board, if used. Pulse rate inputs are fanned to the TMR VSVA boards through twisted shielded pair cables, with DA-15 connectors, between J5 receptacles on the three VSVA front panels and JR5, JS5 and JT5 receptacles on the TSVA. When Pulse Rate inputs are used, J5 on the VSVA board must be connected to JR5 on the TSVA terminal board. JR1 must be connected to J3 on the VME rack using cables with DC-37 pin connectors. If Pulse rate inputs are not required, J5 can be left unconnected. If J5 is used, then the J12 4 pin cable must connect the two TSVA boards.

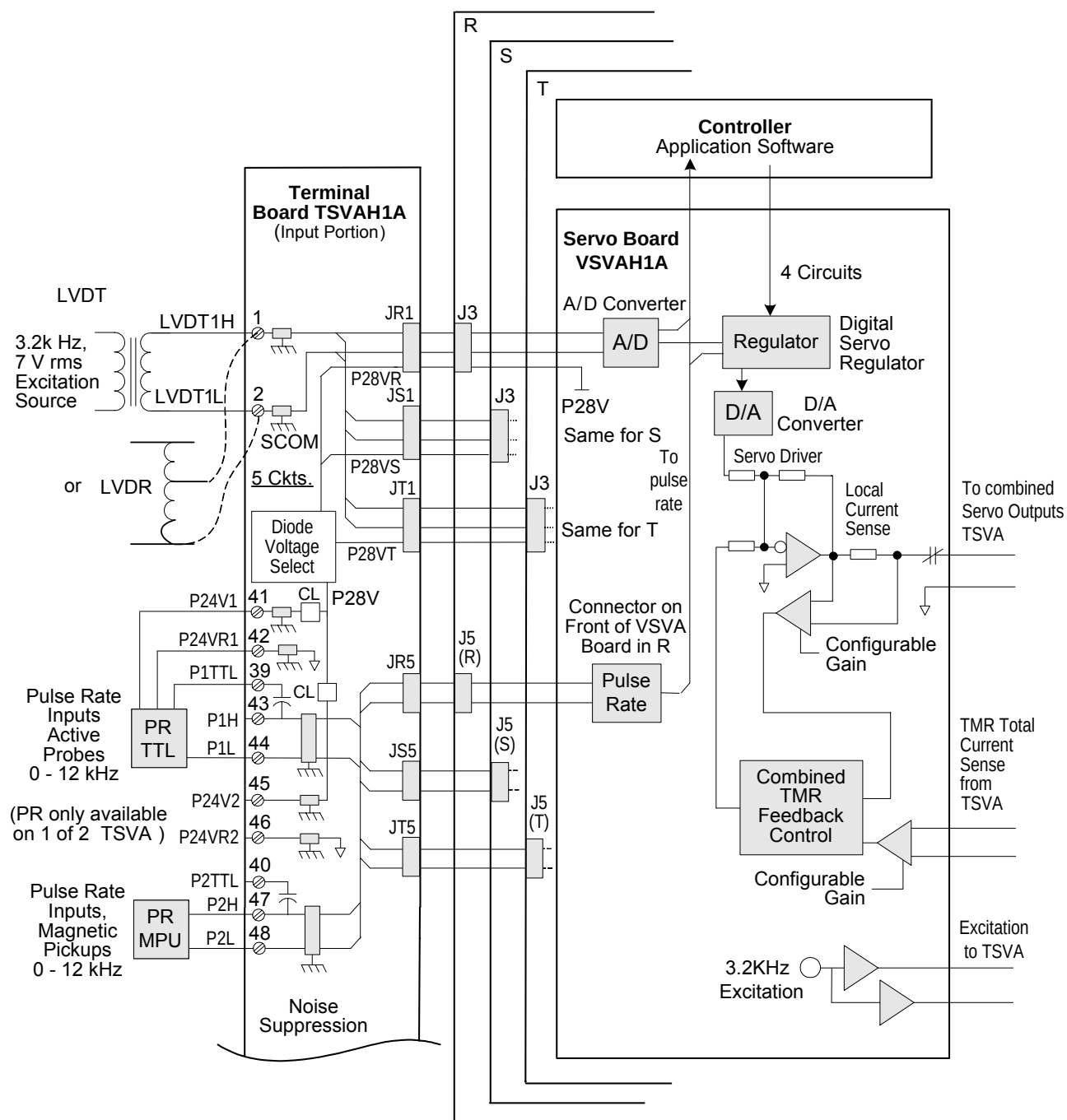
Jumpers on the TSVA are configured to select appropriate in-line resistors that limit servo output current overdrive depending on coil resistance. Jumpers JP1 through JP5 and JP6 through JP10 select resistors compatible with full-scale servo output current ranges of 10 mA, 20 mA, 40 mA, 80 mA, or 120 mA for servo output channels. Refer to the figures for VSVA/TSVA inputs and outputs.

TSVA provides five channels of LVDT/LVDR differential inputs and two channels of redundant automatically switched-over LVDT/LVDR excitation outputs at 7.10 Vrms at 3.2 kHz.

TSVA provides redundant LVDT/LVDR excitation switchover relays to automatically select a good excitation source from an R, S, or T VSVA board. This feature ensures that a failure of a single VSVA board will not result in the loss-of-excitation output on the TSVA board. It also allows any one of the R, S, or T racks to be powered down to support online VSVA board replacement. TSVA excitation outputs to LVDT/LVDR sensors minimize effects on servo control when either the high or low side of the input or output windings are inadvertently shorted to ground.

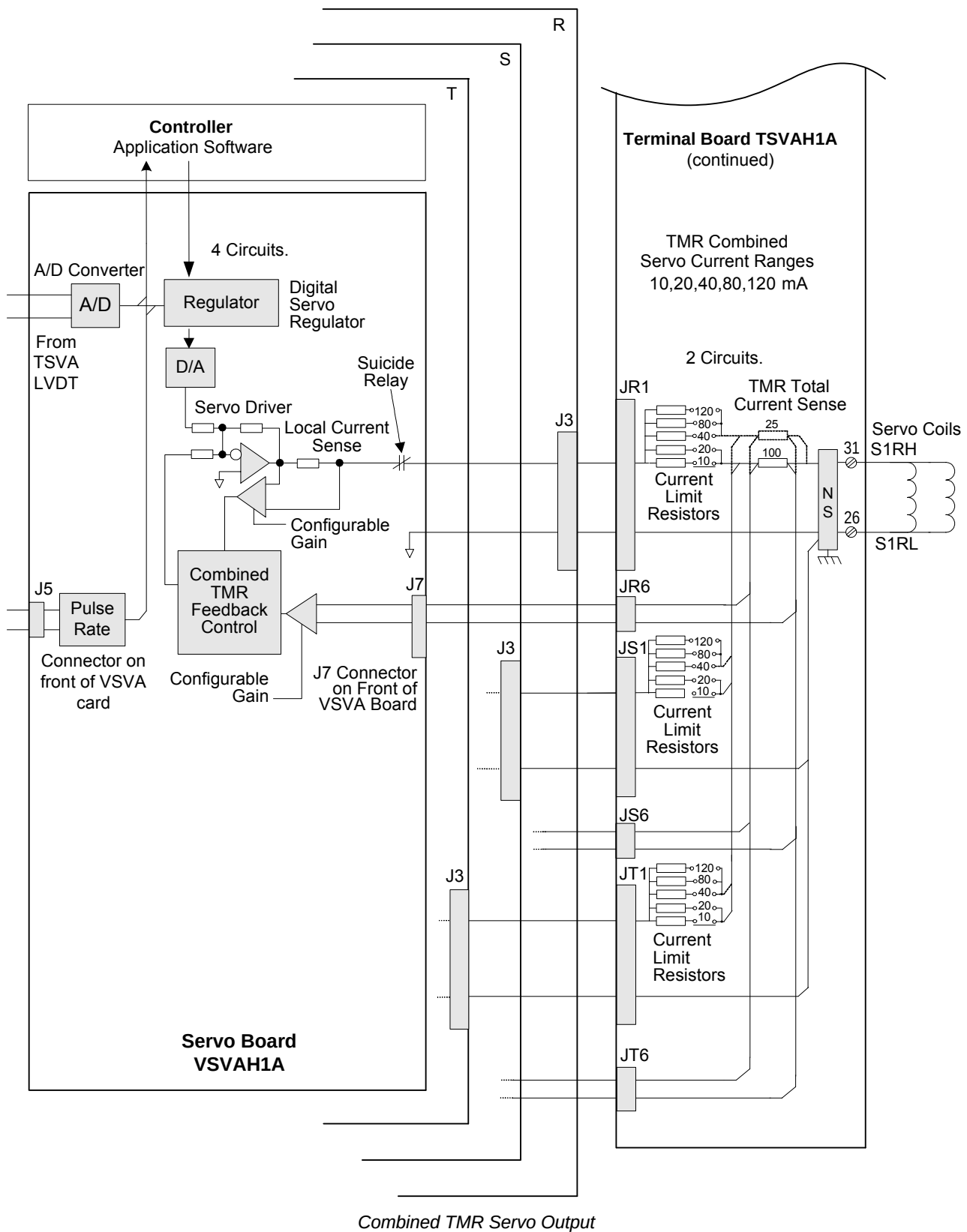
This excitation output switchover feature is especially useful for retrofit applications using a single LVDT/LVDR position sensor. The excitation switchover source selection commands are controlled by software on the R, S, and T VSVA boards, which continuously monitor the excitation switchover outputs. A redundant hardware voter circuit on the TSVA board ensures that a single fault on a VSVA board or rack power-off condition will not result in loss-of -excitation output.

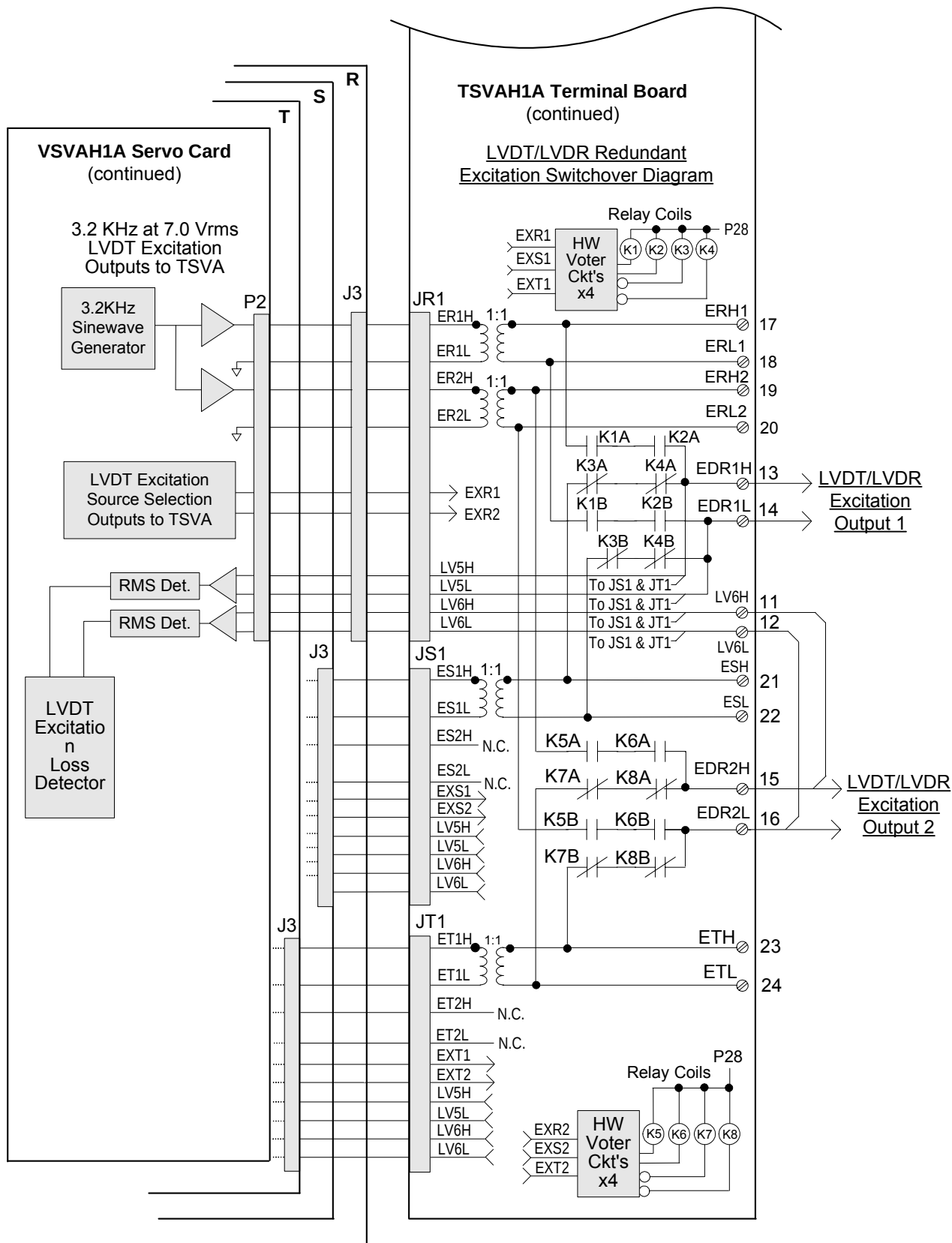
The two pulse rate circuits on the TSVA board have two current-limited 24 V dc outputs, at 40 mA each, to supply power to active pulse rate input devices.



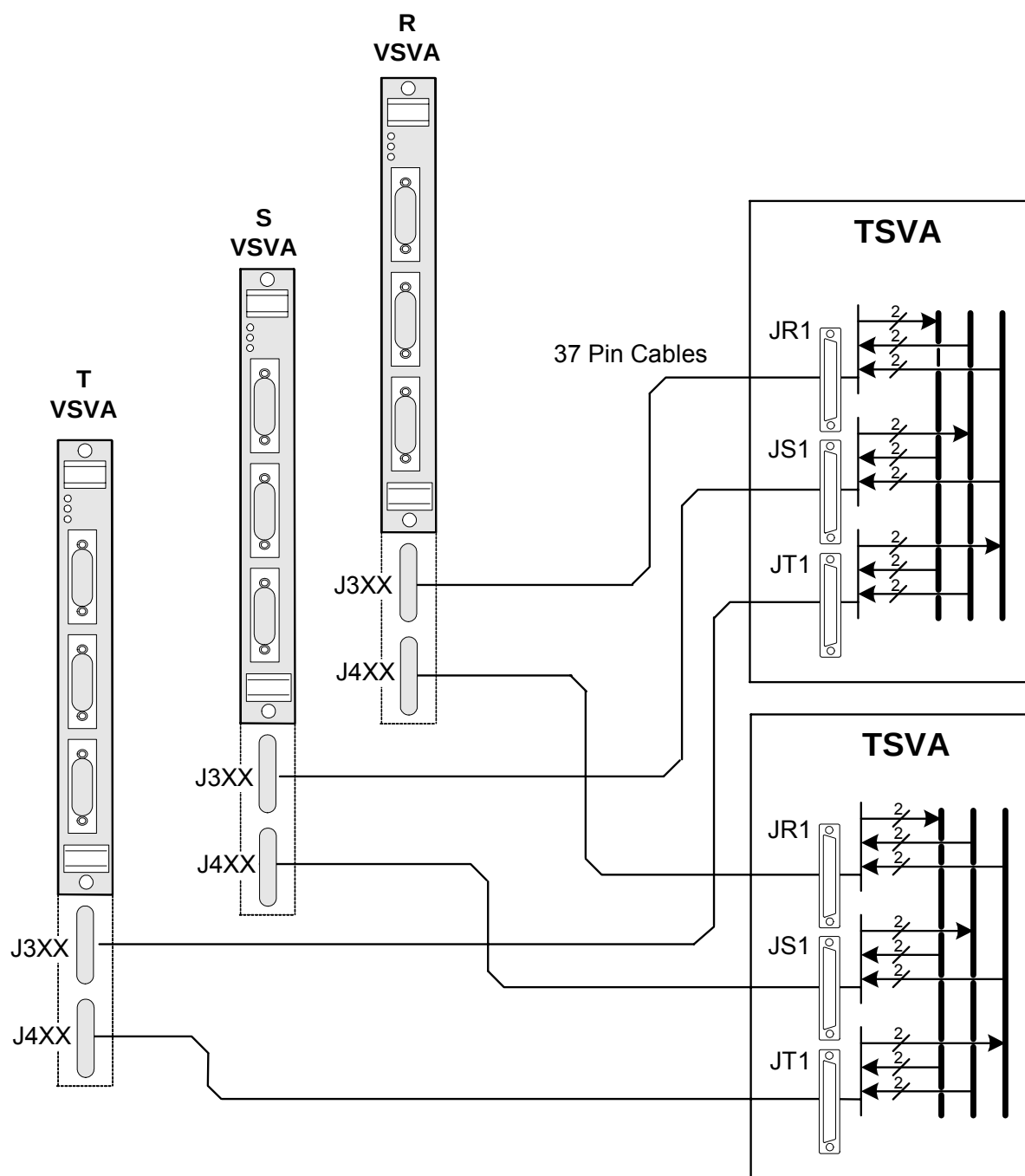
LVDT and Pulse Rate Inputs, TMR Servo Outputs

Note Signal pairs from LVDT/LVDR pulse rate devices are twisted shielded pairs.





LVDT Excitation Swchover Source Selection Relays



VSVA-to-VSVA Serial Communications Bus Interconnection Diagram

VSVA Function	Data Type	State Definition	VSVA to VSVA Transfer Rate
Servo outputs 1-4 over-current status	Servo over-current status bit	1 = Over current 0 = Normal	14.4 ms
Servo outputs 1-4 local current polarity	Servo local current polarity status bit	1 = Positive 0 = Negative	14.4 ms
LVDT excitation - out 1 and 3 source selection	LVDT source selection status bit	1 = S 0 = R1	432 ms
LVDT excitation - out 2 and 4 source selection	LVDT source selection status bit	1 = T 0 = R2	432 ms
Check of R, S, and T VSVA critical configuration parameter match at power-up	Cyclic redundancy check (CRC) of critical configuration parameters	R, S, and T CRCs must match at power-up	432 ms

Examples that define both internal cable and customer sensor wire interconnections to VSVA and TSVA boards are shown in the following five examples.

Example 1: Two Dual Coil Servo Valves and Single LVDT/LVDR

The first example supports two dual coil servo valves with coils electrically connected in parallel, and a single LVDT/LVDR position feedback device per valve. Only one servo valve and associated feedback device are connected to each one of the two TSVA boards. This supports online TSVA replacement with the loss of only one servo valve function. Three TMR VSVA boards plus two TSVA boards control a total of two servo valves plus associated LVDT/LVDR position feedback devices.

This configuration supports steam turbine control retrofit applications that can continue to operate with the loss of any single servo controlled steam valve. No single point fault, including online replacement of a TSVA board, will result in losing more than one servo valve control function. VSVA boards and cables can be replaced online without the losing servo output functions.

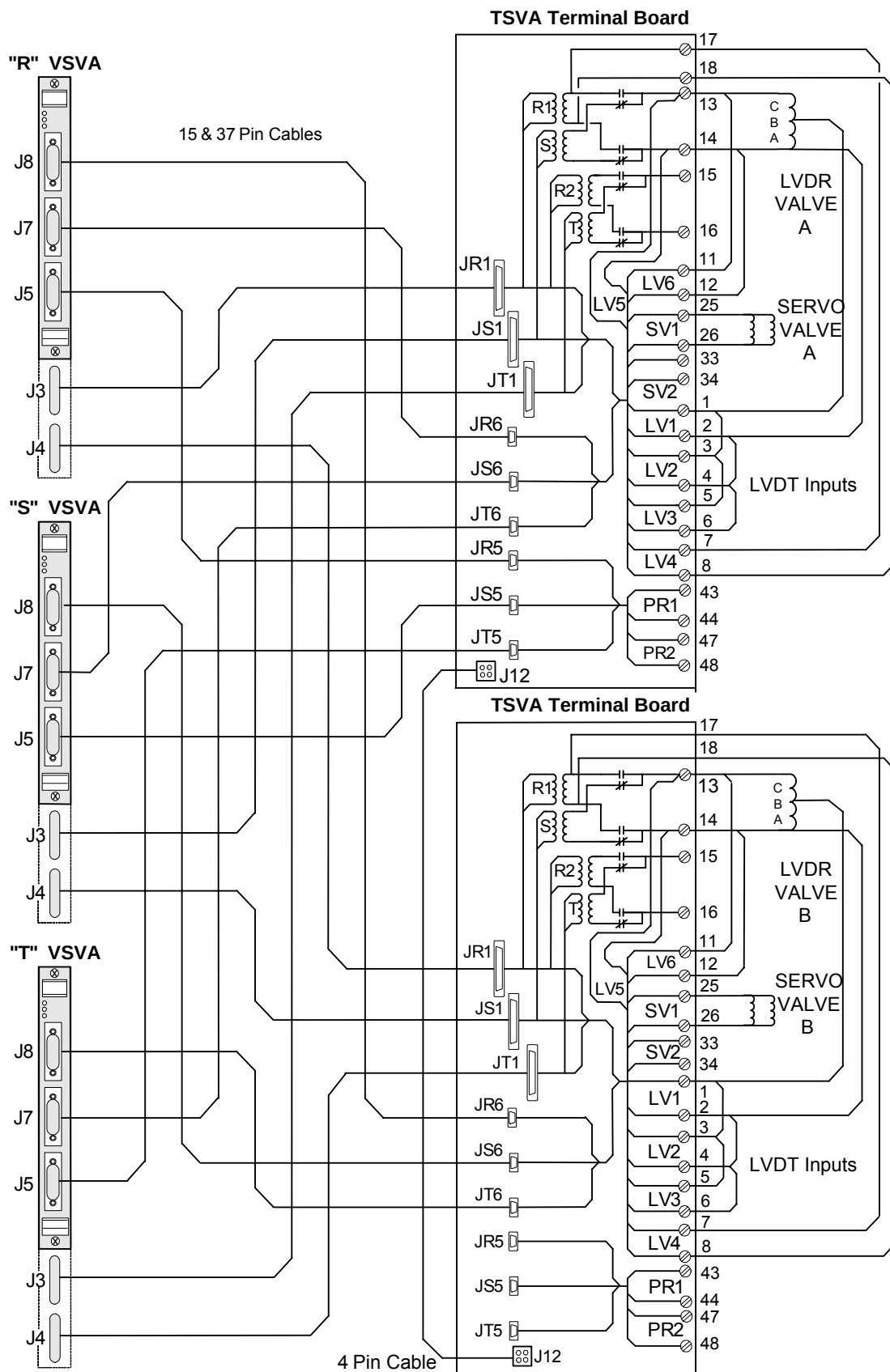
Three TMR VSVA boards, R, S, and T, connect to either one or two TSVA terminal boards using cables, with DC-37 pin connectors, between the TSVA JR1, JS1 and JT1 connectors and the R, S, or T VME rack backplane J3xx or J4xx connectors. JR6, JS6 and JT6 TSVA connectors feed total servo output combined current sense signals back to the associated VSVA front panel connectors, J7 and J8, using twisted/shielded pair cables with DA-15 pin connectors. The J7 and J3xx cables must connect to one of the TSVA boards, while J8 and J4xx must connect to a second TSVA board, if used. Pulse rate inputs are fanned into the three TMR VSVA boards using twisted/shielded pair cables, with DA-15 pin connectors, connected between the J5 connectors on the VSVA front panels and JR5, JS5, and JT5 connectors on the TSVA. When pulse rate inputs are used, the J5 cables must be connected to the TSVA board associated with the J3xx 37 pin backplane cable. If pulse rate inputs are not required, connecting the J5 cables is unnecessary. The 4-pin J12 connectors and cable connect the LVDT switchover relay status between two TSVA boards. If the J5 cable is not used, the J12 cable is not needed. Refer to the figure, *Application Example 1: Two Dual Coil Servo Valve with Tied Coils and One LVDT/LVDR per TSVA*.

Spare I/O resources are wired at the TSVA terminal block providing redundant monitoring functions improving VSVA board fault detection and localization. For example: LVDT inputs 1, 2, and 3 are wired together on the TSVA terminal block using three different LVDT/LVDR input cables and conditioning circuits on the VSVA and TSVA boards. Selecting a three-position, mid-select regulator configuration for regulator 1 and servo output 1 ensures a single fault in any of the three LVDT/LVDR input conditioning circuits or cables will not adversely affect the servo outputs. Mode 1 configuration enables limit checking on the VSVA board between the three LVDT regulator inputs while detecting and reporting disagreements between them. Mode 1 also enables limit checking between LVDT inputs 7, 8, and 9 assigned to servo regulator 3 and servo output 3. Refer to the *Configuration* section for more detailed information.

Mode 1 configuration checks the R1 excitation sources of both TSVA boards, enhancing fault detecting and reporting capability.

LVDT inputs 6 and 12 are wired at the TSVA terminal block redundantly monitoring LVDT excitation switchover outputs 1 and 3. Circuits on the VSVA boards use LVDT inputs 5 and 11 to detect loss-of-excitation, controlling the excitation 1 and 3 output switchover functions. LVDT inputs 5 and 11 are internally fed back on the TSVA to the VSVA boards. Refer to the *Configuration* section for more detailed information.

Mode 1 only checks the following defined functions: detecting LVDT/LVDR disagreements and generating diagnostic alarms/messages.



Application Example 1: Two Dual Coil Servo Valve with Tied Coils and One LVDT/LVDR per TSVA

Example 2: Four Dual Coil Servo Valves and Single LVDT/LVDR

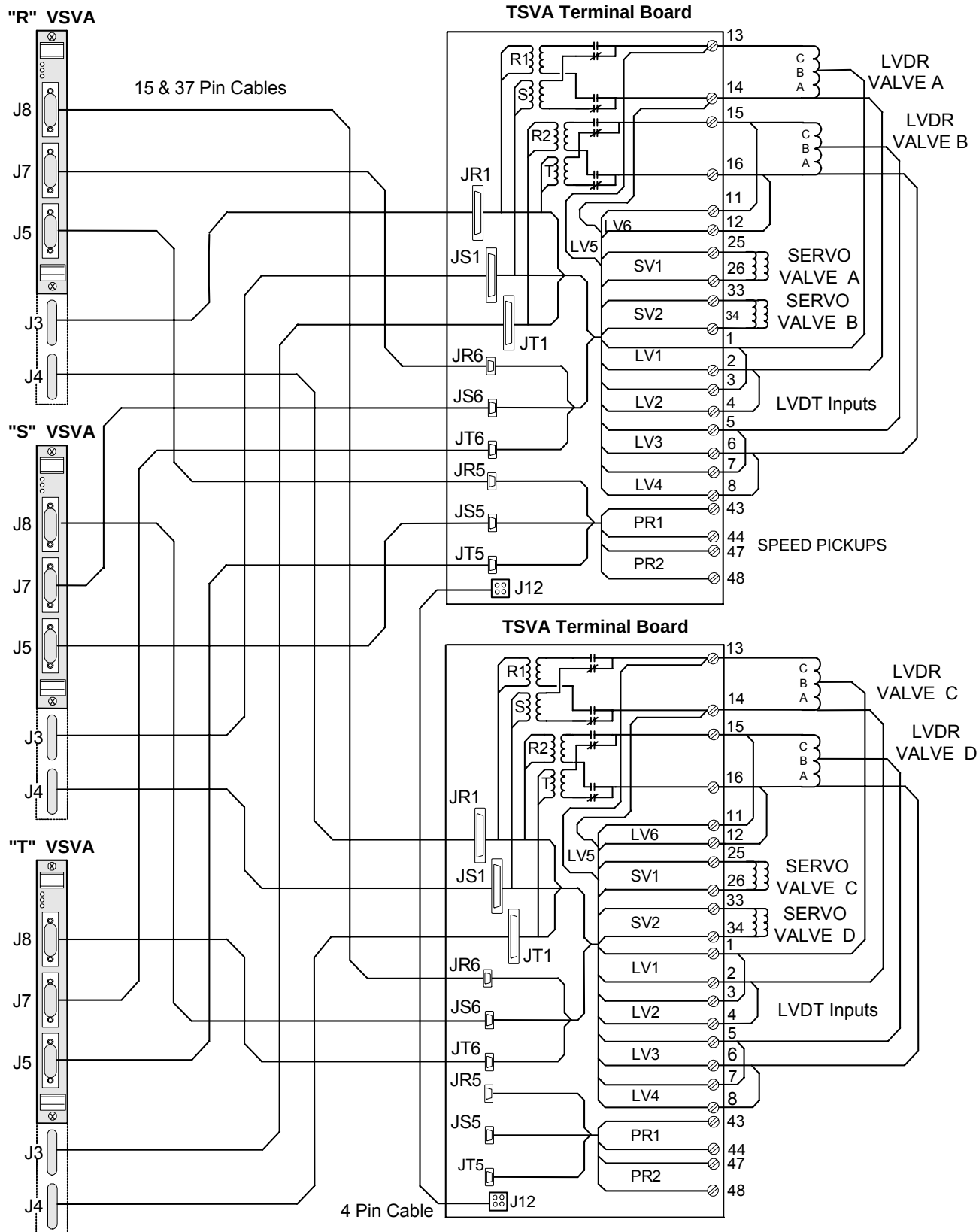
The second application example supports four dual coil servo valves with tied coils and a single LVDT/LVDR position feedback device per servo valve. Two servo valves and associated feedback devices are connected to each of the two TSVA boards. The three TMR VSVA boards plus two TSVA boards and associated cables shown in the following figure provide servo control outputs for up to four servo valve functions. The VSVA boards and internal cables can be replaced online without the loss of servo output functions. Online replacement of a TSVA board will result in the loss of up to two servo valve control functions during the replacement time period.

Spare I/O resources are wired at the TSVA terminal block providing redundant monitoring functions enhancing VSVA board fault detecting and localization. For example: LVDT inputs 1 and 2 are wired together on the TSVA terminal block utilizing two different LVDT/LVDR input cables and input conditioning circuits on the VSVA and TSVA boards. A two position, minimum or maximum, regulator configuration can be selected for regulators 1 - 4 and servo outputs 1 - 4 ensuring a single fault in either of two associated LVDT/LVDR input conditioning circuits will not affect the servo output functions. A mode 2 configuration should be selected enabling limit checking on the VSVA board between LVDT/LVDR regulator inputs 1 and 2, assigned to servo channel 1, detecting and reporting disagreements between them. Mode 2 enables limit checking between LVDT input pairs 3 - 4, 7 - 8, and 9 - 10 assigned to servo regulators and servo outputs 2 through 4. Refer to the *Configuration* section for more detailed information on mode 2 servo configuration and operation. Refer to the figure, *Application Example 2: Four Dual Coil Servo Valves with Tied Coils-One LVDT/LVDR per Valve*.

Mode 2 checks for LVDT/LVDR input pair disagreements for monitors 1 through 12 when configured to a 2_LVposMIN or 2_LVposMAX configuration and assigned to input pairs 1 - 2, 3 - 4, 7 - 8, and 9 - 10. Each of the input pairs must be assigned to one of the 12 monitoring functions when enabling mode 2.

Mode 2 only checks between LVDT/LVDR specified pairs on regulators and monitors detecting disagreements that generate diagnostic alarms and messages.

LVDT input 6 and 12 are wired at the TSVA terminal block to monitor and control LVDT excitation switchover outputs 2 and 4. Excitation switchover outputs 1 and 3 are monitored and controlled using LVDT/LVDR inputs 5 and 11. These are internally fed back to the TSVA detecting loss-of-excitation. Refer to the *Configuration* section for specifics on setting up and enabling LVDT excitation switchover circuit function.



Application Example 2: Four Dual Coil Servo Valves with Tied Coils -One LVDT/LVDR per Valve

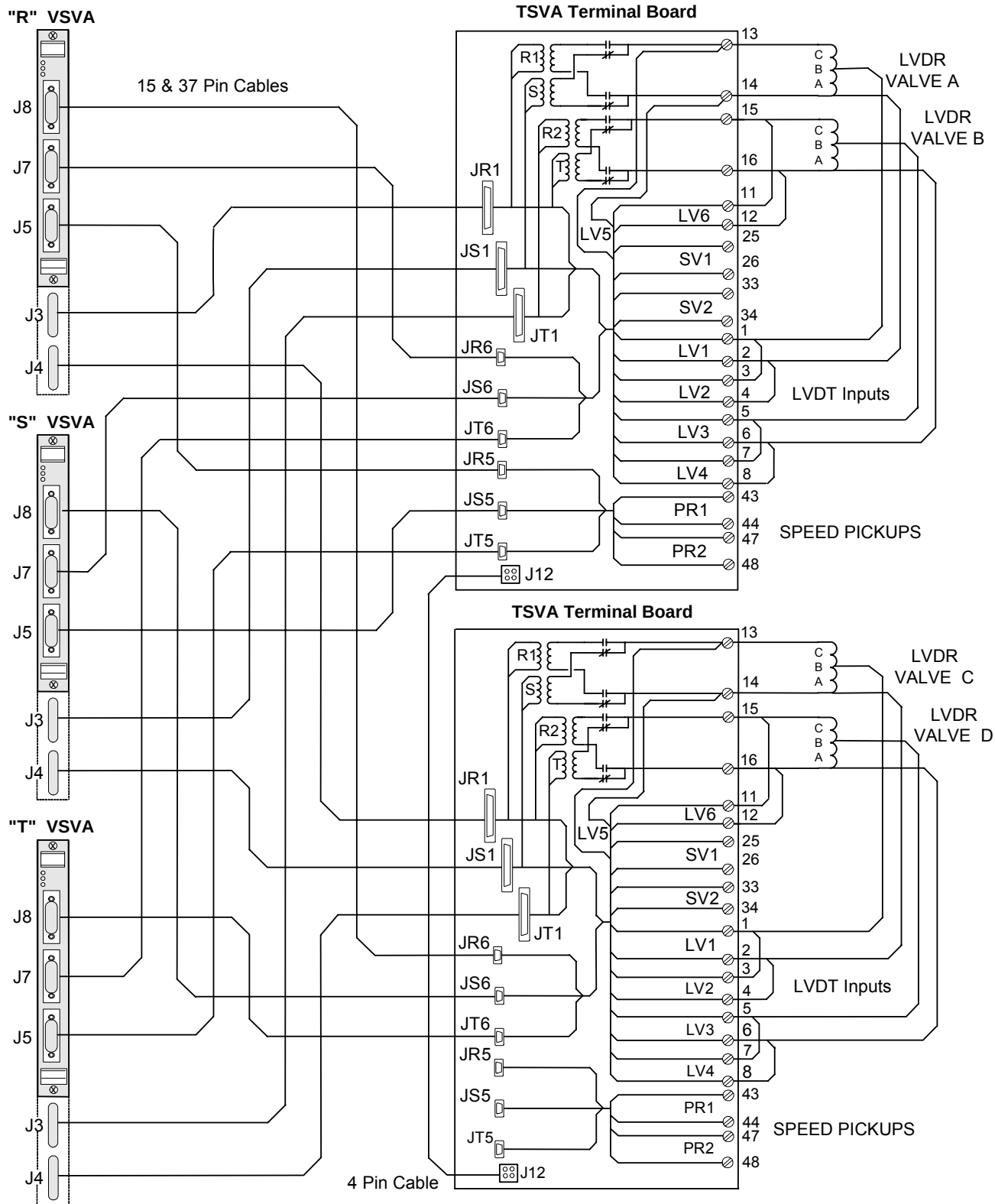
Example 3: Four LVDT/LVDR Valve Position Only Monitors

The third application example shows supports four LVDT/LVDR valve position only monitors. LVDT/LVDR position information from four remotely driven servo valves is monitored using this configuration. This configuration was developed to support NSTC monitoring valve positions on customer-controlled valves.

The three TMR VSVA boards plus two TSVA boards and associated cables shown in the following figure provide four LVDT/LVDR excitation sources and LVDT/LVDR input position monitoring functions supporting four customer-controlled valves. The VSVA boards and internal cables can be replaced online without losing LVDT/LVDR excitation/monitor functions. Online replacement of a TSVA board can result in the loss of two servo valve monitoring functions during the replacement time period.

LVDT/LVDR input pairs 1 - 2, 3 - 4, 7 - 8, and 9 - 10 are wired at the TSVA terminal block providing redundant monitoring, enhancing VSVA board fault detecting and localization. For example: LVDT inputs 1 and 2 are wired together on the TSVA terminal block utilizing two different LVDT/LVDR input cables and input conditioning circuits. A two position minimum or maximum monitor configuration can be selected for monitors 1 through 12 ensuring a single fault in either of the two LVDT/LVDR input conditioning circuits will not affect the related LVDT/LVDR monitoring function. A mode 2 configuration can be selected enabling limit checking on the VSVA board between the two LVDT/LVDR monitor inputs for detecting and reporting disagreements between LVDT input pairs 3 - 4, 7 - 8, and 9 - 10 assigned to one of the 12 monitors. Each of these input pairs must only be assigned to one of the 12 monitor functions when enabling mode 2. Refer to the *Configuration* section for more detailed information on mode 2 servo configuration and operation. Refer to the figure, *Application Example 3: Four LVDT/LVDR Value Position Monitors Only Configuration*.

LVDT inputs 6 and 12 are wired at the TSVA terminal block monitoring and controlling LVDT excitation switchover outputs 2 and 4. Excitation switchover outputs 1 and 3 are monitored and controlled based on LVDT/LVDR inputs 5 and 11. These are internally fed back to the TSVA board detecting loss-of-excitation. Refer to the *Configuration* section for more detailed information on setting up and enabling LVDT excitation switchover circuit function.



Application Example 3: Four LVDT/LVDR Valve Position Monitors Only Configuration

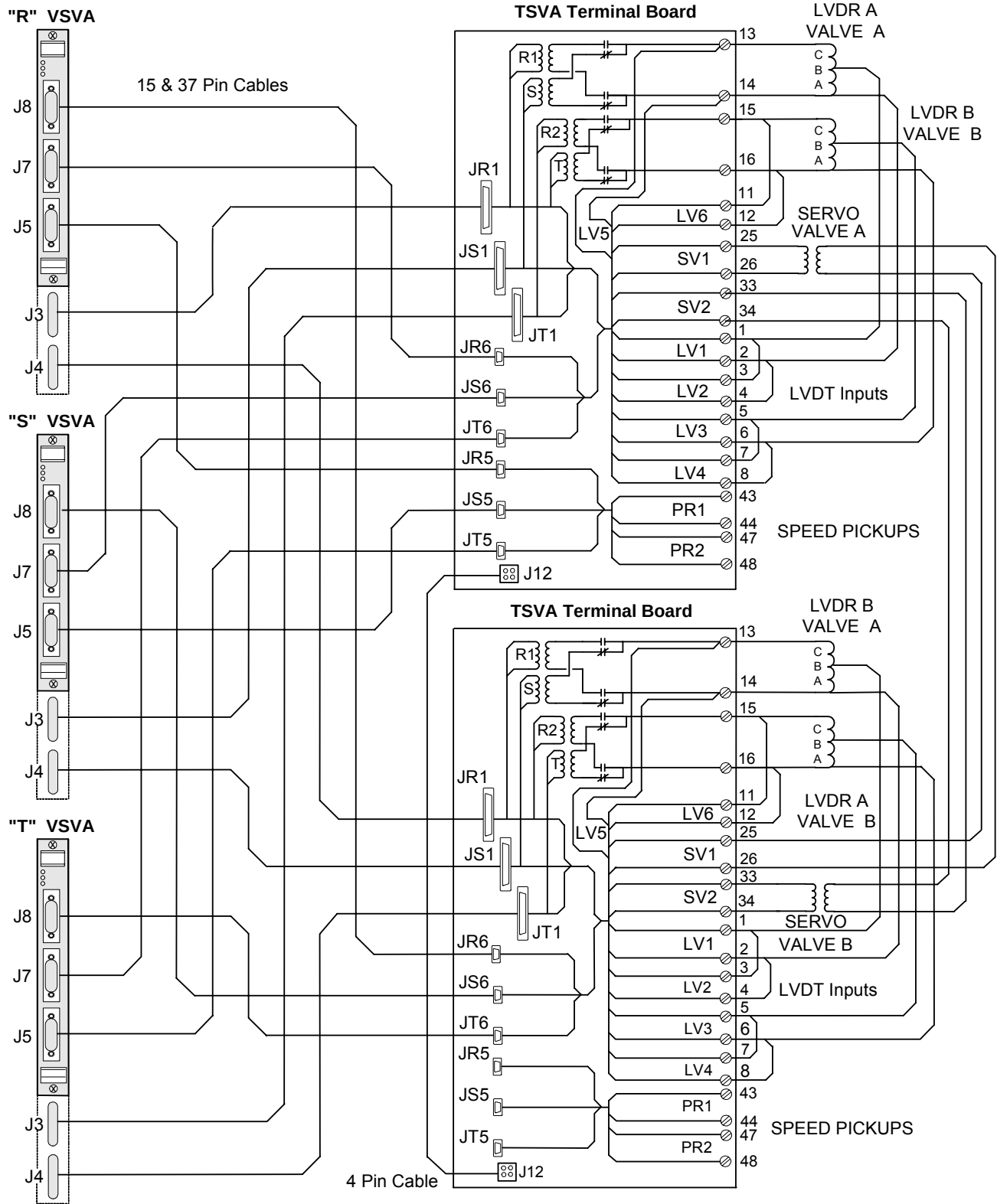
Example 4: Two Dual Coil Servo Valves and Two LVDT/LVDR Devices

The fourth application example supports two dual coil servo valves with split coils and two separate LVDT/LVDR devices per servo valve. The split coils of the two servo valves and the associated LVDT/LVDR devices are divided between the two TSVA boards as shown in the following figure. This supports changing VSVA boards, TSVA boards and cables while online without losing either of the two servo output functions.

Loss of one servo control output channel to one of the two split servo coils will result in a 50% reduction in gain and null bias.

Spare I/O resources are wired on the TSVA terminal block providing redundant monitoring functions while enhancing VSVA board fault detection and localization. For example: LVDT inputs 1 and 2 are wired together on the TSVA terminal block. They utilize two different LVDT/LVDR input cables and input conditioning circuits on the VSVA and TSVA boards while monitoring a single LVDT/LVDR input. A two position minimum or maximum monitor arrangement can be configured using monitor 1. LVDT/LVDR inputs 3 - 4, 7 - 8, and 9 - 10 can be configured using monitor 3, monitor 7, and monitor 9. A mode 2 configuration can be selected enabling a limit check on the VSVA board between these pairs of LVDT/LVDR monitor inputs detecting and reporting disagreements between them. Refer to the *Configuration* section for more detailed information on Mode 2 monitor configuration and operation. Refer to the figure, *Application Example 4: Two Dual Coil Valves with Split Coils - Two LVDT/LVDRs per Valve*.

LVDT input 6 and 12 are wired at the TSVA terminal block to monitor and control LVDT excitation switchover outputs 2 and 4. Excitation switchover outputs 1 and 3 are monitored and controlled based on LVDT/LVDR inputs 5 and 11. These are internally fed back on the TSVA to detect loss-of-excitation. Refer to the *Configuration* section for specifics on setting up and enabling LVDT excitation switchover circuit functions.

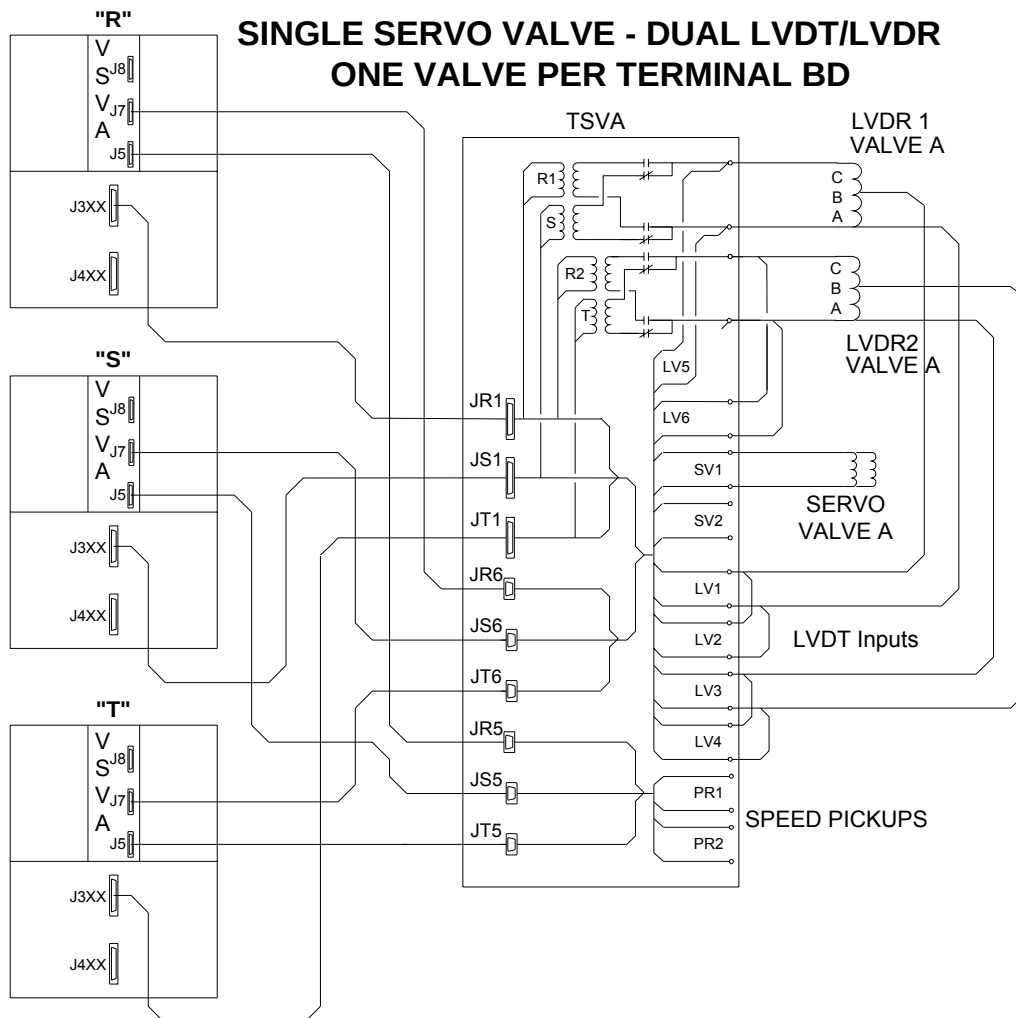


Application Example 4: Two Dual Coil Valves with Split Coils – Two LVDT/LVDRs per Valve

Example 5: Single Servo Valve - Dual LVDT/LVDR One Value Per Terminal Board

The fifth application example supports a single-coil servo valve with two separate LVDT/LVDR devices per servo valve. The single-coil servo valve and the associated LVDT/LVDR devices are supported by a single TSVA terminal board as shown in the following figure.

Spare I/O resources are wired on the TSVA terminal block providing redundant monitoring functions while enhancing the VSVA board fault detection and localization. For example: LVDT inputs 1 and 2 are wired together on the TSVA terminal block. They utilize two different LVDT/LVDR input cables and input conditioning circuits on the VSVA and TSVA boards while monitoring a single LVDT/LVDR input. A two position minimum or maximum monitor arrangement can be configured using monitor 1. LVDT/LVDR inputs 3-4, 7-8 and 9-10 can be configured using monitor 3, monitor 7 and monitor 9. A mode 2 configuration can be selected enabling a limit check on the VSVA board between these pairs of LVDT/LVDR monitor inputs detecting and reporting disagreements between them. Refer to the Configuration section for more detailed information on Mode 2 monitor configuration and operation.



Application Example 5: Single Servo Valve - Dual LVDT/LVDR

Typical Servo Coil Ratings

Coil Type	Nominal Current	Nominal Coil Resistance (Ω /Coil)	Typical Servo Design	Rated Current for Rated Flow	Internal TSVA Resistance (Ω)	J1 – J10 TSVA Jumper Setting
1	± 10 mA	1,000	2 and 3 Coil Gas	10 mA	102	10 mA
2	± 20 mA	250	25 GPM, 3 and 4 Way, 2 Coil	16 mA	416	20 mA
3	± 20 mA	500	70 GPM, 3 Way, 2 Coil	17 mA	416	10 mA
4	± 40 mA	125	50 GPM, 4 Way, 2 Coil	34.5 mA	185	40 mA

The above table defines standard servo coil resistance and associated internal resistance, selectable with the terminal board jumpers shown in the preceding figure. In addition, non-standard jumper settings could be used to drive non-standard coils. The total resistance would be equivalent to the standard setting.

Control valve position is sensed with either a four wire LVDT or a three-wire linear variable differential reluctance (LVDR). The application software allows maximum flexibility checks for the feedback devices. LVDT/LVDRs can be mounted up to 300 m (984 ft) from the turbine control with a maximum two-way cable resistance of 15 Ω .

Note The excitation source is isolated from signal common (floating) and is capable of operation at common mode voltages up to 35 V dc, or 35 V rms, 50/60 Hz

Two LVDT/LVDR excitation sources are located on each terminal board for Simplex applications and another two for TMR applications. Excitation voltage is 7 V rms and the frequency is 3.2 kHz with a total harmonic distortion of less than 1% when loaded.

A typical LVDT/LVDR has an output of 0.7 V rms at the zero stroke position of the valve stem, and an output of 3.5 V rms at the designed maximum stroke position (some applications have these reversed). The LVDT/LVDR input is converted to dc and conditioned with a low pass filter. Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check.

Two pulse rate inputs are cabled to a single J5 connector on the VSVA board front. This is a dedicated connection minimizing noise sensitivity on the pulse rate inputs.

Inputs support both passive magnetic pickups and active pulse rate transducers (TTL type). Both are interchangeable without configuration. Pulse rate inputs can be located up to 300 m (984 ft) from the turbine control cabinet, provided 70 NF shielded-pair cable is used or 35 NF differential capacitance with 15 Ω resistance.

A frequency range of 2 to 12 kHz can be monitored at a normal sampling rate of either 10 or 20 ms. Magnetic pickups typically have an output resistance of 200 Ω and an inductance of 85 mHz excluding cable characteristics. The transducer is a high impedance source, generating energy levels insufficient to cause a spark.

Note The maximum short circuit current is approximately 100 mA with a maximum power output of 1 W.

Specifications

Item	Specification
Number of inputs (per TSVA)	LVDT 1-4 and 6. Five LVDT windings Two pulse rate signals (total of two per VSVA)
Number of outputs (per TSVA)	Two servo valves (total of four per VSVA board) Four excitation sources for LVDTs Two special TMR switchover LVDT/LVDR excitation sources Two excitation sources (24 V dc) for pulse rate transducers
Internal sample rate	200 Hz
Pulse Rate Excitation Source (TSVA)	Nominal 24 V dc --- 40 mA max
LVDT accuracy	1% with 14-bit resolution
LVDT input filter	Low pass filter with three down breaks at 50 rad/sec $\pm 15\%$
LVDT common mode rejection	CMR is 1 V, 60 dB at 50/60 Hz
LVDT excitation output	Frequency of 3.2 ± 0.2 kHz Voltage of 7.00 ± 0.14 V rms
Pulse rate accuracy	0.05% of reading with 16-bit resolution at 50 Hz frame rate Noise of acceleration measurement is less than ± 50 Hz/sec for a 10,000 Hz signal being read at 10 ms
Pulse rate input	Minimum signal for proper measurement at 4 Hz is 33 mVpk, and at 12 kHz is 827 mVpk.
Magnetic PR pickup signal input	Generates 150 V peak-to-peak into 60 k Ω
Active PR Pickup Signal input	Generates 5 to 27 V peak-to-peak into 60 k Ω
Servo valve output accuracy	2% with 12-bit resolution Dither amplitude and frequency adjustable; unused, 12.5 Hz, 25 Hz, 33.33 Hz, 50 Hz, 100 Hz; 0 to 10% Amplitude
Fault detecting	Suicide servo outputs initiated by: Servo current out of limits Regulator feedback signal out of limits

Diagnostics

Three LEDs at the top of the VSVA front panel display status information. The normal RUN condition is a flashing green, and FAIL is solid red. The third LED is normally off but displays a steady orange if an alarm condition exists on the board

Servo diagnostics cover items such as out of range LVDT voltage, servo suicide, servo current open circuit, and short circuit. If any one of the signals goes unhealthy a composite diagnostic alarm, L#DIAG_VSVA occurs. If the associated regulator has two sensors, the bad sensor is removed from the feedback calculation and the good sensor is used. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and reset with the RESET_DIA signal if they go healthy

Connectors JR1, JS1, JT1, JR6, JS6, JT6, JR5, JS5 and JT5 on the TSVA terminal board have their own ID device that is interrogated by the VSVA board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

Configuration

Jumpers on the TSVA must be configured to select appropriate in-line resistors that limit Servo output current overdrive. Jumpers JP1 to JP5 and JP6 to JP10 select resistor values that are compatible with full-scale servo output currents of 10 mA, 20mA, 40 mA, 80 mA or 120 mA for servo output channels 1 and 2 respectively.

Parameter	Description	Choices
Configuration		
System Limits	Enable / Disable system limits for Pulse Rate Inputs.	Enable, disable
Mode	Modes 1 and 2 for specific VSVA board applications. Mode 1: Mode1 generates diagnostic alarms for applications using one servo valve with dual coils tied in parallel and a single LVDT for position feedback. Only one servo valve and associated LVDT is supported per TSVA terminal board. If Regulator 1 and 3 is used, RegType must be selected to 3_LV_PosMid using LVDT inputs 1, 2 and 3 and 7,8 and 9 respectively. Regulators 2 and 4 must be selected to RegType unused. A diagnostic alarm is generated when an LVDT input assigned to Regulator 1 or 3 exceeds the TMR_DiffLimt referenced to the voted median value. If Monitors 4 and 10 are used, they must be assigned to LVDT inputs 4 and 10 respectively. A diagnostic alarm will be generated if LVDT input 4 or 10 is < 6.6 Vrms or > 7.7 Vrms. Excitation sources J3 ER1 and J4 ER1 must be wired to LVDT Inputs 4 and 10 respectively if Monitors 4 and 10 are used. Mode 2: Mode2 generates diagnostic alarms for applications using one or two servo valves with dual split coils and one or two LVDTs each for position feedback. These applications will typically split the servo valves and LVDTs between the two TSVA terminal boards. Mode2 also supports four-valve LVDT position monitoring only applications. If Regulators 1,2,3 or 4 are used, they must be selected to RegType 2_LV_PosMax or Min using LVDT input pairs (1,2) (3,4) (7,8) (9,10) respectively. If Monitors 1-12 are used and assigned to any of LVDT input pairs (1,2) (3,4) (7,8) or (9,10), they must be selected to RegType 2_LV_PosMax or Min. Only one Monitor can be assigned to one of these pairs. If a Regulator or Monitor is assigned LVDT input pairs (1,2) (3,4) (7,8) or (9,10) and the difference within the pair exceeds the associated TMR_DiffLimt value, a diagnostic alarm will be generated.	Unused, Mode1, Mode 2
SrvOcSiucHld	If an over-current condition exists on a used Servo Output 1,2,3 or 4 and it exceeds the selected Curr_Suicide value, the suicide command will be held off for this time interval to prevent suicide action on a short transient over-current condition.	Unused, 10 ms, 15 ms, 20 ms, 25 ms, 30 ms, 35 ms, 40 ms, 45 ms, 50 ms
LvdtExFIHold	Hold-off time to allow LVDT input hardware filter recovery when LVDT Excitation source switch over occurs. The LVDT input retains last known good value for the time selected.	Unused, 5 ms, 10 ms, 15 ms, 20 ms, 25 ms, 30 ms, 35 ms, 40 ms

Parameter	Description	Choices
Regulators		
Regulator 1		
RegType	Algorithm used in the regulator	Unused, no_fbk, 1_PulseRate, 2_PlsRateMAX, 1_LVPosition, 2_LV_PosMIN, 2_LV_PosMAX, 3_LV_PosMid, 2_LV_pilotCyl, 4_LVp/cylMAX
RegGain	Position loop gain in (%current/%position)	Gain –200 to 200
RegNullBias	Null bias in % current, balances servo spring force	Null Bias –100 to 100
DitherAmpl	Dither in % current (minimizes hysteresis)	Dither amp: 0 to 10%
Dither Frequency	Dither Frequency in Hz	Dither Frequency: unused, 12.5Hz, 25Hz, 33.33Hz, 50Hz, 100Hz
MinPOSvalue	Position at Min End Stop in engineering units	Range: -15 to150
MAxPOSvalue	Position at Max End Stop in engineering units	Range: -15 to150
LVDT#input	LVDT Input Selection	Unused; LVDT 1 through 12
MnLVDT#_Vrms	LVDT# Vrms at Min End Stop – Normally set by Auto-Calibrate	Range: 0 to10
MxLVDT#_Vrms	LVDT# Vrms at Max End Stop – Normally set by Auto-Calibrate	Range: 0 to10
LVDT_Margin	Allowable Range Exceeded Error of LVDT in Percent	Range: 0 to7.1
TMR_DiffLimit	Diagnostic, Limit TMR Input Vote Difference, Position in Engineering Units	Range: -15 to150
Monitor 1		
Monitor type	Monitor algorithm	Unused 1_Lvposition, 2_LVposMIN, 2_LVposMAX, 3_LVposMID
MinPOSvalue	Position at Min End Stop in engineering units	Range: -15 to150
MAxPOSvalue	Position at Max End Stop in engineering units	Range: -15 to150
LVDT#input	LVDT Input Selection	Unused; LVDT 1 through 12
MnLVDT#_Vrms	LVDT# Vrms at Min End Stop – Normally set by Auto-Calibrate	Range: 0 to10
MxLVDT#_Vrms	LVDT# Vrms at Max End Stop – Normally set by Auto-Calibrate	Range: 0to10
LVDT_Margin	Allowable Range Exceeded Error of LVDT in Percent	Range: 0 to7.1
TMR_DiffLimit	Diagnostic, Limit TMR Input Vote Difference, Position in Engineering Units	Range: -15 to150

Parameter	Description	Choices
Monitor 2		
Monitor 12		
J3:IS200TSVAH1A	Terminal board 1 connected to VSVA through J3	J3 connected, not connected
ExctFailOvr1	Excitation 1 Failover Status: indicates whether excitation source "R1" or Excitation source "S" is selected. (R1=0; S=1)	(Input BIT)
ExciteMode	If both LVDT Excitation Failover Outputs 1 and 2 are required, independent should be selected. If only LVDT Excitation Failover Output 1 is required, "redundant" should be selected and LVDT Input 6 must be wired to LVDT Excitation Failover Output 1. This provides redundant monitoring of LVDT Input 5 failover detecting circuits. Switch_R2T must be set to "Disable".	Independent, Redundant
Switch_R1S	Disable or Enable Excitation 1 Failover.	Disable, Enable
RndtLvdtDiag	Enable - Configures LVDT 6 Input as a redundant monitor of excitation Source Select 1 switchover logic. Produces a Diagnostic if disagreement occurs.	Disable, Enable
ExctFailOvr2	Excitation 2 Failover Status: indicates whether excitation source "R2" or Excitation source "T" is selected. (R2=0; T=1)	(Input BIT)
Switch_R2T	Disable or Enable Excitation 2 Failover. Set to Disable if ExciteMode is set to Redundant.	Disable, Enable
Servo Output1	Measured Servo Output 1 Current Total in Percent	(Input FLOAT)
Reg Number	Identify regulator number	Unused, Reg1, Reg2, Reg3, Reg4
Servo_mA_Out	Select current output for coil windings	10, 20, 40, 80, 120 mA
EnableCurSuic	Select Suicide function based on current	Enable, disable
Curr_Suicide	Percent current error to initiate suicide	75 to 125% (output current error)
EnablFbkSuic	Select Suicide function based on feedback	Enable, disable
Fdbk_Suicide	Percent position error to initiate suicide	0 to 10% (actuator position error)
Servo Output2	Measured Servo Output 2 Current Total in Percent	(input FLOAT)
J4:IS200TSVAH1A	Terminal Board 2 connected to VSVA through J4	J4 connected, not connected
ExctFailOvr1	Excitation 3 Failover Status: indicates whether excitation source "R1" or Excitation source "S" is selected. (R1=0; S=1)	(Input BIT)
ExciteMode	If both LVDT Excitation Failover Outputs 3 and 4 are required, independent should be selected. If only LVDT Excitation Failover Output 3 is required, "redundant" should be selected and LVDT Input 12 must be wired to LVDT Excitation Failover Output 3. This provides redundant monitoring of the LVDT Input 11 failover detecting circuits. Switch_R2T must be set to "Disable".	Independent, Redundant
Switch_R1S	Disable or Enable Excitation 3 Failover.	Disable, Enable
RndtLvdtDiag	Enable - Configures LVDT 12 Input as a redundant monitor of excitation Source Select 3 switchover logic. Produces a Diagnostic if disagreement occurs.	Disable, Enable
ExctFailOvr2	Excitation 4 Failover Status: indicates whether excitation source "R2" or Excitation source "T" is selected. (R2=0; T=1)	(Input BIT)
Switch_R2T	Disable or Enable Excitation 4 Failover. Set to Disable if ExciteMode is set to Redundant.	Disable, Enable

Parameter	Description	Choices	
Servo Output3	Measured Servo Output 3 Current Total in Percent	(Input FLOAT)	
Servo Output4	Measured Servo Output 4 Current Total in Percent	(Input FLOAT)	
J5:IS200TSAH1A	Pulse Rate inputs cabled to J5 connector Note: If used, the J5 cable must be attached to the J3 TSAV terminal board.	Connected, not connected	
FlowRate1	Pulse rate input selected - Board point	(Input FLOAT)	
PRTtype	Select speed or flow type signal	Unused, speed, or flow	
PRScale	Convert Hz to engineering units	0 to 1,000	
SysLim1Enabl	Select system limit	Enable, disable	
SysLim1Latch	Select whether alarm will latch	Latch, not latch	
SysLim1Type	Select type of alarm initiation	>= Or <=	
SysLimit	Select alarm level in GPM or RPM	0 to 12,000	
SystemLim2	Same as above	Same as above	
TMR_DiffLimt	Difference limit off voted pulse inputs (EU)	0 to 12,000	
FlowRate2	Pulse rate input selected - Board point (as above)	(Input FLOAT)	
Board Points (Signals)	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VSVA	Board diagnostic exists	Input	BIT
R1_SuicideNV	Servo 1 Output Suicide Status	Input	BIT
:	:	Input	BIT
R4_SuicideNV	Servo 4 Output Suicide Status	Input	BIT
ER1_StateNV	Excitation 1 Select Relay State	Input	BIT
:	:	Input	BIT
ER4_StateNV	Excitation 4 Select Relay State	Input	BIT
SysLim1PR1	Pulse Rate 1 Limit 1 Status	Input	BIT
SysLim2PR1	Pulse Rate 1 Limit 2 Status	Input	BIT
SysLim1PR2	Pulse Rate 2 Limit 1 Status	Input	BIT
SysLim2PR2	Pulse Rate 2 Limit 2 Status	Input	BIT
Reg1Suicide	Regulator 1 suicide relay status	Input	BIT
:	:	Input	BIT
Reg4Suicide	Regulator 4 suicide relay status	Input	BIT
RegCalMode	Regulator Calibration Status	Input	BIT
Reg1_Fdbk	Regulator 1 Feedback Value	Input	FLOAT
:	:	Input	FLOAT
Reg4_Fdbk	Regulator 4 Feedback Value	Input	FLOAT
MiscFdbk1a	Pilot/Cylinder 1	Input	FLOAT
:	:	Input	FLOAT
MiscFdbk4a	Pilot/Cylinder 4	Input	FLOAT
Reg1_Error	Regulator 1 Position Error	Input	FLOAT
:	:	Input	FLOAT
Reg4_Error	Regulator 4 Position Error	Input	FLOAT
Accel1	GPM/sec	Input	FLOAT
Accel2	GPM/sec	Input	FLOAT
Mon1	Position monitor	Input	FLOAT
:	:	Input	FLOAT
Mon12	Position monitor	Input	FLOAT
AVSelect1NV	Anti-vote Signal Monitor – One of Five Selected Signals. (Local Current, Total Current, Compliance Voltage, DAC Feedback or Position Error)	Input	FLOAT
:	:	Input	FLOAT

Parameter	Description	Choices	
AVSelect4NV	Anti-vote Signal Monitor – One of Five Selected Signals. (Local Current, Total Current, Compliance Voltage, DAC Feedback or Position Error)	Input	FLOAT
CalibEnab1	Enable Calibration for Regulator 1	Output	BIT
:	:	Output	BIT
CalibEnab4	Enable Calibration for Regulator 4	Output	BIT
SuicideForce1	Force Suicide for Servo Output 1	Output	BIT
:	:	Output	BIT
SuicideForce4	Force Suicide for Servo Output 4	Output	BIT
Reg1_Ref	Regulator 1 Position Reference	Output	FLOAT
:	:	Output	FLOAT
Reg4_Ref	Regulator 1 Position Reference	Output	FLOAT
Reg1- GainMod	Regulator 1 Gain Modifier	Output	FLOAT
:	:	Output	FLOAT
Reg4- GainMod	Regulator 4 Gain Modifier	Output	FLOAT
Reg1_NullCor	Reg 1 Null Bias Correction	Output	FLOAT
:	:	Output	FLOAT
Reg4_NullCor	Reg 4 Null Bias Correction	Output	FLOAT
Internal Variables	Internal variables to service the auto-calibration display, not configurable		

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (VSVA board is not allowed to go online unless override is active)
3	CRC failure override is Active	Board firmware programming error (VSVA board is allowed to go online – should not happen on released code)
16	System Limit Checking is Disabled Limit checks for J5 Pulse Rate Inputs disabled. This diagnostic is disabled if the J5 cable is not present at power-up.	System checking was disabled by configuration.
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to the VSVA board.
30	ConfigCompatCode Mismatch; Firmware: {Firmware: #} (Tre: #) The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on VSVA board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode Mismatch; Firmware: {Firmware: #} (Tre: #) The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the VSVA board. Either the tre file or firmware must change. Contact the factory.
33-44	Monitor LVDT #{1-12} rms voltage out of limits {value} Monitor LVDT # rms voltage is out of limits. The Limits are defined as: Monitor MnLVDT#_Vrms – ((MxLVDT#_Vrms - MnLVDT#_Vrms) * LVDT_MArgin percent /100) = Low Limit Monitor MnLVDT#_Vrms + ((MxLVDT#_Vrms - MnLVDT#_Vrms) * LVDT_MArgin percent /100) = High Limit	Minimum and maximum LVDT rms voltage limits are configured incorrectly. The LVDT may need recalibration. May be a problem on the VSVA board.

Fault	Fault Description	Possible Cause
45	Calibration Mode Enabled A VSVA Servo Regulator was placed into calibration mode.	The VSVA is in calibration mode.
46	VSVA board not online, Servos Suicided The servo is suicided because the VSVA is not online.	The controller (R, S, T) or IONet is down, or there is a configuration problem with the system preventing the VCMI from bringing the VSVA board online.
48-51	Servo current #{1-4} Over current Detected {value} Local Servo # Current exceeded 80% for a continuous time period >80 milliseconds.	Bad Regulator Position reference or position feedback value. May be a problem on the VSVA board.
52-55	Servo current #{1-4} Current Exceeded Limit {value}, Suicided. Produces a diagnostic alarm and suicides the Servo # Output when the following four conditions are met: Servo local current exceeds the Curr_Suicide Limit in percent. The time hold off requirement of SrvOcSiuchld {value} is met Local Current polarities for R, S and T Servo Outputs support isolation of a single VSVA board/servo output to suicide. Configuring the EnableCurSuic to disable will disable the suicide action.	Bad Regulator Position reference or position feedback value. May be a problem on the VSVA board.
56-59	Servo posit. #{1-4} fdbk out of range {value}, Suicided Servo position feedback is out of limits resulting in a Suicide. The Limits are defined as: Regulator # MinPOSvalue - Servo # Fdbk_Suicide value = low limit Regulator # MaxPOSvalue + Servo # Fdbk_Suicide value = high limit. Configuring the EnableFbkSuic to disable will disable the suicide action.	Minimum and maximum LVDT rms voltage limits are configured incorrectly. The LVDT may need recalibration. May be a problem on the VSVA board.
60	ConfigMsg error for regulator #{1-4} Configuration Message Error for Regulator Number #. There is a problem with the VSVA configuration and the servo will not operate properly.	The LVDT minimum and maximum voltages are equal or reversed, or an invalid LVDT, regulator, or servo number is specified.
61	On board ref voltages {Pos ref} {Neg ref} Onboard Calibration Voltage Range Fault for Positive 9.09 V dc and/or Negative 9.09 V dc References. Message displays the values for the P9.09 and N9.09 reference voltage readings.	Problem on the VSVA board.
62	VSVA LVDT Exct Out Mon to J3 {ER1, ES, ET} voltage out of range {value} LVDT Excitation Voltage out of range. (<6.3Vrms or >7.7Vrms)	May be a problem on the VSVA board.
63	VSVA LVDT Exct Out Mon to J4 {ER1, ES, ET} voltage out of range {value} LVDT Excitation Voltage out of range. (<6.3Vrms or >7.7Vrms)	May be a problem on the VSVA board.
64	VSVA LVDT Exct Out Mon to J3 {ER2, ES2 unused, ET2 unused} voltage out of range {value} LVDT Excitation Voltage out of range. (<6.3Vrms or >7.7Vrms)	May be a problem on the VSVA board.
65	VSVA LVDT Exct Out Mon to J4 {ER2, ES2 unused, ET2 unused} voltage out of range {value} LVDT Excitation Voltage out of range. (<6.3Vrms or >7.7Vrms)	May be a problem on the VSVA board.

Fault	Fault Description	Possible Cause
66	Servo Output Assignment Mismatch Servo output assignment mismatch. Regulator types 8 and 9 (pilot cylinder configurations) use two-servo outputs each. They have to be consecutive pairs, and they have to be configured as the same range	Fix the regulator configurations.
67-68	J3 Excitation failure #{1-2} Excitation Switchover An excitation switchover has occurred due to loss of LVDT Excitation output for {1} J3 Exc R1/S or {2} J3 Exc R2/T.	The Power Supply for the R, S or T rack may have been turned off. (R or S for #1, R or T for #2).
69-70	J4 Excitation failure #{3-4} Excitation Switchover An excitation switchover has occurred due to loss of LVDT Excitation output for {3} J4 Exc R1/S or {4} J4 Exc R2/T.	The Power Supply for the specified R or T rack may have been turned off. R and S for #3, R and T for #4.
71	J3 {R, S, T}_Pack DIO Communication Failure on {R, S} channels 1+2 Both J3 Serial Communication channels 1 and 2 for the specified R or S channel are not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The Power Supply for the specified R or S rack may be off.. The specified R or S VSVA board may have a problem sending or receiving serial communications The 37 pin J3 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector
72-73	J3 {R, S, T}_Pack DIO Communication Failure on {R, S} channel #{1 or 2} One of the J3 Serial Communication channels 1 or 2 for the specified R or S channel is not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified R or S VSVA board may have a problem. The 37 pin J3 cable associated with the specified R or S VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector or may have a shorted / open wire or pin.
74	J3 {R, S, T}_Pack DIO Communication Failure on {S, T} channels 1+2 Both J3 Serial Communication channels 1 and 2 for the specified S or T channel are not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The terminal board may have a signal net open or shorted to another signal. The Power Supply for the specified S or T rack may be off. The specified S or T VSVA board may have a problem sending or receiving serial communications The 37 pin J3 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector
75-76	J3 {R, S, T}_Pack DIO Communication Failure on {S, T} channel #{1 or 2} One of the J3 Serial Communication channels 1 or 2 for the specified S or T channel is not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified R or S VSVA board may have a problem. The 37 pin J3 cable associated with the specified R or S VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector or may have a shorted / open wire or pin.
77	J3 {R, S, T}_Pack DIO Communication Failure on {R, S, T} channels 1+2 Both J3 Serial Communication channels 1 and 2 for the specified R or S or T channel are not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The terminal board may have a signal net open or shorted to another signal. The Power Supply for the specified R, S or T rack may be off. The specified R, S or T VSVA board may have a problem sending or receiving serial communications The 37 pin J3 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector

Fault	Fault Description	Possible Cause
78-79	J3 {R, S, T}_Pack DIO Communication Failure on {R, S, T} channel #{1 or 2} One of the J3 Serial Communication channels 1 or 2 for the specified R or S or T channel is not communicating. J3 R or J3 S or J3 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified R, S or T VSVA board may have a problem. The 37 pin J3 cable associated with the specified R, S or T VSVA may not be properly mated at the TSVA terminal board, the rack backplane connector or may have a shorted / open wire or pin. The terminal board may have a signal net open or shorted to another signal.
80	J4 {R, S, T}_Pack DIO Communication Failure on {R, S} channels 1+2 Both J4 Serial Communication channels 1 and 2 for the specified R or S channel are not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The Power Supply for the specified R or S rack may be off. The specified R or S VSVA board may have a problem sending or receiving serial communications The 37 pin J4 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector
81-82	J4 {R, S, T}_Pack DIO Communication Failure on {R, S} channel #{1 or 2} One of the J4 Serial Communication channels 1 or 2 for the specified R or S channel is not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified R or S VSVA board may have a problem. The 37 pin J4 cable associated with the specified R or S VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector or may have a shorted / open wire or pin. The terminal board may have a signal net open or shorted to another signal.
83	J4 {R, S, T}_Pack DIO Communication Failure on {S, T} channels 1+2 Both J4 Serial Communication channels 1 and 2 for the specified S or T channel are not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The Power Supply for the specified S or T rack may be off. The specified S or T VSVA board may have a problem sending or receiving serial communications The 37 pin J4 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector
84-85	J4 {R, S, T}_Pack DIO Communication Failure on {S, T} channel #{1 or 2} One of the J4 Serial Communication channels 1 or 2 for the specified S or T channel is not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified S or T VSVA board may have a problem. The 37 pin J4 cable associated with the specified S or T VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector or may have a shorted / open wire or pin. The terminal board may have a signal net open or shorted to another signal.
86	J4 {R, S, T}_Pack DIO Communication Failure on {R, S, T} channels 1+2 Both J4 Serial Communication channels 1 and 2 for the specified R or S or T channel are not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The Power Supply for the specified R, S or T rack may be off. The specified R, S or T VSVA board may have a problem sending or receiving serial communications The 37 pin J4 cable associated with the specified VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector
87-88	J4 {R, S, T}_Pack DIO Communication Failure on {R, S, T} channel #{1 or 2} One of the J4 Serial Communication channels 1 or 2 for the specified R or S or T channel is not communicating. J4 R or J4 S or J4 T clarifies which VSVA board saw the fault and generated this diagnostic alarm.	The specified R, S or T VSVA board may have a problem. The 37 pin J4 cable associated with the specified R, S or T VSVA may not be properly mated at the TSVA terminal board or the rack backplane connector or may have a shorted / open wire or pin. The terminal board may have a signal net open or shorted to another signal.
97-100	Suicide relay #{1-4} does not match commanded state Suicide relay status contact feedback does not match the relay commanded state.	There is a problem on the associated VSVA board.

Fault	Fault Description	Possible Cause
101-104	Excitation relay Driver #{1-4} does not match commanded state The VSVA excitation switchover driver state output to the TSVA terminal board does not match the VSVA commanded state.	There may be a problem on the associated VSVA board. The TSVA terminal board may be the problem. The J3 or J4 37 pin cable may be the problem.
105-106	J3 Excitation relay #{1-2} does not match commanded state The TSVA LVDT Excitation 1 or 2 relay driver state does not match the commanded state. If the J5 cable is not connected, this diagnostic is suppressed. If the J5 cable and two TSVA terminal boards are used, the J12 cable must be installed.	The J3 TSVA terminal board may be the problem. Switchover Excitation Output (1 or 2) may be shorted at the J3 TSVA TB Screws.
107-108	J4 Excitation relay #{3-4} does not match commanded state The TSVA LVDT Excitation 3 or 4 relay driver state does not match the commanded state. If the J4 TSVA terminal board is used and J5 is connected to the J3 TSVA board, the J12 cable must be installed.	The J4 TSVA terminal board may be the problem. Switchover Excitation Output (1 or 2) may be shorted at the J4 TSVA TB Screws.
109-112	Regulator #{1-4} failed, exceeded position limits {value} Regulator position feedback is out limits. The limits are defined as: Regulator # MinPOSvalue - Servo # Fdbk_Suicide value = low limit. Regulator # MAXPOSvalue + Servo # Fdbk_Suicide value = high limit.	Minimum and maximum Regulator LVDT rms voltage limits are configured incorrectly. The assigned LVDTs may need recalibration. May be a problem on the VSVA board.
113-116	Excitation Failover #{1-4} limit exceeded {value} The LVDT Excitation # output is faulted. The VSVA fault detecting circuitry has toggled the selection relays on the TSVA terminal board four times within a 100 msec period attempting to select a good excitation source. This action has been repeated after waiting 16 seconds for the fault to go away. After 3 attempts separated by 16 seconds each, the VSVA boards will stop commanding the failover relays to toggle to prevent excessive long-term stress on the relays. (Nominal limit value displayed will be 12) If the fault goes away at any time and the Excitation Output returns to a healthy state, the failover detector circuits will restart and return to an active mode.	The LVDT Excitation output may be shorted. The LVDT Excitation output may be faulted to an open state on the TSVA terminal board.
117-120	Excitation #{1-4} Not Valid LVDT Excitation # Failover output has been faulted for more than three seconds at the failover detector comparator circuit.	Excitation Outputs may be shorted at the TSVA TB-1 Screw Inputs.
128	J3 TB ID not found or invalid JR1, JS1 or JT1 cable ID device on the TSVA terminal board connected to the J3 cable was not found.	The TSVA ID devices may have a problem. The VSVA has a problem reading the ID. The J3 cable connectors may not be properly mated.
129	J4 TB ID not found or invalid JR1, JS1 or JT1 cable ID device on the TSVA terminal board connected to the J4 cable was not found.	The TSVA ID devices may have a problem. The J4 cable connectors may not be properly mated.
130	J5 TB ID not found or invalid JR5, JS5 or JT5 cable ID device on the TSVA terminal board connected to the J5 cable was not found.	The TSVA ID devices may have a problem. The J5 cable connectors may not be properly mated.
131	J7 TB ID not found or invalid JR6, JS6 or JT6 cable ID device on the TSVA terminal board connected to the J7 cable was not found.	The TSVA ID devices may have a problem. The J7 cable connectors may not be properly mated.

Fault	Fault Description	Possible Cause
132	J8 TB ID not found or invalid JR6, JS6 or JT6 cable ID device on the TSVA terminal board connected to the J8 cable was not found.	The TSVA ID devices may have a problem. The J8 cable connectors may not be properly mated.
133	J3 + J7 TB ID Barcode Do NOT MATCH J3 and J7 cables must be connected to the same TSVA Terminal Board to properly close the Servo TMR total current regulation loops. If both the J3 and J7 cables are unconnected at power up, this diagnostic is suppressed.	The J3 37 pin cable and the J7 15 pin cables must be connected to the same TSVA. The TSVA ID devices may have a problem. The VSVA board may have a problem reading the ID devices.
134	J4 + J8 TB ID Barcode Do NOT MATCH J4 and J8 cables must be connected to the same TSVA Terminal Board to properly close the Servo TMR total current regulation loops. If both the J4 and J8 are unconnected at power up, this diagnostic is suppressed.	The J4 37 pin cable and the J8 15 pin cables must be connected to the same TSVA. The TSVA ID devices may have a problem. The VSVA board may have a problem reading the ID devices.
135-138	Servo #{1-4} Suicided Status of Servo Suicide state independent of a reason for the suicide condition.	VSVA Board may be off line or in the process of startup. Vsua board may have a problem.
139	RST Configuration mismatch of critical items The VSVA is not allowed to go Online following power on because one or more critical configuration parameters do not match between the R, S and T boards. If the code revision is a match, a configuration download is required.	Critical configuration parameters or the firmware revision do not match the other R, S or T VSVA boards in this slot location. Download the firmware and configuration to this board.
140	Redundant LVDT5+LVDT6 Vrms Diff > 0.5v {value} LVDT Excitation Output 1 ExciteMode is selected to Redundant and the LVDT 5 and 6 Vrms input values are not within 0.5VRMS of each other.	Wires on J3 TSVA Between TB-1 Screws 11 and 13 or 12 and 14 may be loose or missing. The VSVA board may have a problem.
141	Redundant LVDT11+LVDT12 Vrms Diff > 0.5v {value} LVDT Excitation Output 3 ExciteMode is selected to Redundant and LVDT 11 and 12 Vrms input values are not within 0.5VRMS of each other.	Wires on J4 TSVA Between TB-1 Screws 11 and 13 or 12 and 14 may be loose or missing. The VSVA board may have a fault.
142	J3 Redundant Excitation Loss Failure Detected LVDT5+LVDT6 LVDT Excitation Output 1 ExciteMode is selected to Redundant and the LVDT 6 input redundant loss detector disagreed with the LVDT 5 detector event detecting time.	Wires on J3 TSVA Between TB-1 Screws 11 and 13 or 12 and 14 may be loose or missing. The VSVA board may have a problem.
143	J4 Redundant Excitation Loss Failure Detected LVDT11+LVDT12 LVDT Excitation Output 3 ExciteMode is selected to Redundant and the LVDT 12 input redundant loss detector disagreed with the LVDT 11 detector event detecting time.	Wires on J4 TSVA Between TB-1 Screws 11 and 13 or 12 and 14 may be loose or missing. The VSVA board may have a fault.
160	LVDT4 Pre-Relay R1 Excitation Low {value} Mode 1 specific diagnostic alarm. The ER1 Excitation output for the J3 TSVA terminal board which must be wired to LVDT4 Input at the TSVA terminal board screws is < 6.6Vrms or > 7.7 Vrms.	The "R" VSVA board ER1 LVDT Excitation out has a problem. The transformer on the TSVA board may have an open winding. The J3 cable may be improperly mated, have an open wire/connector pin or a short between signal and ground.

Fault	Fault Description	Possible Cause
161	LVDT10 Pre-Relay R1 Excitation Low {value} Mode 1 specific diagnostic alarm. The ER1 Excitation output for the J4 TSVA terminal board which must be wired to LVDT4 Input at the J4 TSVA terminal board screws is < 6.6Vrms or > 7.7 Vrms.	The "R" VSVA board ER1 LVDT Excitation out has a problem. The transformer on the TSVA board may have an open winding. The J4 cable may be improperly mated, have an open wire/connector pin or a short between signal and ground.
162	Mode1 REG1 3_LVDT (1,2,3){#1 or 2 or 3} Exceeded TMR Median Diff Limit {value} LVDT 1, 2 and 3 inputs to Regulator 1 are compared to the median selected value. A diagnostic alarm is generated and the faulted LVDT # and value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
165	Mode1 REG3 3_LVDT (7,8,9){#7 or 8 or 9} Exceeded TMR Median Diff Limit {value} LVDT 7, 8 and 9 inputs to Regulator 3 are compared to the median selected value. A diagnostic alarm is generated and the faulted LVDT # and value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
170	Mode2 REG1 LVDT (1,2) Exceeded Diff Limit ({value}) {value} LVDT 1and 2 inputs to Regulator 1 are compared to either the Min or Max value dependent upon the RegType selection. A diagnostic alarm is generated and the fault value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
171	Mode2 REG2 LVDT (3,4) Exceeded Diff Limit ({value}) {value} LVDT 3 and 4 inputs to Regulator 2 are compared to either the Min or Max value dependent upon the RegType selection. A diagnostic alarm is generated and the fault value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
172	Mode2 REG3 LVDT (7,8) Exceeded Diff Limit ({value}) {value} LVDT 7 and 8 inputs to Regulator 3 are compared to either the Min or Max value dependent upon the RegType selection. A diagnostic alarm is generated and the fault value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
173	Mode2 REG4 LVDT (9,10) Exceeded Diff Limit ({value}) {value} LVDT 9 and 10 inputs to Regulator 4 are compared to either the Min or Max value dependent upon the RegType selection. A diagnostic alarm is generated and the fault value is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.

Fault	Fault Description	Possible Cause
174	Mode2 MON {1-12} LVDT (1,2) Exceeded Diff Limit {value} If LVDT input pair 1 and 2 are assigned to any of the Monitors 1-12, the LVDT inputs 1 and 2 are compared to either the Min or Max value dependent upon the Monitor type selection. A diagnostic alarm is generated and the faulted Monitor # is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
175	Mode2 MON {1-12} LVDT (3,4) Exceeded Diff Limit {value} If LVDT input pair 3 and 4 are assigned to any of the Monitors 1-12, the LVDT inputs 3 and 4 are compared to either the Min or Max value dependent upon the Monitor type selection. A diagnostic alarm is generated and the faulted Monitor # is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
176	Mode2 MON {1-12} LVDT (7,8) Exceeded Diff Limit {value} If LVDT input pair 7 and 8 are assigned to any of the Monitors 1-12, the LVDT inputs 7 and 8 are compared to either the Min or Max value dependent upon the Monitor type selection. A diagnostic alarm is generated and the faulted Monitor # is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
177	Mode2 MON {1-12} LVDT (9,10) Exceeded Diff Limit {value} If LVDT input pair 9 and 10 are assigned to any of the Monitors 1-12, the LVDT inputs 9 and 10 are compared to either the Min or Max value dependent upon the Monitor type selection. A diagnostic alarm is generated and the faulted Monitor # is inserted into the message if the TMR Median Diff Limit value is exceeded.	VSVA Board Electronics or the associated 37 pin cable may have an LVDT Input fault. Wire on LVDT input screws may be loose or missing.
180-191	Regulator LVDT #{1-12} rms voltage out of limits {value} Regulator LVDT # position input is out of limits. The Limits are defined as: Regulator MnLVDT#_Vrms – ((MxLVDT#_Vrms - MnLVDT#_Vrms) * LVDT_Margin percent /100) = Low Limit Regulator MnLVDT#_Vrms + ((MxLVDT#_Vrms - MnLVDT#_Vrms) * LVDT_Margin percent /100) = High Limit	Minimum and maximum Regulator LVDT rms voltage limits are configured incorrectly. The LVDT may need recalibration. May be a problem on the VSVA board.
192-255	Logic Signal {name} Voting Mismatch The specified signal from this VSVA disagrees with the TMR voted value. Voter Disagreement Diagnostic	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
288-323	Input Signal {name} Voting Mismatch, Local={value}, Voted={value} The specified input signal from this VSVA varies from the voted value of the signal by more than the TMR Diff Limit value. Voter Disagreement Diagnostic.	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable

VSCA Serial Communication Input/Output

VSCA Serial Communication Input/Output

Functional Description

The Serial Communication Input/Output (VSCA) board provides I/O interfaces for external devices using RS-232C, RS-422, and RS-485 serial communications. Currently the IS200VSCAH2A version is available. The DSCB terminal board connects to the external devices, which include intelligent pressure sensors such as smart Honeywell[®] pressure transducers and Kollmorgen[®] electric drives.

VSCA connects to the DSCB terminal board(s) through the J6 and J7 front panel connectors. These are parallel connected using 37-pin D shell connectors with group shielded twisted pair wiring. For RS-422 and RS-485, DSCB can interface with external devices at distances up to 1000 ft, at baud rates up to 375 kbps. For RS-232C, the distance is only 50 ft or 2500 pF of cable capacitance (including the cable from VSCA to the DSCB). It supports short haul modems for longer distances.

Installation

➤ To install the V-type board

- 1 Power down the VME I/O processor rack.
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors.
- 3 Tighten the captive screws at the top and bottom of the front panel.

Note Cable connections to the terminal boards are made at the J6 and J7 connectors on the front panel. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel; for details refer to the section on diagnostics in this document.

It may be necessary to update the VSCA firmware to the latest level. For instructions, refer to *GEH-6403 Control System Toolbox for the Mark VI Turbine Controller*.

Operation

Note VSCA/DSCB is a data terminal device (DTE).

The VSCA is a single slot board with six serial communication ports. Each port can be independently configurable as an RS-232C, RS-485, or RS-422 interface, using a three-position group jumper (berg array). Both RS-232C and RS-422 support full duplex. The line drivers on VSCA include appropriate termination resistors with configurable jumpers to accommodate multi-drop line networks. RS-422 and RS-485 outputs have tri-state capability. I/O goes to a high impedance condition when powered down. They do not cause significant disturbance when powered down/up (less than 10 ms) on a party line. The open wire condition on a receiver is biased to a high state.s

- RS-232C supports: RXD, TXD, DTR/RTS, GND, CTS (five wire)
- RS-422 supports: TX+, TX-, RX+, RX-, GND
- RS-485 supports: TX/RX+, TX/RX-, GND

Data Flow from VSCA to Controller

The data flow from VSCA to the UCV_ controller is of two types: fixed I/O and Modbus[®] I/O. Fixed I/O is associated with the smart pressure transducers and the Kollmorgen electric drive data. This data processes completely, every frame, as with conventional I/O. The required frame rate is 100 Hz. These signals are mapped into signal space, using the .tre file, and have individual health bits, use system limit checking, and have offset/gain scaling.

Note Two consecutive time outs are required before a signal is declared unhealthy. Diagnostic messages are used to annunciate all communication problems.

Modbus I/O is associated with the Modbus ports. Because of the quantity of these signals, they are not completely processed every frame. Instead they are packetized and transferred to the UCV_ processor over the IONet through a special service. This accommodates up to 2400 bytes at 4 Hz, or 9600 bytes at 1 Hz, or combinations thereof. This I/O is known as second class I/O, where coherency is at the signal level only, not at the device or board level. Health bits are assigned at the device level, the UCV_ expands (fully populate) for all signals, and system limit checking is not performed.

Ports 1 and 2 only (as an option) support the Honeywell pressure configuration. It reads inputs from the Honeywell smart pressure transducers, type LG-1237. This service is available on ports 1 and 2 as an option (pressure transducers or Modbus, or drives). The pressure transducer protocol uses the XDSAG#AC interface board and RS-422. Each port can service up to six transducers. The service is 375 kbaud, asynchronous, and with nine data bits (11 bits including start and stop). It includes the following failsafe features:

- Communication miss counters, one per device, and associated diagnostics
- After four consecutive misses it forces the input pressure to 1.0 psi, and posts a diagnostic. After four consecutive hits (good values) it removes the forcing and the diagnostic.

Three ports (any three, but no more than three) support the Kollmorgen electric drive. It communicates with a Kollmorgen electric fast drive FD170/8R2-004 at a 19200 baud rate, point-to-point, using RS-422.

Modbus service

The current Modbus design supports the master mode. However the design does not prevent the future enhancement of Modbus slave mode of operation. It is configurable at the port level as follows:

- Used, not used
- Baud Rate RS-232C: 300, 600, 1200, 2400, 4800, 9600, 19200, 38400, 57600
- Baud Rate RS-485/422: 19200, 38400, 57600, 115000
- Parity: none, odd, even
- Data bits: seven, eight
- Stop bits: one, two
- Station addresses
- Multi-drop, up to eight devices per port; maximum of 18 devices per board
- RTU
- Time out (seconds) per device

The Modbus service is configurable at the signal level as follows:

- Signal type
- Register number
- Read/write
- Transfer rate, 0.5, 1, 2, or 4 Hz
- Scaling, offset, and gain

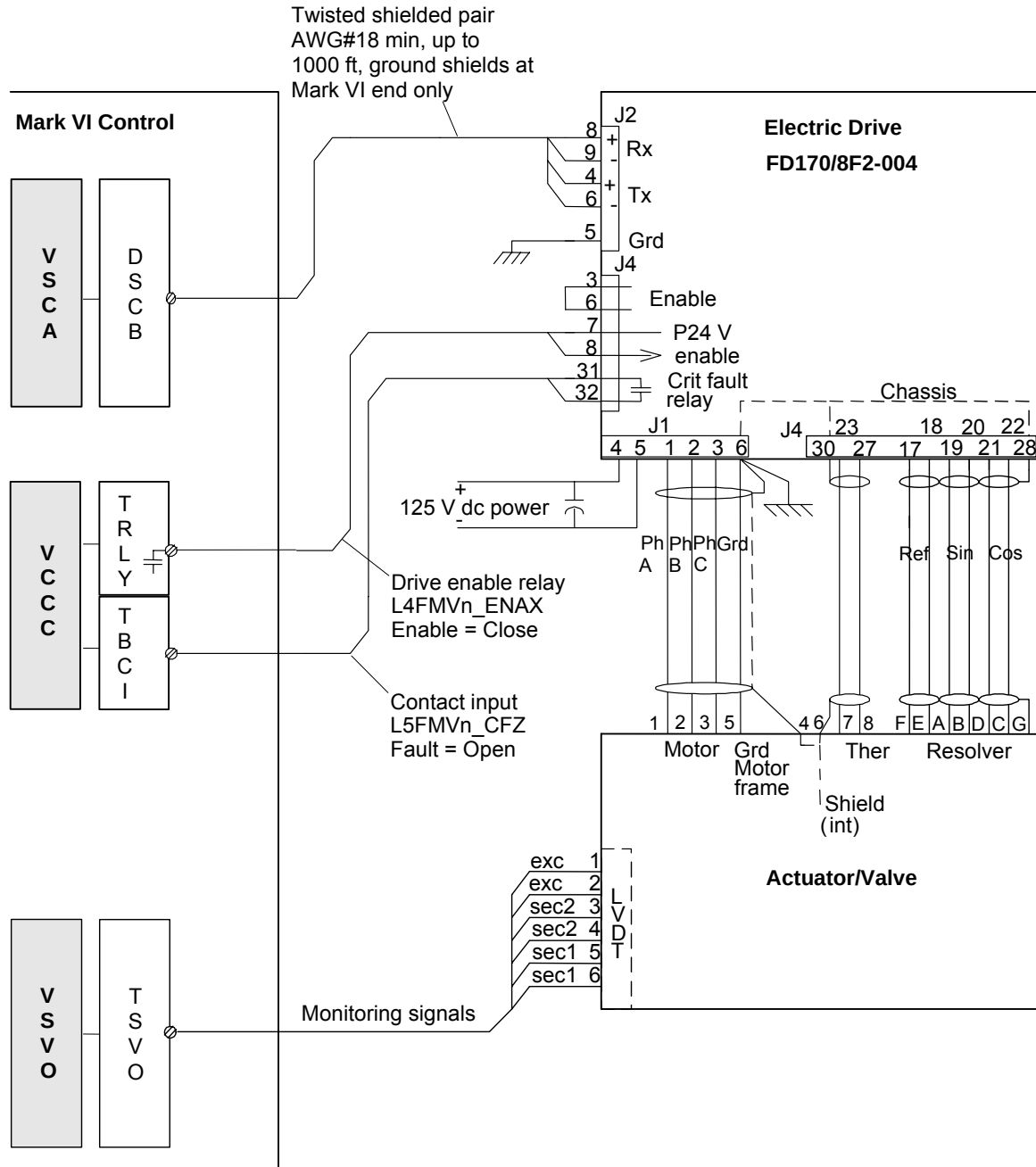
The service supports function codes 1-7, 15, and 16. It also supports double 16-bit registers for floating point numbers and 32-bit counters. It periodically tries 20 attempts to reestablish communications with a dead station. The VSCA and toolbox support type casting and scaling of all I/O signals to/from engineering units, for both fixed I/O and Modbus I/O.

Physical interfaces

Special connections are required for RS-485 applications with VSCA/DSCB located somewhere in the middle of the transmission path. Because of the potential length of the connection between VSCA and DSCB, there may be substantial stub length to the connection that will affect signal quality. For this reason, VSCA supports the connection of two DSCB boards wired in parallel. This permits RS-485 signals to come in one DSCB, pass through VSCA with the RS-485 transceiver, and go out the opposite DSCB. This ensures that the stub-length of the RS-485 path is minimized.

Note The above arrangement is not required when the VSCA/DSCB is located at one end of the RS-485 wiring.

The following figure shows the physical interface to the electric drives. For the Honeywell transducer interface using DSCB and DPWA, refer to the section, *DSCB Serial Input/Output*.



VSCA Interface to Electric Servo Drive using DSCB Board

Specifications

Item	Specification			
Number of Serial Ports	6 per VSCA board			
Devices	Port	Pressure Transducer	Electric Drive*	Modbus Comm.
	1	Y	Y	Y
	2	Y	Y	Y
	3	-	Y	Y
	4	-	Y	Y
	5	-	Y	Y
	6	-	Y	Y
	Type	RS-422 (375 KB)	RS-422 (19.2 KB)	RS-232 (57.6 KB) RS-422 (115 KB) RS-485 (115 KB)
	Boards	DSCB, DPWA	DSCB	DSCB
Choices (jumper select)				
RS-232C	50 ft	Baud Rates up to 57.6 kbps.		Full duplex
RS-422	1000 ft	Baud Rates up to 375 kbps		
RS-485	1000 ft	Baud Rates up to 375 kbps		Full duplex
Ports 1 and 2	Honeywell pressure transducers, 6 transducers per port using XDSA board			
Ports 1 through 6	Modbus operation or Kollmorgen electric fast drive FD170/8R2-004. * Note			
Size	26.04 cm high x 1.99 cm wide x 18.73 cm deep (10.25 in. x 0.78 x 7.375 in.)			

Note Any three ports, but no more than three, can support the electric drive.

Diagnostics

Three LEDs at the top of the VSCA front panel provide status information. The normal RUN condition is a flashing green, and FAIL is a solid red. The third LED shows a steady orange if a diagnostic alarm condition exists in the board. Diagnostic checks include the following:

- Each port checks communications and if there is no response, or bad data, or the communication port is non functional, a diagnostic fault is set. This creates a composite diagnostic alarm, L3DIAG_VSCA, referring to the entire board. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each terminal board has its own ID device, which is interrogated by the I/O board. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JA1 connector. When the chip is read by the I/O board and a mismatch is encountered, a hardware incompatibility fault is created.

Details of diagnostic faults generated by the electric actuator are a separate category and are listed in the *Alarms* section of this document.

Configuration

VSCA is configured with board jumpers and with the toolbox. Jumpers JP1 through JP6 are block jumpers, used to select the port electrical characteristic, RS-232C, RS-422, or RS-485. Each jumper has three positions marked 232, 422, and 485.

Jumpers JP7 through JP12 are block jumpers, used to select the correct termination configuration for all the transmission lines (Tx). Each jumper has three positions marked TRM, THR, and PRK where:

- TRM means with terminating resistor.
- THR means no terminating resistor, pass through to J7.
- PRK means no terminating resistor, or park position

Jumpers JP13 through JP18 are block jumpers, and are used to select the correct termination configuration for all the receive lines (Rx). Each jumper has three positions marked, TRM, THR, and PRK, where the meanings are the same as above.

A two-position jumper, JPU1, selects between Honeywell pressure transducer and Modbus operation for ports 1 and 2. The default position for JPU1 is X2, which enables the serial clock for operation with Honeywell transducers. Position X1 selects the clock needed for Modbus operation. JPU1 is located at the bottom of the board towards the backplane connector (away from the other jumpers).

VSCA Board Jumper Positions

Network Port Number	232/422/485 Communication	Tx TRM/THR/PRK	Rx TRM/THR/PRK
Port 1	JP1	JP7	JP13
Port 2	JP2	JP8	JP14
Port 3	JP3	JP9	JP15
Port 4	JP4	JP10	JP16
Port 5	JP5	JP11	JP17
Port 6	JP6	JP12	JP18

Parameter	Description	Choices
VSCA_Crd_Cfg		
Pressure_Port1_Cfg		
PortNum	Toolbox Parameter, Applicable port, Port 1 only	
PortType	Type of VSCA port	
Priority	Priority	None, Odd, Even
PhyConnect	Type of physical connection	RS-232, RS-422, RS-485
TermType	Type of Termination	None, Terminated, Pass through
BitsPerChar	Bits per character	7 Bits, 8 Bits, 9 Bits
Parity	Normal parity	None, Odd, Even
StopBits	Normal Parity	1 StopBit, 2 StopBit
Baud	Baud rate	
DevAddr1	Device Address for transducer (first of six devices)	
TimeOut	Time out in msec	10 ... 60000
Pressure_Port2_Cfg	(Similar configuration, for six devices)	
PressureXdr_Pnt_Cfg		

Parameter	Description	Choices
RawMin	Scaling Factor Raw Limit	-3.4E+038, +3.4E+038
RawMax	Scaling Factor Raw Limit	-3.4E+038, +3.4E+038
EngMin	Scaling Factor eng limit	-3.4E+038, +3.4E+038
EngMax	Scaling Factor eng limit	-3.4E+038, +3.4E+038
Lim1Enable	Enable Limit 1 check	Disable, Enable
Lim1_Latch	Latch error limit 1	NotLatch, Latch
Lim1Comp	Latch error compare (Similar for Lim2)	<=, >=
Limit1	Limit 1	
Limit2	Limit 2	
ElectDrive_Port_Cfg		
PortNum	Toolbox Parameter, Applicable port, Port 1 thru 6	
PortType	Type of VSCA port	
Priority	Priority	None, Odd, Even
PhyConnect	Type of physical connection	RS-232, RS-422, RS-485
TermType	Type of Termination	None, Terminated, Pass through
BitsPerChar	Bits per character	7 Bits, 8 Bits, 9 Bits
Parity	Normal parity	None, Odd, Even
StopBits	Normal Parity	1 StopBit, 2 StopBit
Baud	Baud rate	
ATA	Drive parameter, Ampl Temp Alarm	
PCP	Drive parameter, Position Loop Comp	
PDP	Drive parameter, Position Loop Comp	
PIN	Drive parameter, Position Integral Gain	
PPN	Drive parameter, Position Loop Proportional Gain	
RES_p1	Drive parameter, Resolver excit amplitude	
RES_p2	Drive parameter, Resolver excit freq	
RMS_p1	Drive parameter, Resolver excit freq	
RMS_p2	Drive parameter, Resolver excit freq	
RTL_p1	Drive parameter, Time limit	
RTL_p2	Drive parameter, Time limit	
TOF	Drive parameter, Torque Offset	
TimeOut	Time Out in msec	10 ... 60000
ElectDriveRefCfg		
RawMin	Scaling Factor Raw Limit	-3.4E+038, +3.4E+038
RawMax	Scaling Factor Raw Limit	-3.4E+038, +3.4E+038
EngMin	Scaling Factor eng limit	-3.4E+038, +3.4E+038
EngMax	Scaling Factor eng limit	-3.4E+038, +3.4E+038
ElectDrivePosCfg	(Similar to PressureXdr_Pnt_Cfg)	
ElectDriveVelCfg	(Similar to ElectDriveRefCfg)	
ElectDriveTorCfg	(Similar to ElectDriveVelCfg)	
Modbus_Port_Cfg		
PortNum	Toolbox Parameter, which port, Port 1 thru 6	
PortType	Type of VSCA port	
Priority	Priority	0 ... 7
PhyConnect	Type of physical connection	RS-232, RS-422, RS-485
TermType	Type of Termination	None, Terminated, Pass through
BitsPerChar	Bits per character	7 Bits, 8 Bits, 9 Bits

Parameter	Description	Choices
Parity	Normal parity	None, Odd, Even
StopBits	Normal Parity	1 StopBit, 2 StopBit
Baud	Baud rate	300, 600, 800, 1200, 2400, 9600, 115000, 192000, 384000, 57600, 375000.
StationCount	Toolbox Parameter, Number of stations	
Modbus_Station_Cfg		
StationAddr	What is station address	1 ... 255
PageCount	Toolbox Parameter, Number of Pages	
TimeOut	Time Out in msec	10 ... 60000
FuncCode15	The connected station supports Modbus command FC15 Force Mult Coils.	Enable, Disable
FuncCode16	The connected station supports Modbus command FC16 Write Mult Registers.	Enable, Disable
DataSwap	Float Data Format, swap words, ie Most Significant first	LswFirst, MswFirst
MaxBools	Maximum Number of Booleans per request	-32768 ... +32767
MaxReg	Maximum Number of Registers per request	-32768 ... +32767
DeviceDelay	Transmit Delay Time in msec for non Modbus compliant slaves	0 ... 60000
Modbus_Page_Cfg		
PageType	What is the page type – HC, HR, OC, CC ...	
PointCount	Toolbox Parameter, Number of points	
Modbus_Bit_Cfg		
Address	Address of remote Register/Discrete	1 ... 9999
BitNumber	Bit-Packed register bit number –1 = Not Used	0 or –1
RemDataType	Data-type of remote register/discrete	UNS16, PAC16, SIGN16
UpdateRate	The rate at which inputs are updated – Never means spare	½, 1, 2, 4 Hz
RawMin	Scaling factor raw minimum	-3.4E+038, +3.4E+038
RawMax	Scaling factor raw maximum	-3.4E+038, +3.4E+038
EngMin	Scaling factor engineering minimum	-3.4E+038, +3.4E+038
EngMax	Scaling factor engineering maximum	-3.4E+038, +3.4E+038
Modbus_Long_Cfg	(Similar to Modbus_Bit_Cfg)	
Modbus_Float_Cfg		
Address	Address of remote Register/Discrete	
BitNumber	Bit-Packed register bit number –0 = LSB (Similar to Modbus_Bit_Cfg)	-1 or 0
PointDefs		
	Pressure Transducer Port 1 and 2 Point Definitions.	
	Electric Drive Port Point Definitions (see drive Faults in the Alarm section).	

Alarms

VSCA I/O Board Diagnostic Alarms

Fault	Fault Description	Possible Cause
2	Flash ,memory CRCCRC failure	Board firmware programming error (board will not go online)
3	CRCCRC failure override is active	Board firmware programming error (board is allowed to go online)
16	System limit checking is disabled	System checking was disabled by configuration
30	ConfigCompatCode mismatch; Firmware: []	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory
31	IOCompatCode mismatch; Firmware: []	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32	Port [] Device/Station [] No Response	Message sent but no response received. Hardware or software configuration error.
33	Port [] Device/Station [] Bad Data	Message sent but bad data received. Software configuration error
34	Configure problem, Port [] , Communications nonfunctional	No communications taking place. Hardware or software configuration error
35	Electric drive, Port [] , save command non functional	
36	Card ID failure	
37	P6 ID failure	

Electric Actuator Diagnostic Alarms

Fault (Point Definition)	Note
L5FMV_CF	Drive critical fault
L3FMV_RST	Drive reset fault feedback
L5FMV_LRC	Drive LRC fault
L5FMV_BOV	Fault, Bus overvoltage (> 240 V)
L5FMV_BUV	Fault, Bus undervoltage (< 90 V)
L30FMV_LVA	Alarm, Low Volts (< 100 V)
L5FMV_WDT	Fault, Watch Dog Timer
L5FMV_OVC	Fault, Bridge Over-Current
L5FMV_POR	Fault, Power On Reset
L5FMV_ATF	Fault, Ampl. Temperature
L5FMV_MTF	Fault, Motor Temperature
L30FMV_RMS	Alarm, Alarm, RMS Over-current
L5FMV_PCF	Fault, Position Control
L5FMV_RTL	Fault, Commun. Time Limit.
L5FMV_CSL	Fault, Check Sum Limit.
L5FMV_CVL	Fault, Control Volts Limit
L5FMV_PF	Fault, Processor Failure
L5FMV_RF	Fault, Resolver Limit

DSCB Simplex Serial Communication Input/Output

Functional Description

The Simplex Serial Communication Input/Output (DSCB) terminal board is a compact interface terminal board, designed for DIN-rail mounting. DSCB connects to the VSCA board with a 37-wire cable. VSCA provides communication interfaces with external devices, using RS-232C, RS-422, and RS-485 serial communications. DSCB is wired to the external devices, which include intelligent pressure sensors such as the smart Honeywell[®] Pressure Transducers and Kollmorgen[®] Electric Drives used for valve actuation.

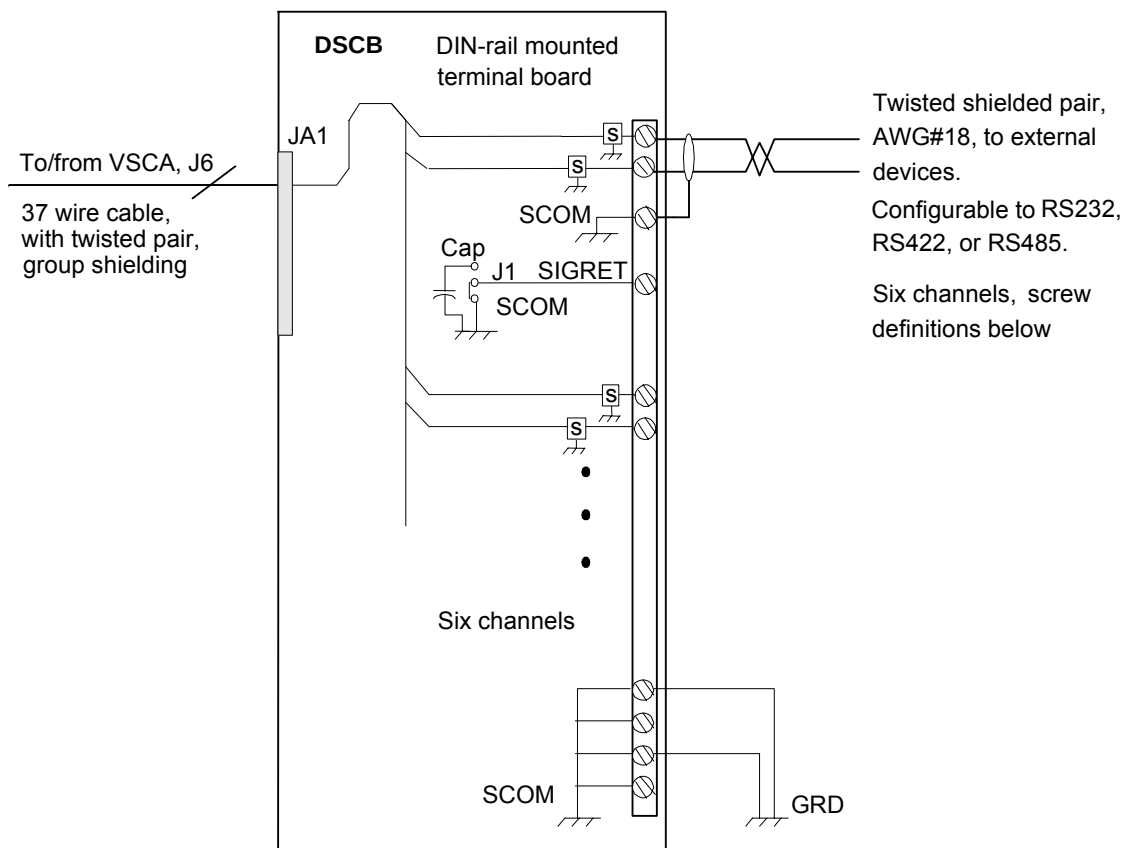
Wiring to devices uses shielded twisted pair. DSCB communication signals have on-board noise suppression. An on-board ID chip identifies the board to VSCA for system diagnostic purposes.

Note DSCB does not work with the PSCA I/O pack.

Installation

Mount the plastic holder on the DIN-rail and slide the DSCB board into place. Connect the wires for the external devices to the Euro-Block type terminal block as shown in the following figure. Four terminals are provided for the SCOM (ground) connection, which should be as short as possible. Connect DSCB to VSCA using the 37 pin JA1 connector.

Note Jumpers J1 - J6 direct SIGRET directly to SCOM or through a capacitor to SCOM. The shield must be grounded at one end or the other, but not both. If the shield is grounded at the device end, the jumpers should be set to include the capacitor in the circuit. If the shield is not grounded at the device end, the jumpers should be set to go directly to SCOM.



DSCB Terminal Assignments

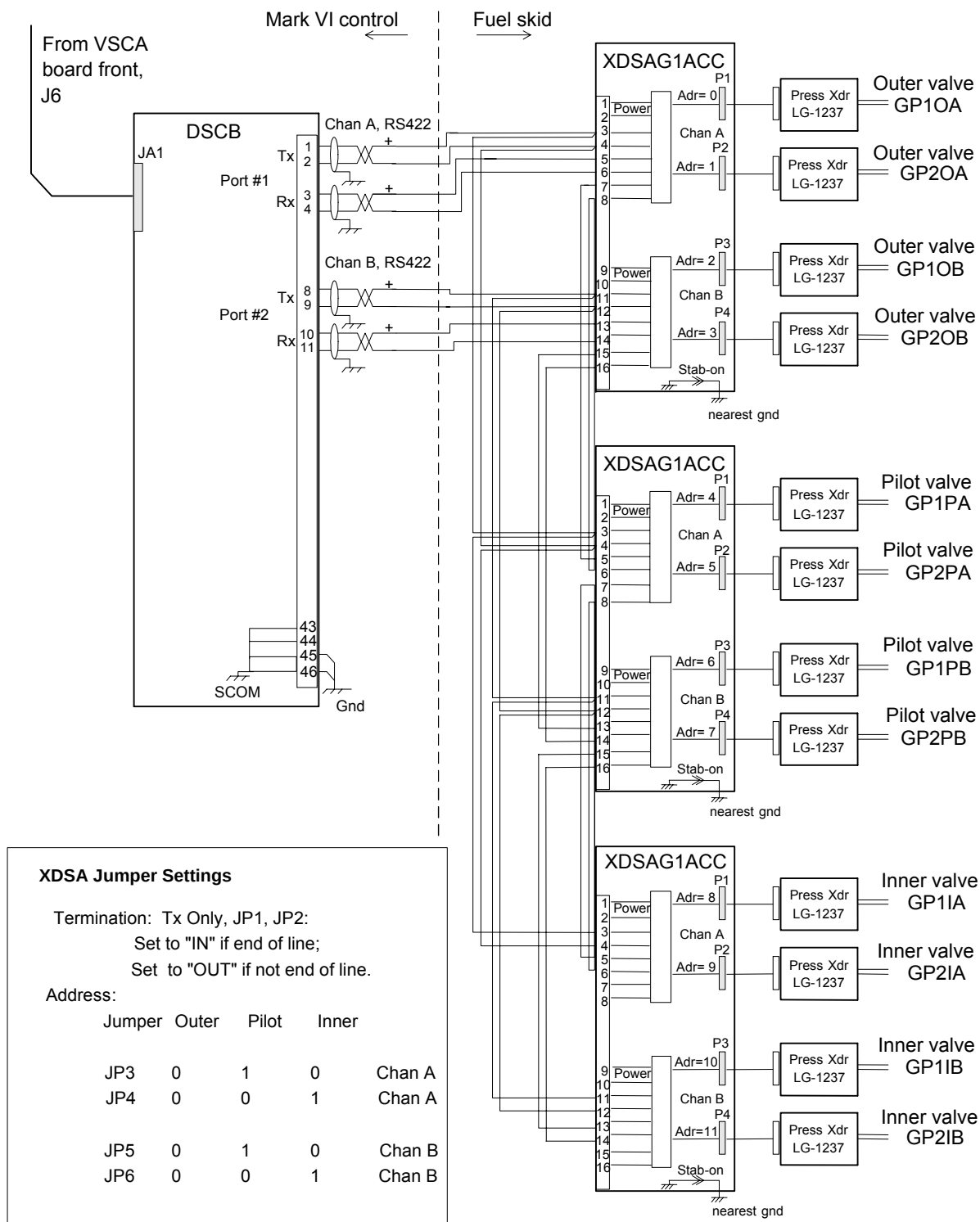
RS422	TX+	TX-	RX+	RX-	NC	SIGRET	JPx	SCOM
RS485	NC	NC	Tx/RX+	Tx/RX-	NC	SIGRET	JPx	SCOM
RS232	CTS	DTR/RTS	RX	NC	TX	SIGRET	JPx	SCOM
Chan 1	1	2	3	4	5	6	JP1	7
Chan 2	8	9	10	11	12	13	JP2	14
Chan 3	15	16	17	18	19	20	JP3	21
Chan 4	22	23	24	25	26	27	JP4	28
Chan 5	29	30	31	32	33	34	JP5	35
Chan 6	36	37	38	39	40	41	JP6	42
								43,44,45,46

Comments: The RS422/RS485 transmit and receive pairs must use a twisted pair in the VSCA to DSCB

DSCB Wiring, Cabling, and Jumper Positions

Operation

The three XDSA boards are intermediate distribution boards for the RS-422 multi-drop signals. The pressure transducers plug into ports P1, P2, P3, and P4 on these boards. The following figure shows DSCB using two of the six VSCA channels, Ports 1 and 2, to interface with 12 Honeywell pressure transducers.



Specifications

Item	Specification
Number of Channels	Six
Choices (jumper select on VSCA)	
RS-232C	50 feet Baud Rates up to 57.6 kbps Full duplex
RS-422	1000 feet Baud Rates up to 375 kbps
RS-485	1000 feet Baud Rates up to 375 kbps Full duplex
Connector for VSCA cable	37-pin D shell connector
Size, with support plate	8.6 cm Wide X 16.2 cm High (3.4 in x 6.37 in)

Diagnostics

The DSCB terminal board has its own ID device, which is interrogated by VSCA. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JA1 connector. When the chip is read by VSCA and a mismatch is encountered, a hardware incompatibility fault is created. Communication and device problems are detected by the VSCA and reported to the toolbox.

Configuration

Each of the six channels has a jumper to connect the cable shield to ground through a capacitor. These are used when the shield is grounded at the device end. The jumper positions are shown in the Installation section. All other configuration is done on the VSCA board and in the toolbox.

DPWA Transducer Power Distribution

Functional Description

The Transducer Power Distribution (DPWA) terminal board is a DIN-rail mounted power distribution board. It accepts input voltage of 28 V dc $\pm 5\%$, provided through a two-pin Mate-N-Lok[®] connector. Connectors are provided for two independent power sources to allow the use of redundant supplies. The input can accept power from a floating isolated voltage source. The input to DPWA includes two 1 k Ω resistors from positive and negative input power to SCOM. These center a floating power source on SCOM. Attenuated input voltage is provided for external monitoring. Output power of 12 V dc $\pm 5\%$ is connected to external devices through a Euro- type terminal block, using screw terminals and AWG#18 twisted-pair wiring. DPWA provides three output terminal pairs with a total output rated at 0 to 1.2 A. The outputs are compatible with the XDSAG#AC interface board. Outputs are short circuit-protected and self-recovering.

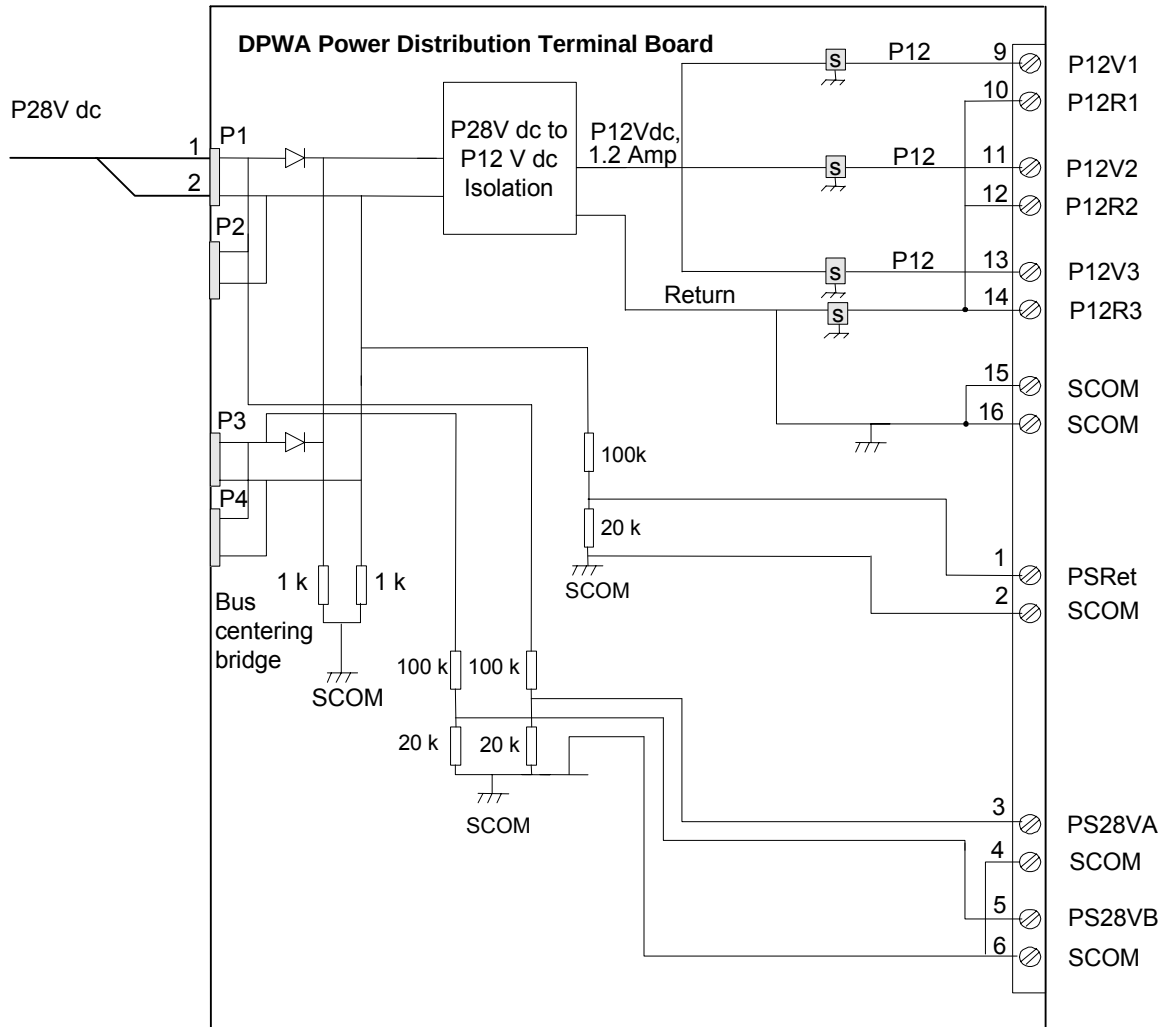
Note DPWA provides excitation power to LG-1237 Honeywell pressure transducers.

Installation

Mount the DPWA assembly on a standard DIN-rail. Connect input power to connector P1. If multiple DPWA boards are used, use connector P2 as a pass-through connection point for the power to additional boards. If a redundant power input is provided, connect power to connector P3 and use connector P4 as the pass-through to additional boards.

Connect the wires for the three output power circuits on screw terminal pairs 9-10, 11-12, and 13-14.

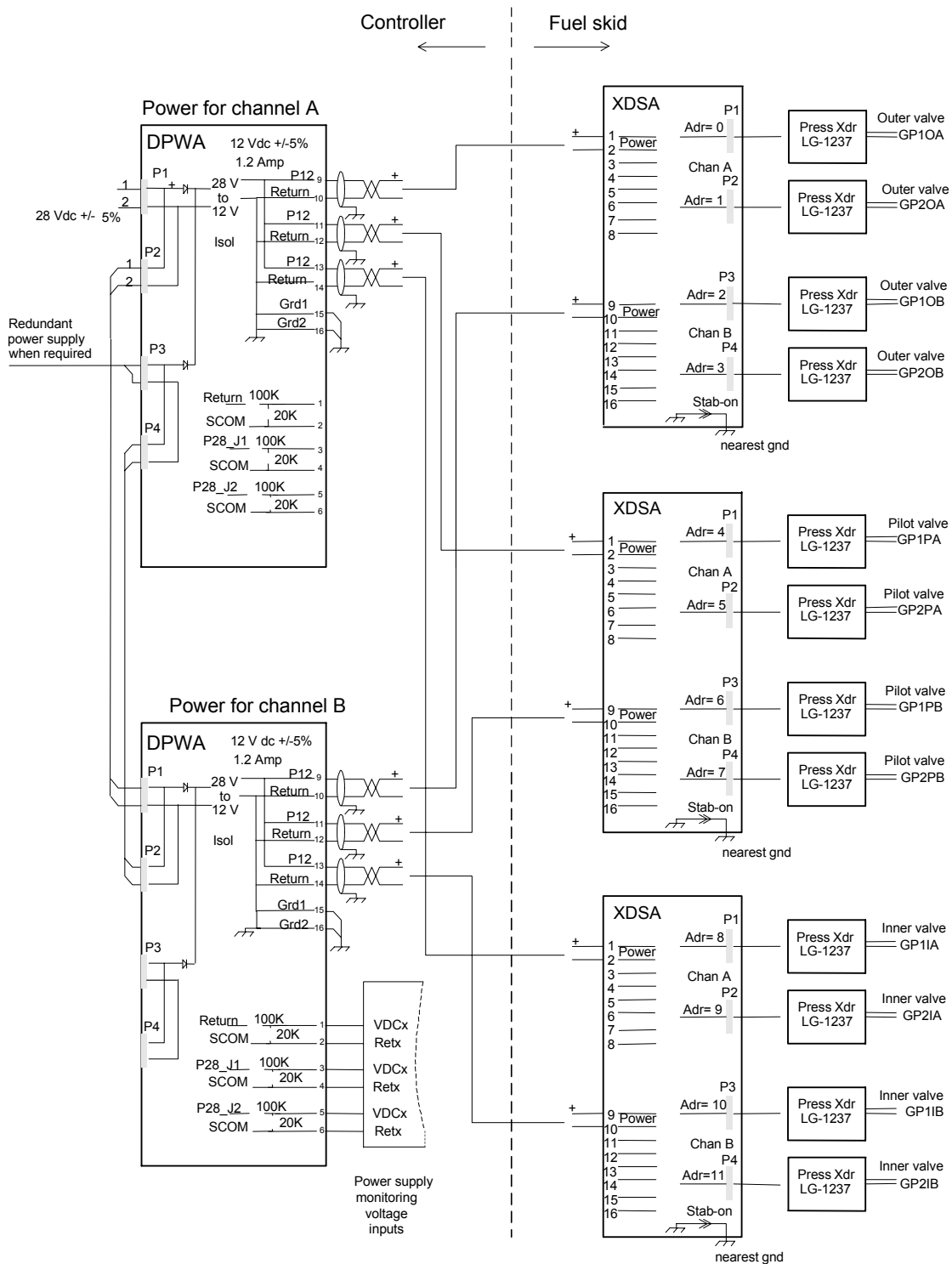
Note The DPWA terminal board includes two screw terminals, 15 and 16, for SCOM (ground) that must be connected to a good shield ground.



DPWA Board Block Diagram

Operation

DPWA has an on-board power converter that changes the 28 V dc to 12 V dc for the transducers. A redundant 28 V dc supply can be added if needed. The following figure shows the DPWA power distribution system feeding power to 12 LG-1237 pressure transducers.



DPWA Power Distribution to XDSA and Smart Pressure Transducers

Specifications

Item	Specification
Number of Channels	Three power output terminal pairs
Input voltage	28 V dc $\pm 5\%$, provisions for redundant source
Input current	Limited by protection to no more than 1.6 A steady state
Output voltage	12 V dc $\pm 5\%$, maximum total current of 1.2 A, short circuit protected, and self-recovering
Monitor voltages	Attenuated by 6:1 ratio

Diagnostics

DPWA features three voltage outputs to permit monitoring of the board input power. The voltage monitor outputs are all attenuated by a 6:1 ratio to permit reading the 28 V dc using an input voltage with 5 V dc full scale input. Terminal 1 (PSRet) is the attenuated voltage present on the power input return line. Terminal 3 (PS28VA) is the attenuated voltage present on the P1 positive power input line. Terminal 5 (PS28VB) is the attenuated voltage present on the P3 positive power input line. Terminals 2, 4, and 6 provide a return SCOM path for the attenuator signals. In redundant systems, monitoring PS28VA and PS28VB permits the detection of a failed or missing redundant input. In systems with floating 28 V power, with the input centered on SCOM, the positive and return voltages should be approximately the same magnitude as a negative voltage on the return. If a ground fault is present in the input power, it may be detected by positive or return attenuated voltage approaching SCOM while the other signal doubles.

Configuration

There are no jumpers or hardware settings on the board.

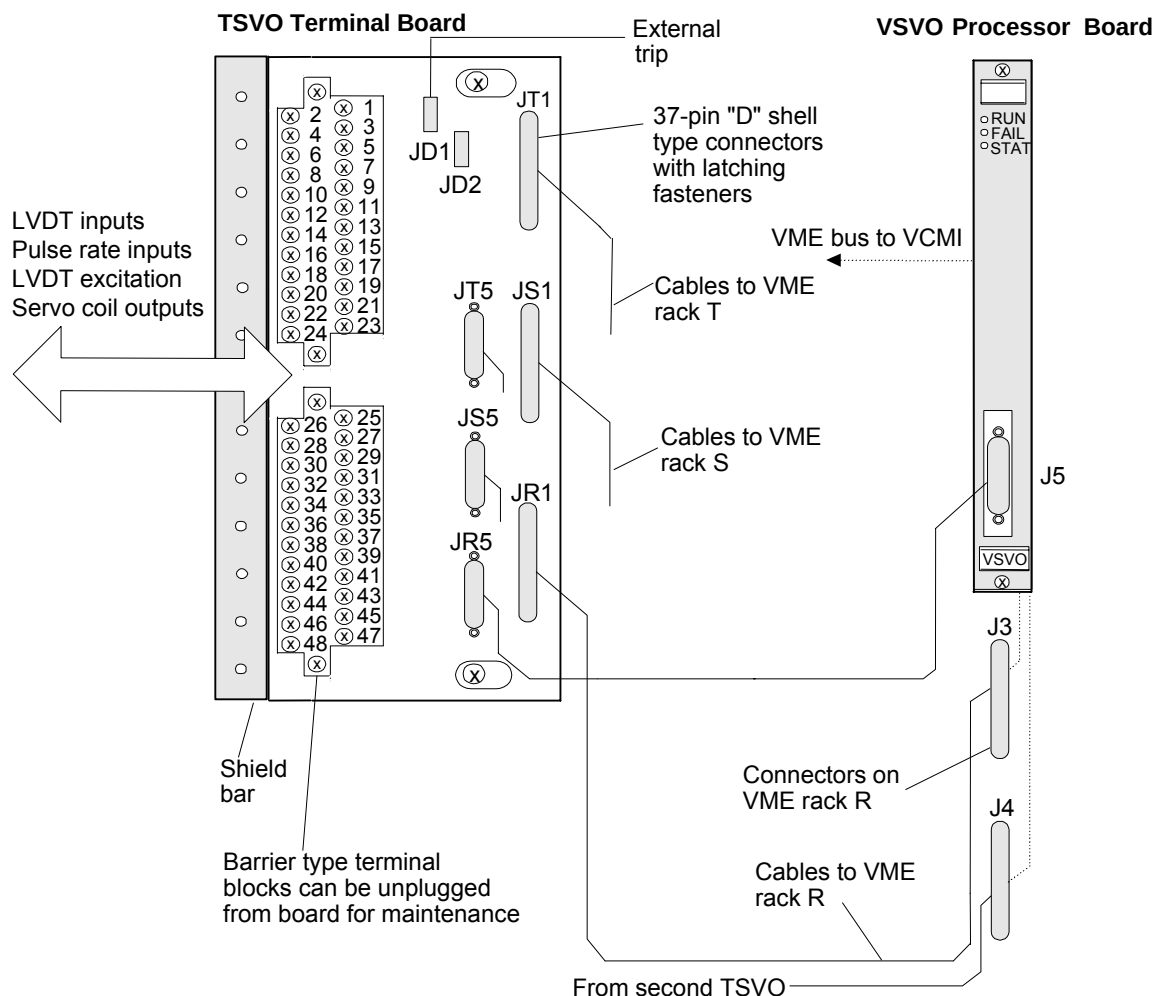
VSVO Servo Control

VSVO Servo Control

Functional Description

The Servo Control (VSVO) board controls four electro-hydraulic servo valves that actuate the steam/fuel valves. These four channels are usually divided between two servo terminal boards (TSVO or DSVO). Valve position is measured with linear variable differential transformers (LVDT). The loop control algorithm is run in the VSVO.

Three cables connect to VSVO on J5 plug on the front panel and the J3/J4 connectors on the VME rack. TSVO provides simplex signals through the JR1 connector, and fans out TMR signals to the JR1, JS1, and JT1 connectors. Plugs JD1 or JD2 are for external trips from the protection module.



Servo/LVDT Terminal Board, VSVO Processor Board, and Cabling

Installation

➤ To install the V-type board

- 1** Power down the VME processor rack
- 2** Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3** Tighten the captive screws at the top and bottom of the front panel

Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the section on diagnostics in this document.

Operation

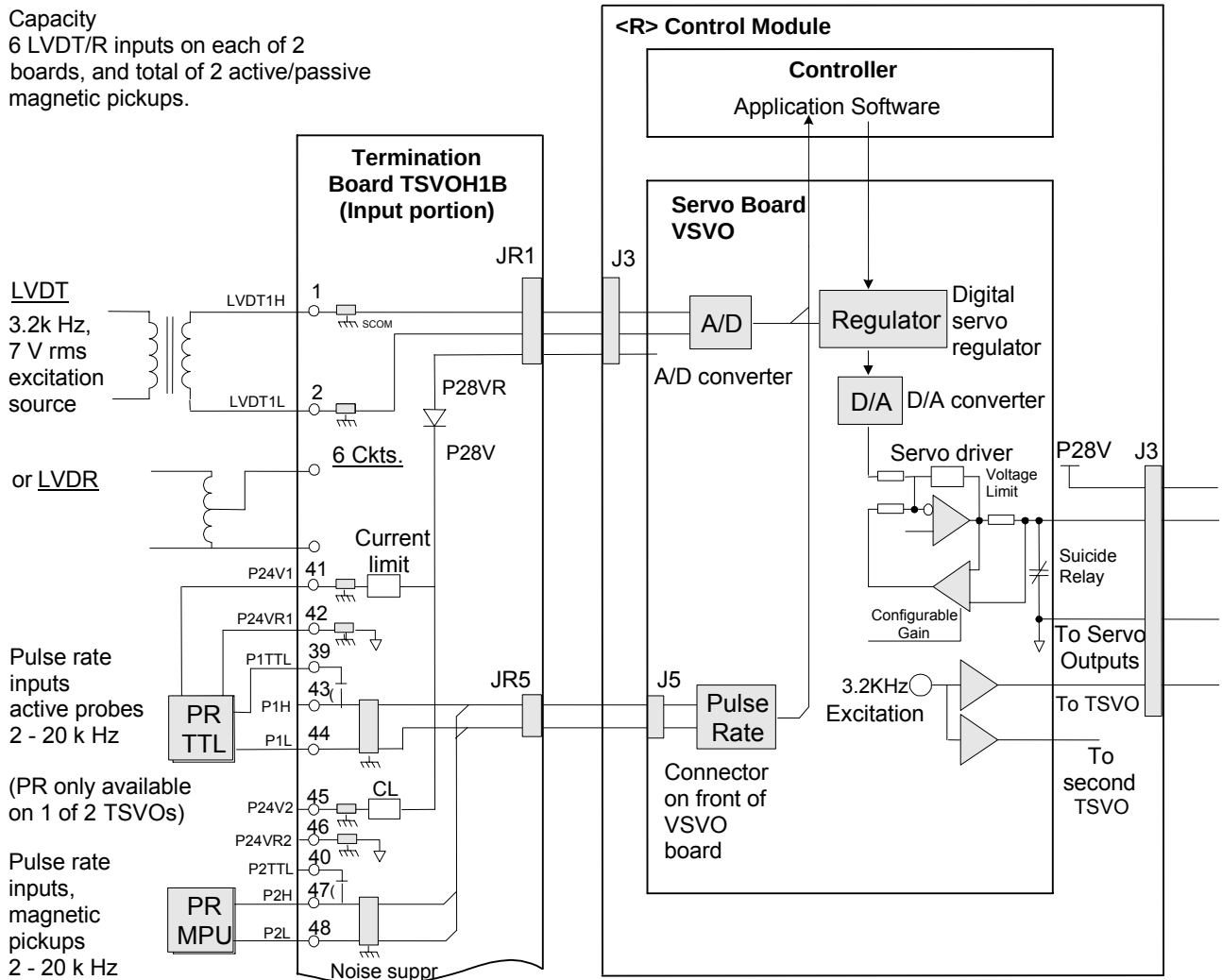
VSVO provides four channels consisting of bi-directional servo current outputs, LVDT position feedback, LVDT excitation, and pulse rate flows inputs. The TSVO provides excitation for, and accepts inputs from , up to six LVDT valve position inputs. There is a choice of one, two three, or four LVDTs for each servo control loop. Three inputs are available for gas turbine flow measuring applications. These signals come through TSVO and go directly to the VSVO board front at J5.

Each servo output is equipped with an individual suicide relay under firmware control that shorts the VSVO output signal to signal common when de-energized, and recovers to nominal limits after a manual reset command is issued. Diagnostics monitor the output status of each servo voltage, current, and suicide relay.

Simplex Systems

VSVO circuits for a simplex system are shown in the following figures.

Capacity
6 LVDT/R inputs on each of 2
boards, and total of 2 active/passive
magnetic pickups.

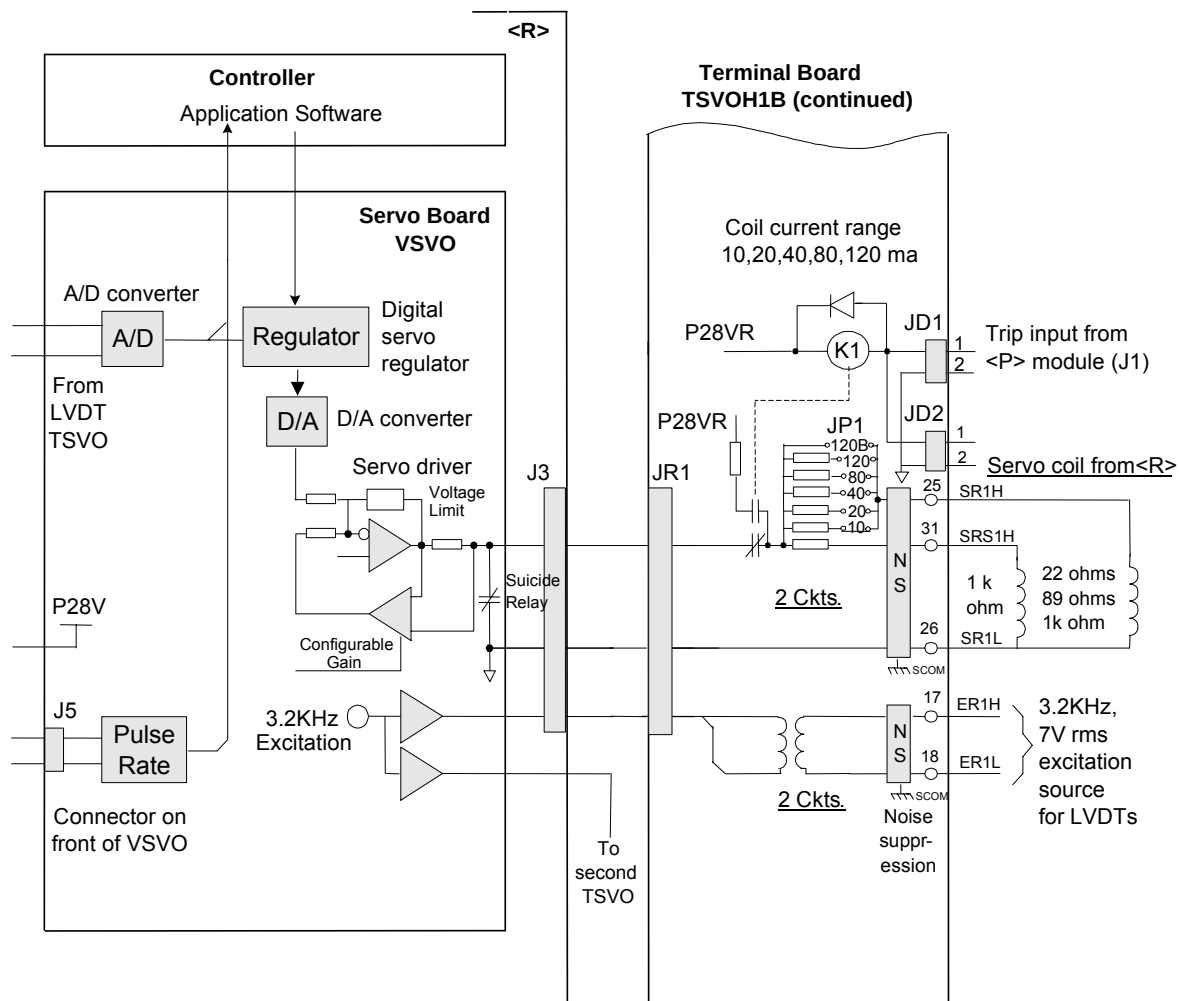


LVDT and Pulse Rate Inputs, Simplex

Each servo output channel can drive one or two-coil servos in simplex applications, or two or three-coil servos in TMR applications. The two-coil TMR applications are for 200# oil gear systems where each of two control modules drive one coil each and the third module interfaces with the servo. Servo cable lengths up to 300 meters (984 feet) are supported with a maximum two-way cable resistance of 15 ohms. Because there are many types of servo coils, a variety of bi-directional current sources are selectable by configuring jumpers.

Another trip override relay, K1, is provided on each terminal board and is driven from the <P> Protection Module. If an emergency overspeed condition is detected in the Protection Module, the K1 relay energizes and disconnects the VSVO servo output from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high, and is functional only with respect to the servo coils driven from <R>.

Note The primary and emergency overspeed systems can trip the hydraulic solenoids independent of this circuit.

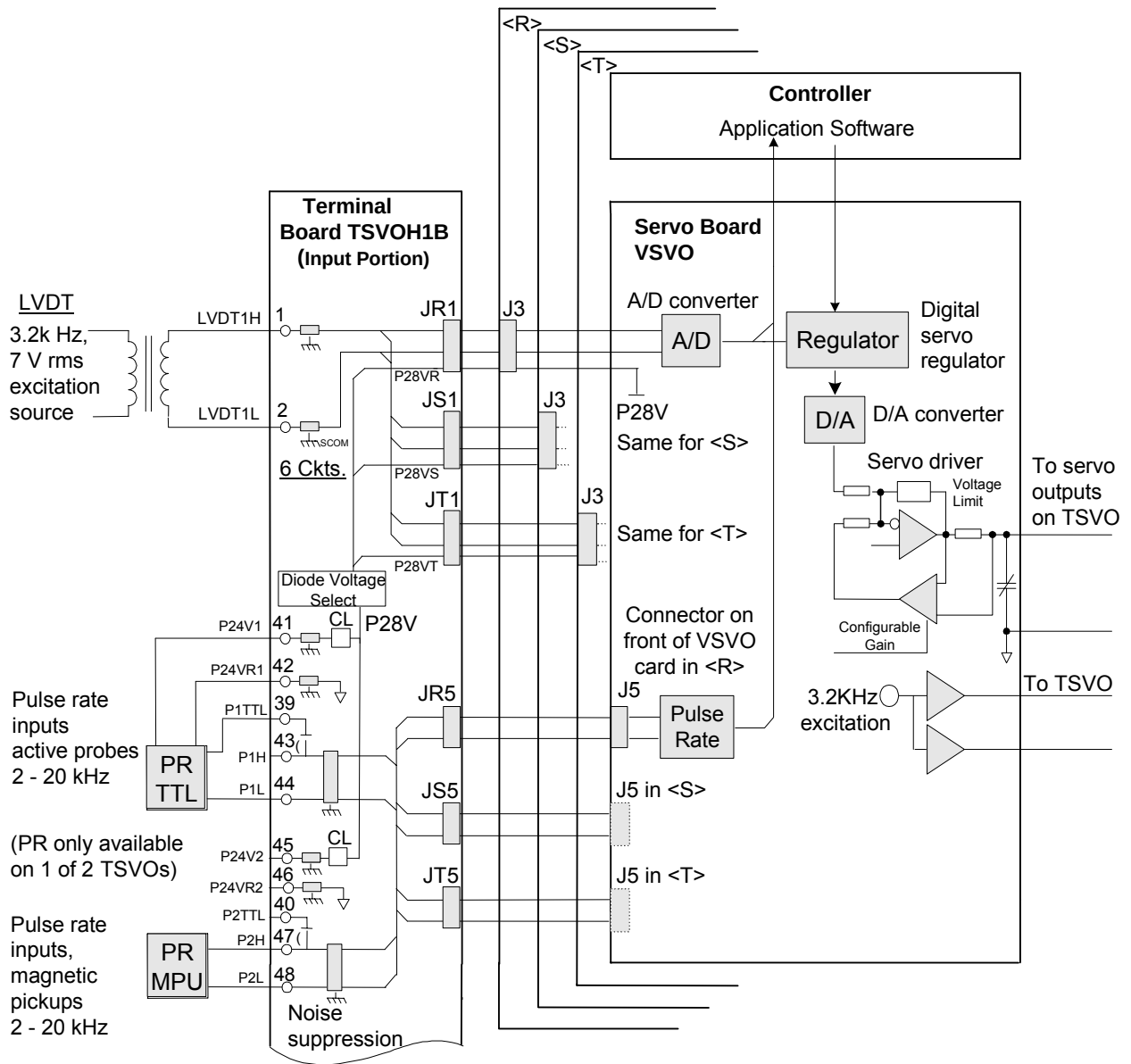


Servo Coil and LVDT Outputs, Simplex (continued) LVDT Outputs, Simplex

TMR Systems

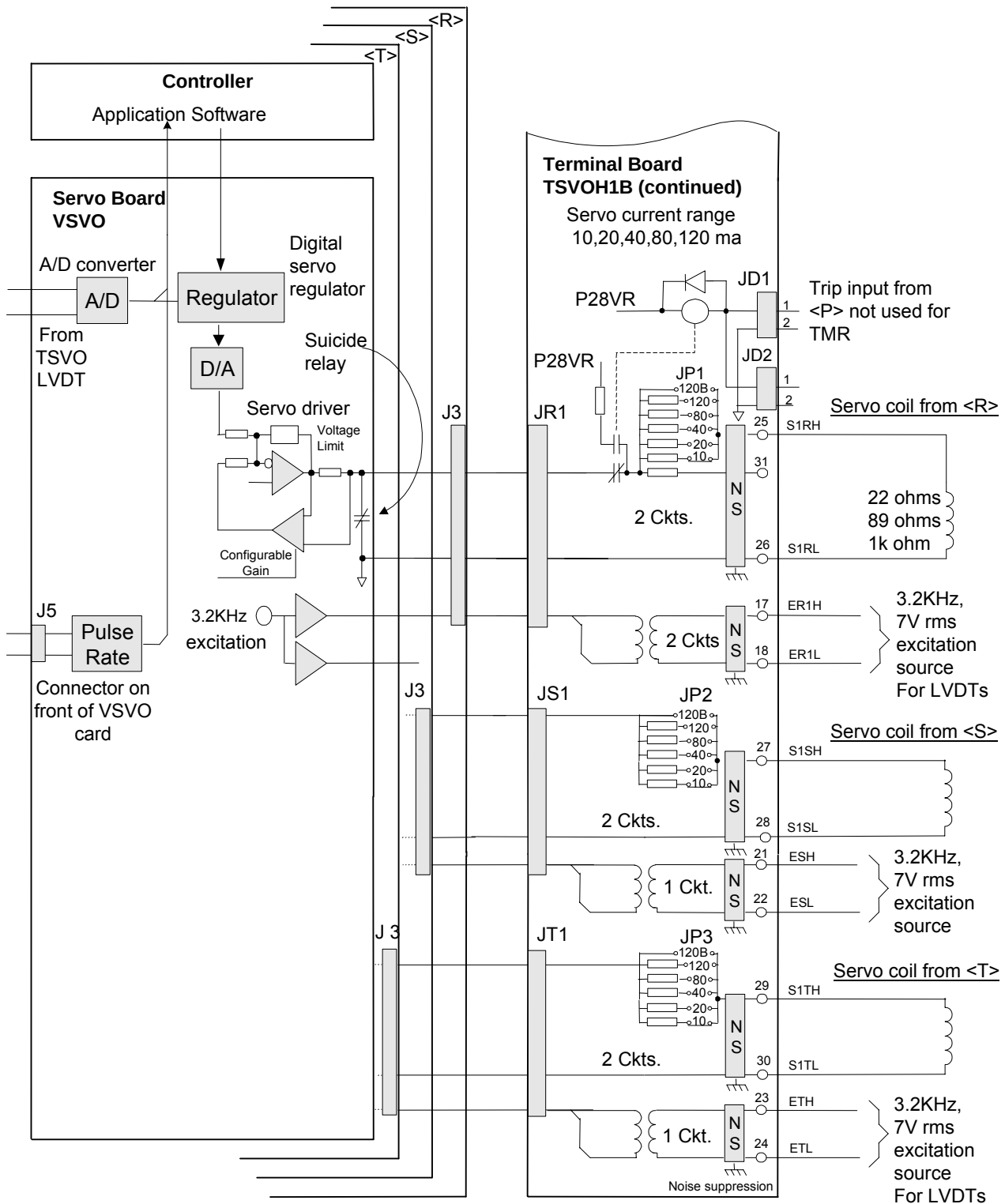
In TMR applications, the LVDT signals on TSVO fan out to three racks through JR1, JS1, and JT1. Three connectors also bring power into TSVO where the three voltages are diode high-selected and current limited to supply 24 V dc to the pulse rate active probes. VSVO circuits for a TMR system are shown in the following figures.

Note Only two pulse rate probes on one TSVO are used.



LVDT and Pulse Rate Inputs, TMR

For TMR systems, each servo channel has connections to three output coils with a range of current ratings up to 120 mA selected by jumper.



Servo Coil Outputs and LVDT Excitation, TMR

The following table defines the standard resistance of servo coils, and their associated internal resistance, selectable with the terminal board jumpers shown in the figure above. In addition to these standard servo coils, non-standard coils can be driven by using a non-standard jumper setting. For example, an 80 mA, 125 Ω coil can be driven by using a jumper setting 120B.

Servo Coil Ratings

Coil Type	Nominal Current	Coil Resistance (Ohms)	Internal Resistance (Ohms)	Application
1	± 10 mA	1,000	180	Simplex and TMR
2	± 20 mA	125	442	Simplex
3	± 40 mA	62	195	Simplex
4	± 40 mA	89	195	TMR
5	± 80 mA	22	115	TMR
6	± 120 mA (A)	40	46	Simplex
7	± 120 mA (B)	75	10	TMR

Note The total resistance is equivalent to the standard setting.

The control valve position is sensed with either a four-wire LVDT or a three-wire linear variable differential reluctance (LVDR). Redundancy implementations for the feedback devices is determined by the application software to allow the maximum flexibility. LVDT/Rs can be mounted up to 300 meters (984 feet) from the turbine control with a maximum two-way cable resistance of 15 Ω .

Each terminal has two LVDT/R excitation sources for simplex applications and four for TMR applications. Excitation voltage is 7 V rms and the frequency is 3.2 kHz with a total harmonic distortion of less than 1% when loaded.

Note The excitation source is isolated from signal common (floating) and is capable of operation at common mode voltages up to 35 V dc, or 35 V rms, 50/60 Hz.

A typical LVDT/R has an output of 0.7 V rms at the zero stroke position of the valve stem, and an output of 3.5 V rms at the designed maximum stroke position (these are reversed in some applications). The LVDT/R input is converted to dc and conditioned with a low pass filter. Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check.

Two pulse rate inputs connect to a single J5 connector on the front of VSVO. This dedicated connection minimizes noise sensitivity on the pulse rate inputs. Both passive magnetic pickups and active pulse rate transducers (TTL type) are supported by the inputs and are interchangeable without configuration. Pulse rate inputs can be located up to 300 meters (984) from the turbine control cabinet, assuming a shielded-pair cable is used with typically 70 nF single ended or 35 nF differential capacitance and 15 Ω resistance.

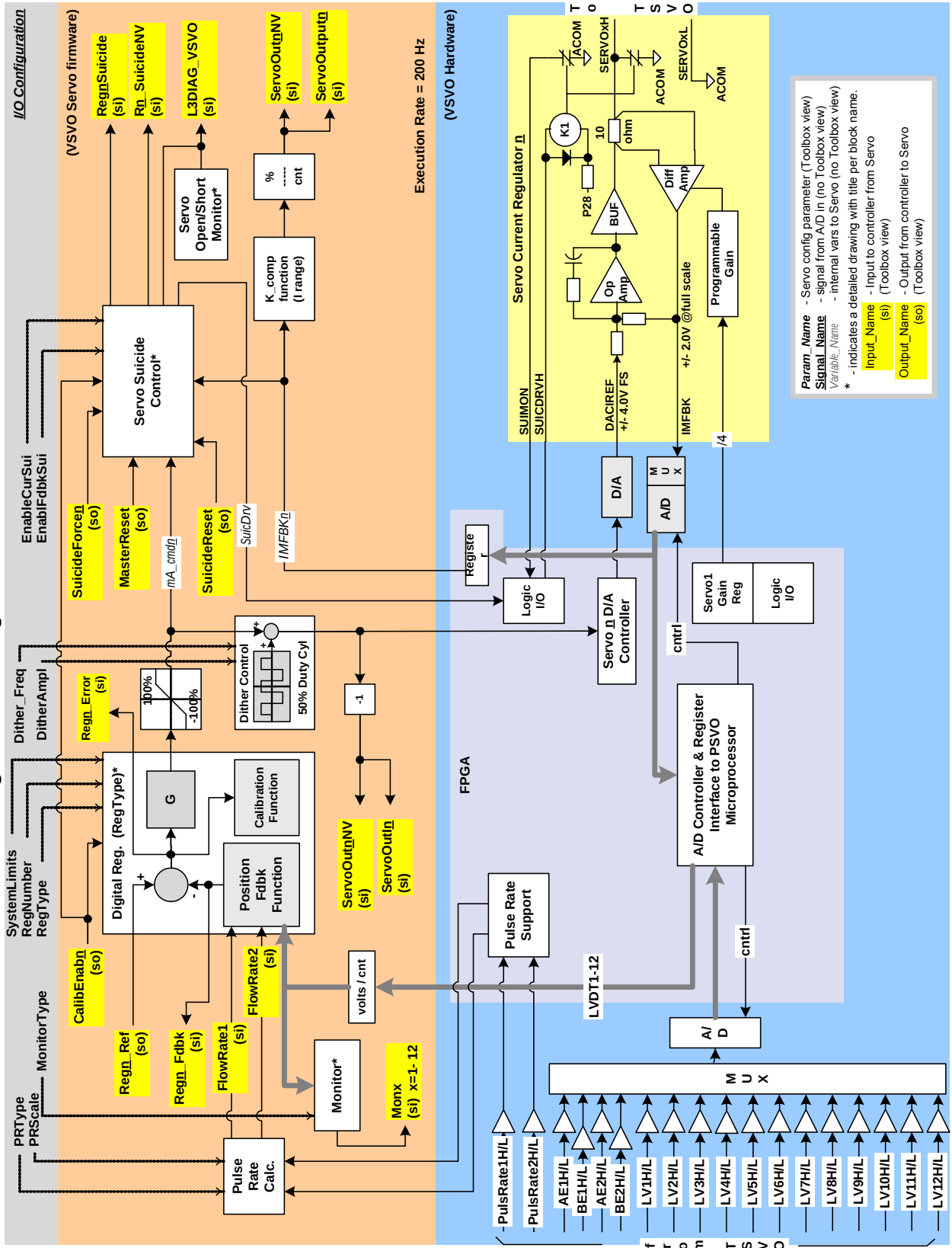
Note The maximum short circuit current is approximately 100 mA with a maximum power output of 1 W.

A frequency range of 2 to 30 kHz can be monitored at a normal sampling rate of either 10 or 20 ms. Magnetic pickups typically have an output resistance of 200 Ω and an inductance of 85 mH excluding cable characteristics. The transducer is a high impedance source, generating energy levels insufficient to cause a spark.

Digital Servo Regulators

The Digital Servo Regulators $n = 1-4$ in the following figure divides the servo regulators into the software and hardware portions of the control loop. The user can choose the LVDT and pulse rate inputs as the servo feedback. The LVDT input is a 3.2 kHz sinusoidal signal with a magnitude proportional to the position of the electro-mechanical valve that is controlled by the servo output. The pulse rate input is TTL-type signal or a periodic signal that triggers a comparator input. The comparator output transitions are counted by an FPGA on VSVO and converted to a flow rate. For LVDT feedbacks, LVDT1 – 12 are scaled and conditioned in the Position Feedback function of the Digital regulator and can also be independently conditioned by a separated Monitoring function. The asterisk after a block name indicates a more detailed drawing exists to better define the block function. All signal space I/O for the VSVO is identified as either *si* for system input (the controller reads the signal space variable from the servo) or *so* for system output (the controller writes the signal space variable to the servo card). Italic text is defined as a configuration parameter that can be changed in the toolbox to redefine the operation of the VSVO. Internal variables, for example *Variable_Name*, are not visible to the user through the toolbox.

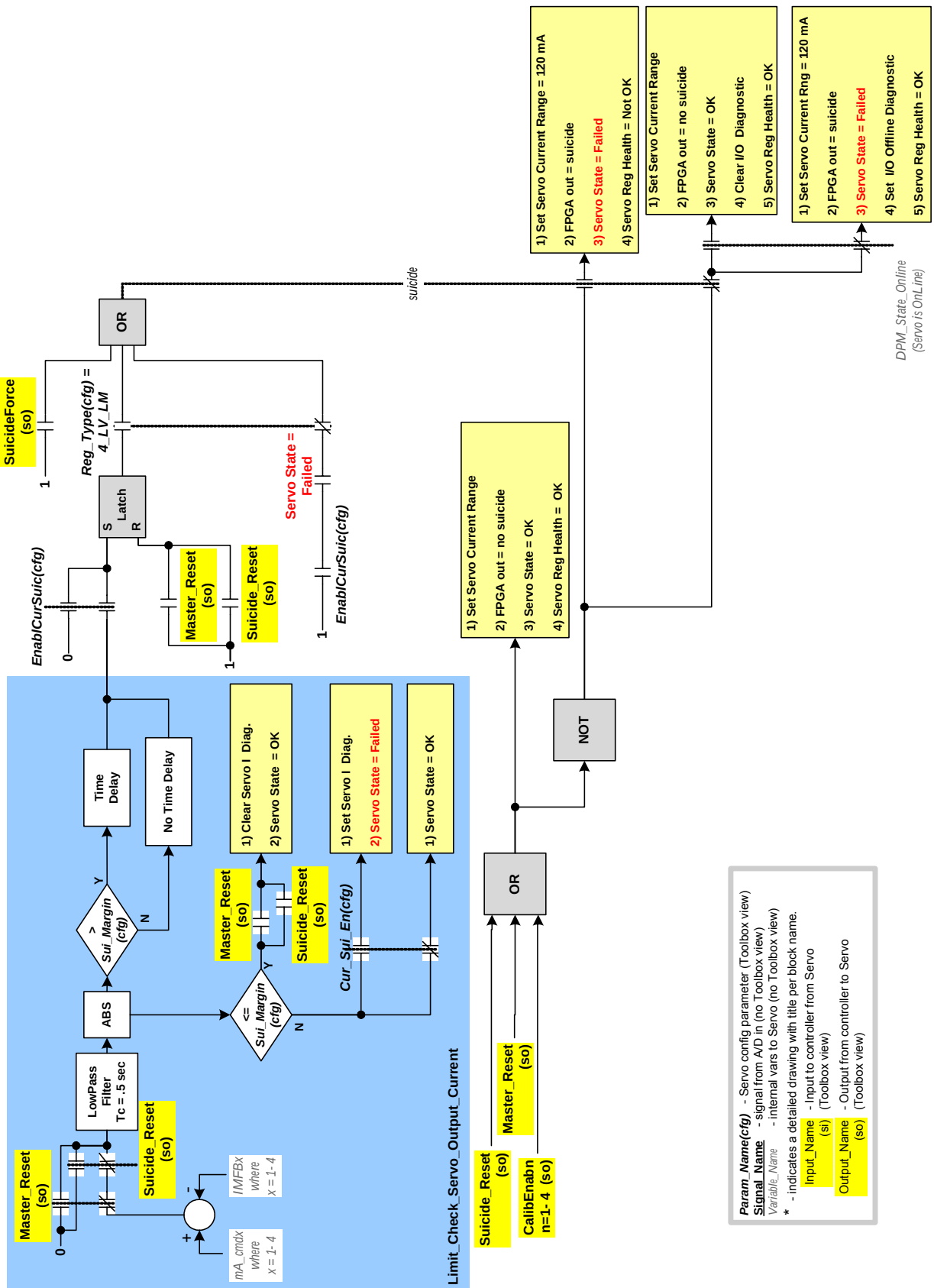
Digital Servo Regulators n = 1 - 4



Servo Suicide Control

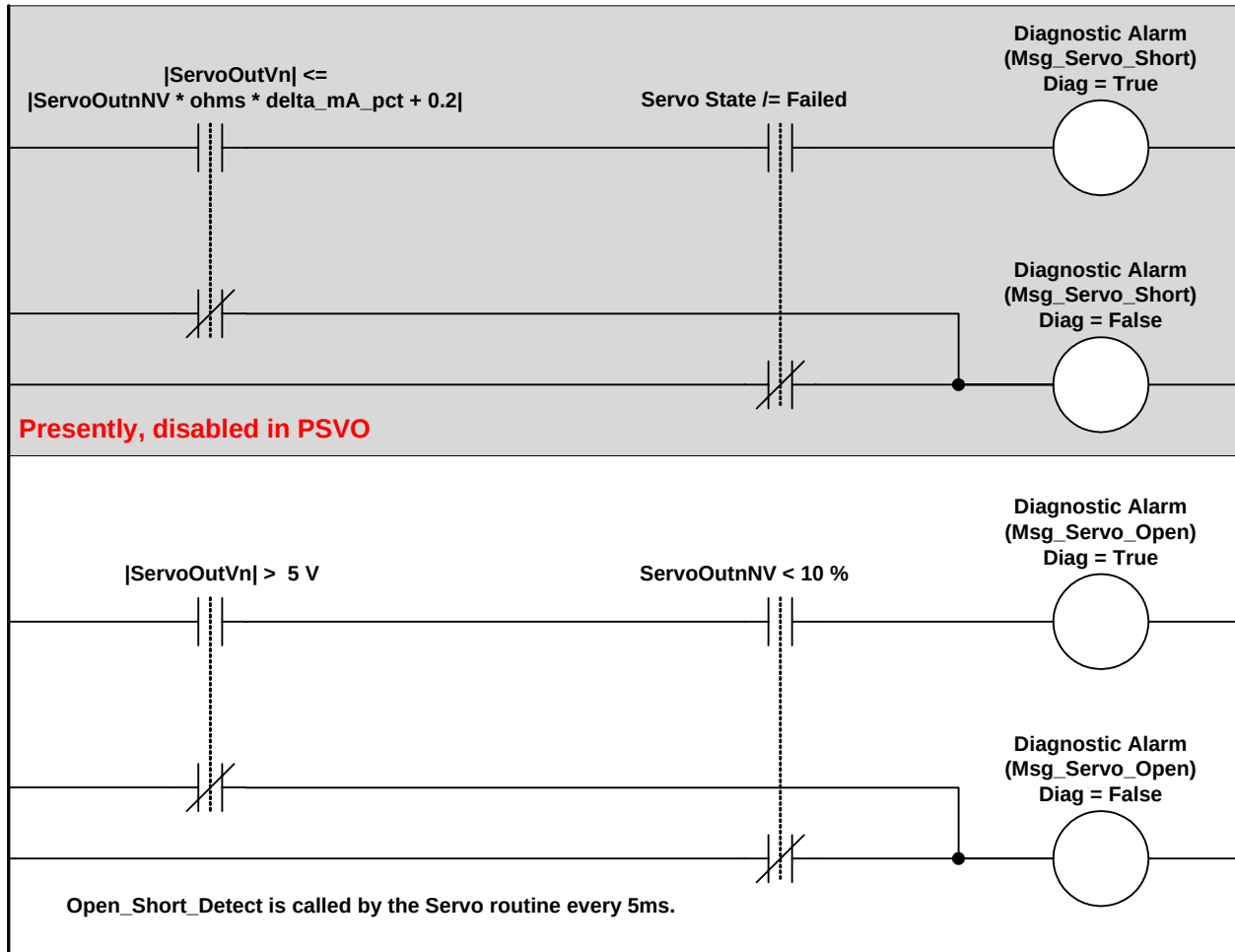
The Servo Suicide Control function compares the absolute value of the filtered servo current error against the configuration parameter value, *Sui_Margin*. This function determines if the hardware servo current regulator has lost control of the current. If the current feedback is not following the current command, a diagnostic is generated and the servo current output is suicided (disabled and put in a safe state).

Servo Suicide Control



Open/Short Detect Function

The servo output open circuit detection function checks for open or broken wires between the terminal screws of the terminal board and the servo coil. If the servo driver voltage is high and no current is flowing, the diagnostic alarm, *Msg_Servo_Open*, is issued.

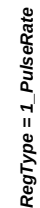


Open Short Detect Function

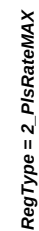
1 PulseRate /2 PulseRateMax

The Digital Servo Regulator is configured as a flow-rate regulator. A pulse signal with a frequency proportional to the flow-rate of the liquid fuel is the feedback for the *1 PulseRate* version of the flow-rate regulator. With the dual input, the larger pulse rate frequency is selected as the feedback for the flow rate regulator. System Limit functions monitor each pulse rate input and are enabled through the configuration parameter, *SysLimxEnabl*. It can latch the signal space limit flags *SysLimxPR1* and/or *SysLimxPR2*.

RegType = 1_PulseRate



RegType = 2_PlsRateMAX



1 LVposition, 2 LVposMIN, 2LVposMAX, 3LVposMID

The following LVDT feedback configurations are provided for the servo value position loop:

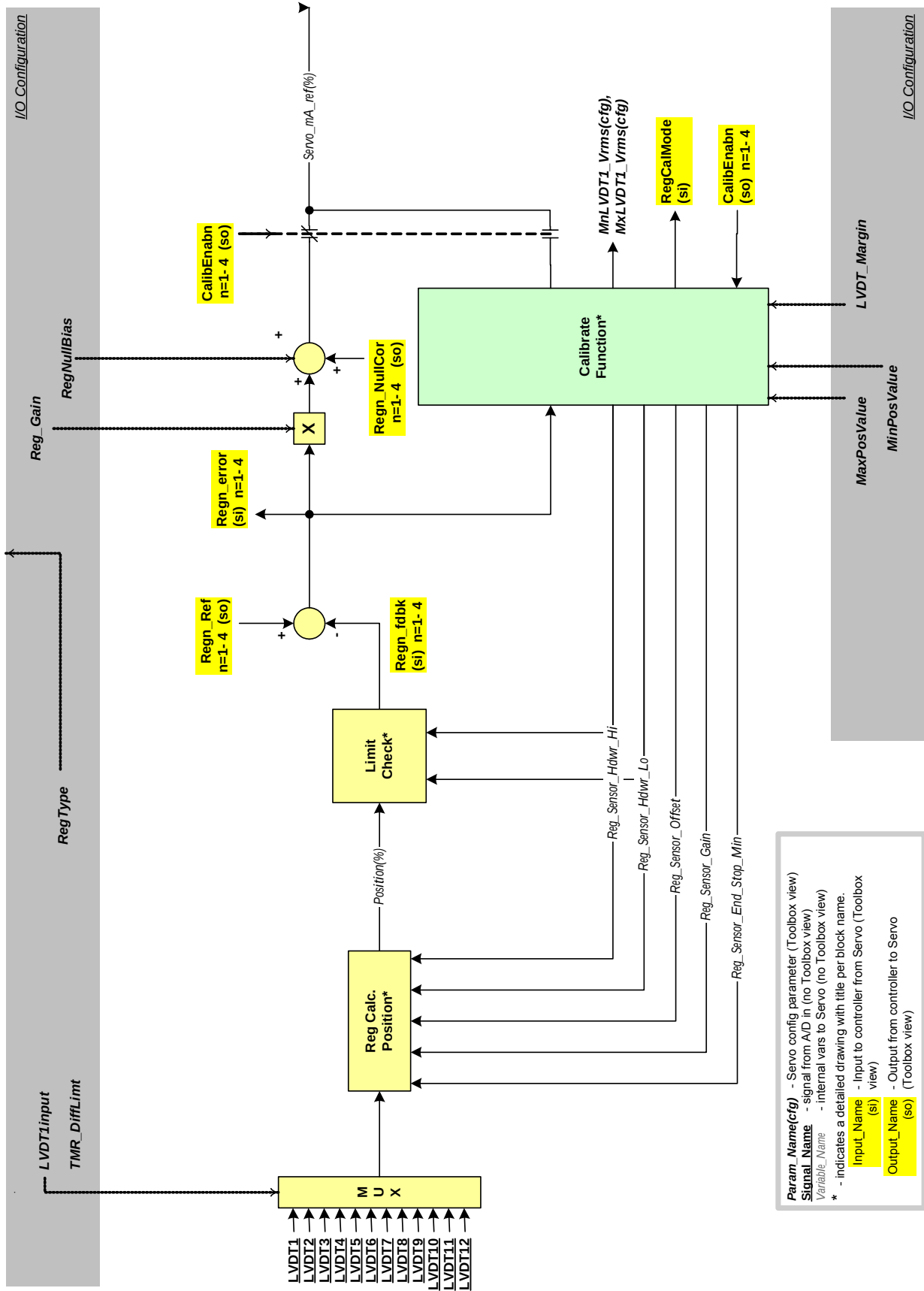
- 1_LVposition – one LVDT signal is used as the position feedback.
- 2_LVposMIN – the minimum of two LVDT signals is selected as the position feedback.
- 2_LVposMAX – the maximum of two LVDT signals is selected as the position feedback.
- 3_LVposMID – the median of three LVDT signals is selected as position feedback.

The LVDT feedback signals are bounded and scaled using the Calibration function. The Calibration function uses the following configuration parameters: position at the minimum end stop in engineering units (EU), *MinPOSvalue*, and the position at the maximum end stop in EU, *MaxPOSvalue*. In the calibration mode the LVDT sensors are forced into the minimum and maximum positions. The feedback voltages, *MnLVDTx_Vrms* and *MxLVDTx_Vrm,s* are recorded for each of the LVDT feedbacks used. From these values, the internal constants *Reg_Sensor_Hdwr_Hi*, *Reg_Sensor_Hdwr_Lo*, *Reg_Sensor_Offset*, *Reg_Sensor_Gain*, and *Reg_Sensor_End_Stop_Min* are calculated. These internal constants are used by the Regulator Calculation Position function.

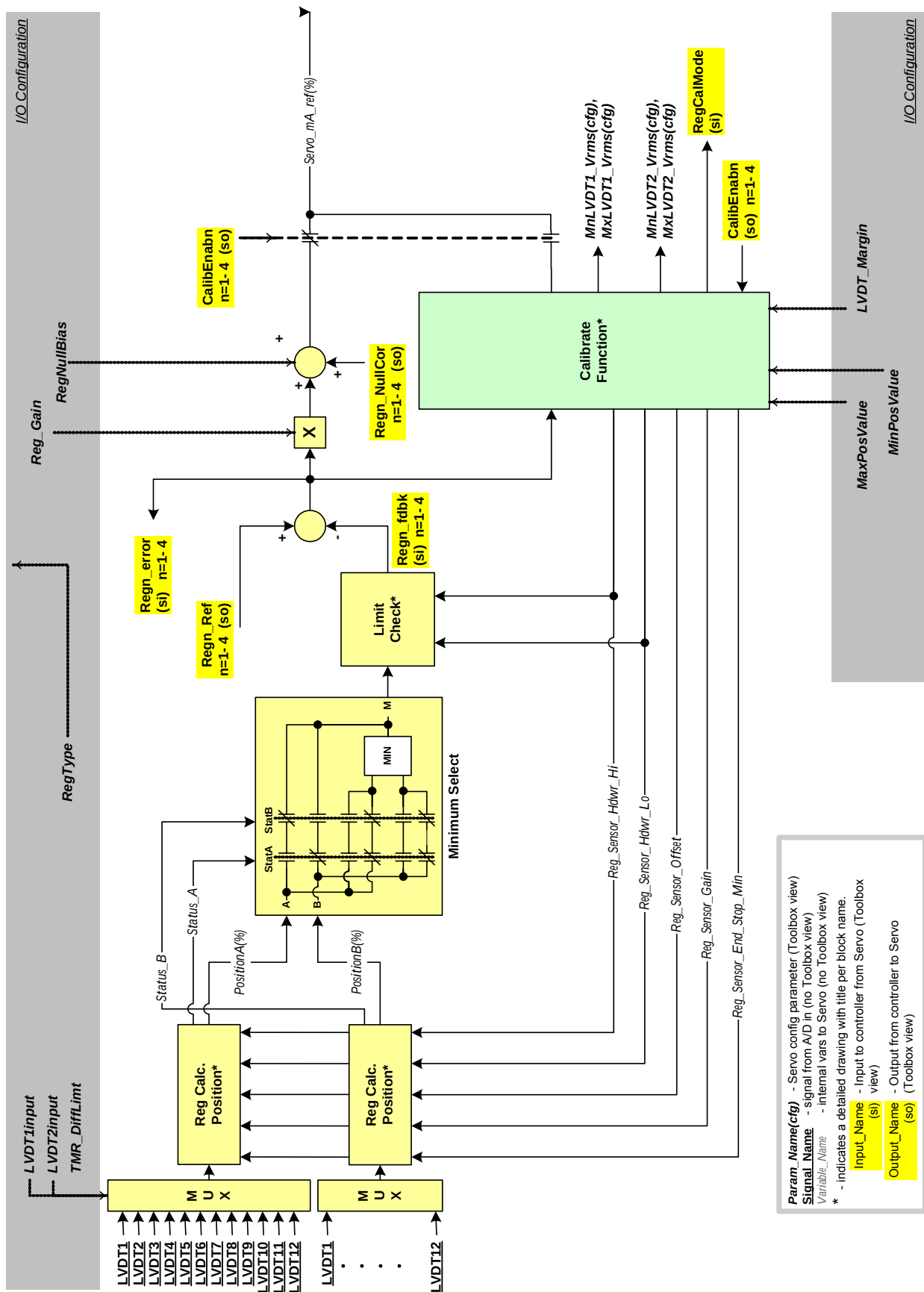
The Regulator Calculation Position function performs an input boundary check that makes sure the input signal is between the values, *Reg_Sensor_Hdwr_Hi* and *Reg_Sensor_Hdwr_Lo*. If the feedback input is out of range a diagnostic alarm is generated. The scaling from volts_rms to position feedback in EU is calculated next. A limit check is then performed on the selected feedback.

Digital Servo Regulator

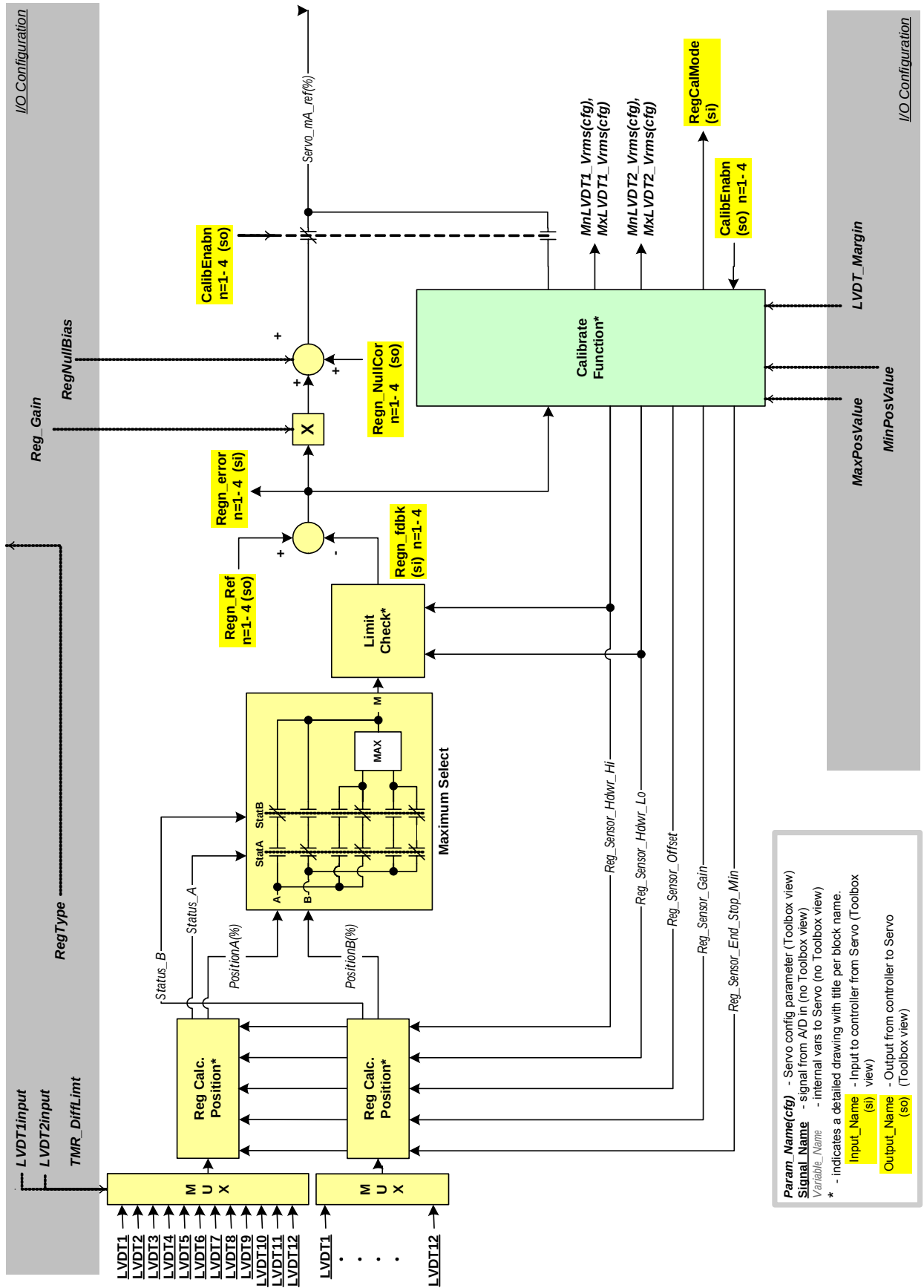
RegType = 1_LVposition



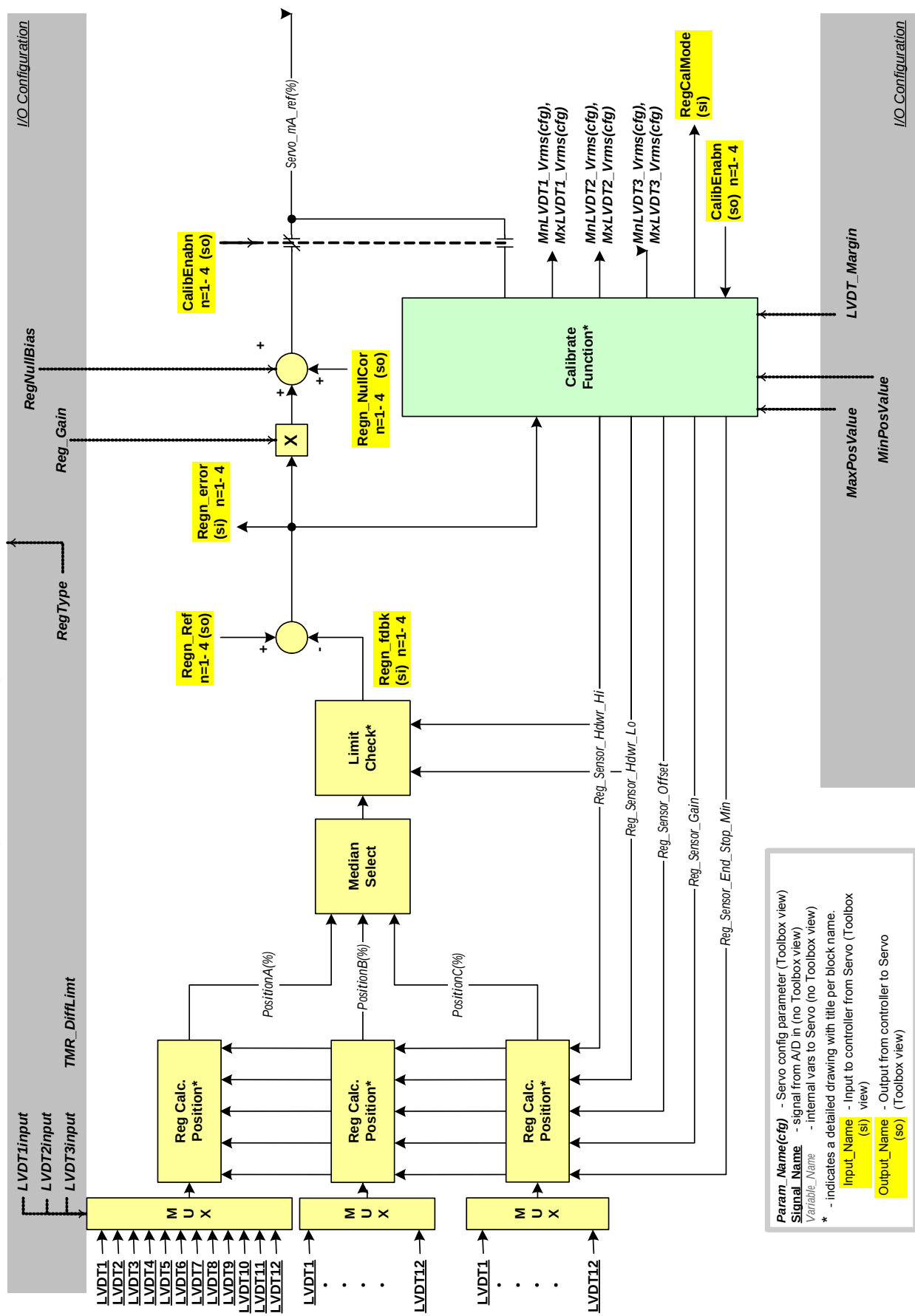
Digital Servo Regulator $\text{RegType} = 2\_LVposMIN$



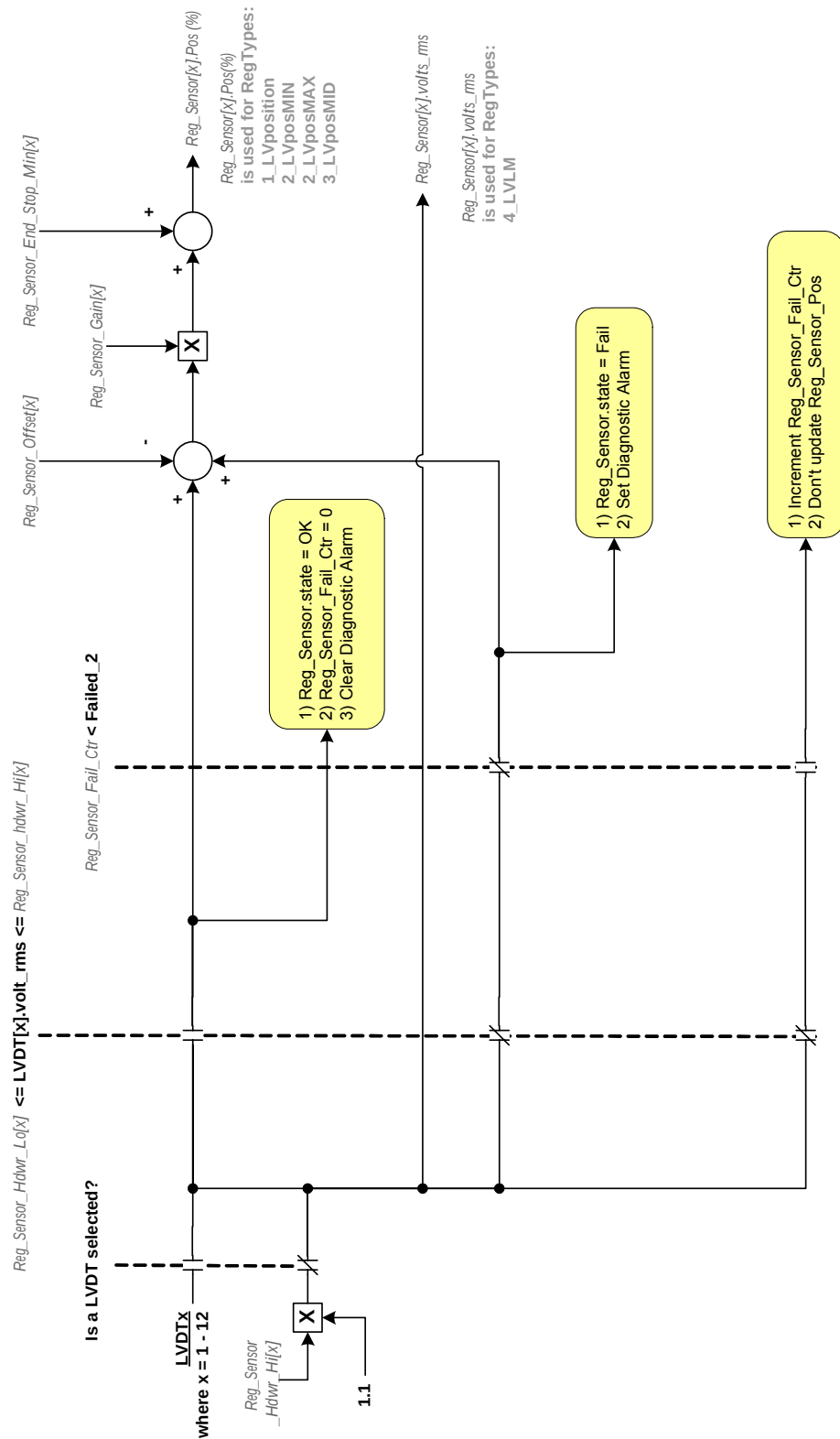
Digital Servo Regulator $RegType = 2\_LVposMAX$



Digital Servo Regulator



Reg_Calc_Position

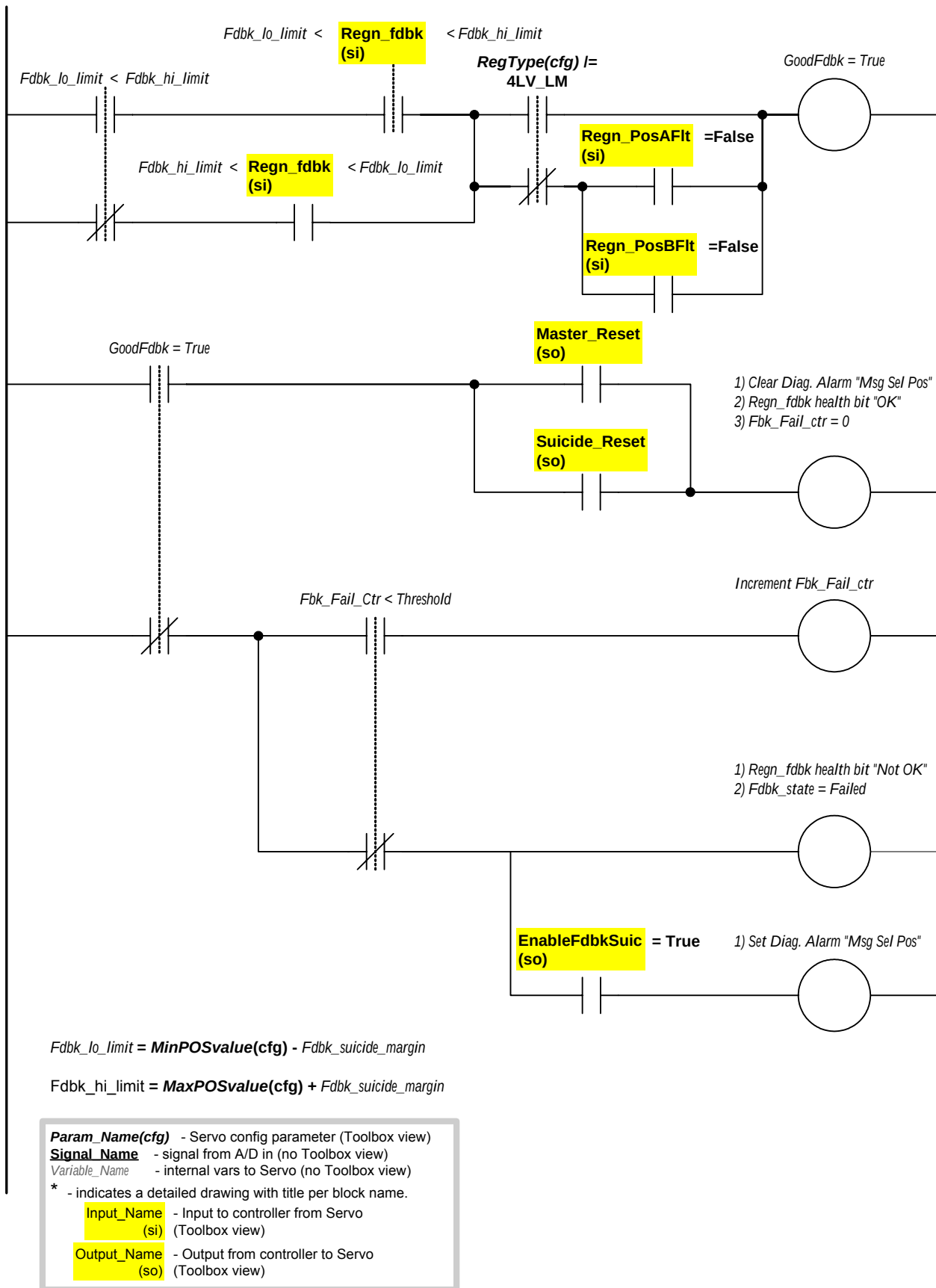


$Reg\_Sensor\_Hdwr\_Lo[x] = MnLVDT\_Vrms(cfg) - (MxLVDT\_Vrms(cfg) - MnLVDT\_Vrms(cfg)) * LVDT\_Margin(cfg) / 100$ before calibration.

$Reg\_Sensor\_Hdwr\_Hi[x] = MxLVDT\_Vrms(cfg) + (MxLVDT\_Vrms(cfg) - MnLVDT\_Vrms(cfg)) * LVDT\_Margin(cfg) / 100$ before calibration.

Param_Name(cfg) - Servo config parameter (Toolbox view)
Signal_Name - signal from A/D in (no Toolbox view)
Variable_Name - internal vars to Servo (no Toolbox view)

Limit Check Function



4 LV_LM

The 4_LV_LM Digital Servo regulator uses four LVDT inputs to calculate the single position feedback required for the servo position loop. The Regulator Calculation Position performs the boundary check for the LVDT input signals. The scaling from volts_rms to position in EU is not calculated, but the volts_rms value for each of the LVDT feedbacks is calculated. The ratio of $(A - B) / (A + B)$ is performed on the LVDT input pairs and scaling is calculated using the input from the Calibration function.

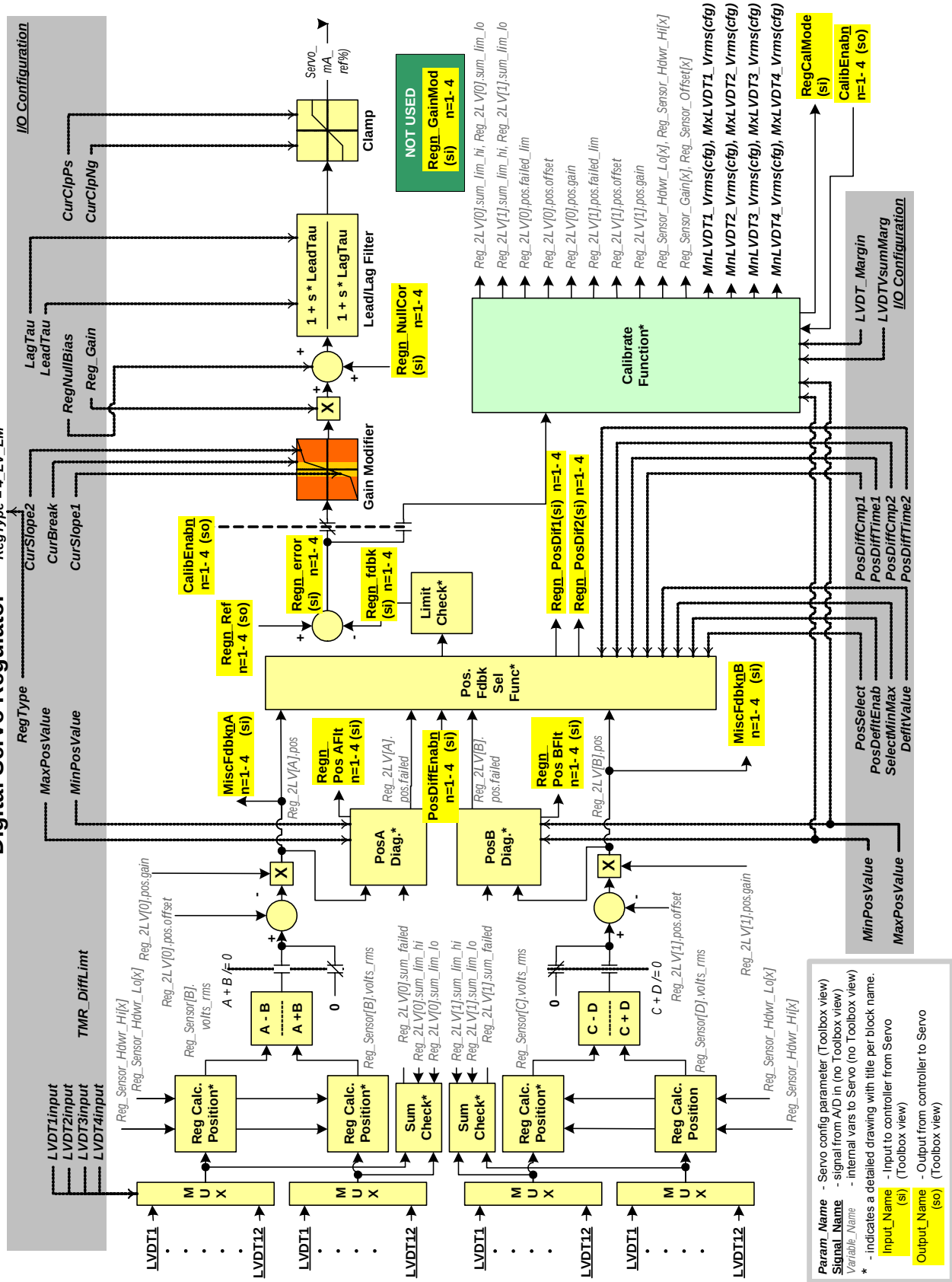
The internal variables, Reg_2LV[A].pos, PosA and Reg_2LV[B].pos, PosB are checked against the configuration parameter limits, MinPOSvalue and MaxPOSvalue in the Position A & B Diagnostic function. Results from PosA, PosB, and the diagnostic Booleans feed the Position Feedback Selection function. Refer to the *Position Feedback Selection* block diagram to understand the details of the function.

Other differences in the LM servo regulator are the following:

- Gain Modifier function
- Lead/Lag filter on the position error
- Configurable servo position error output clamp

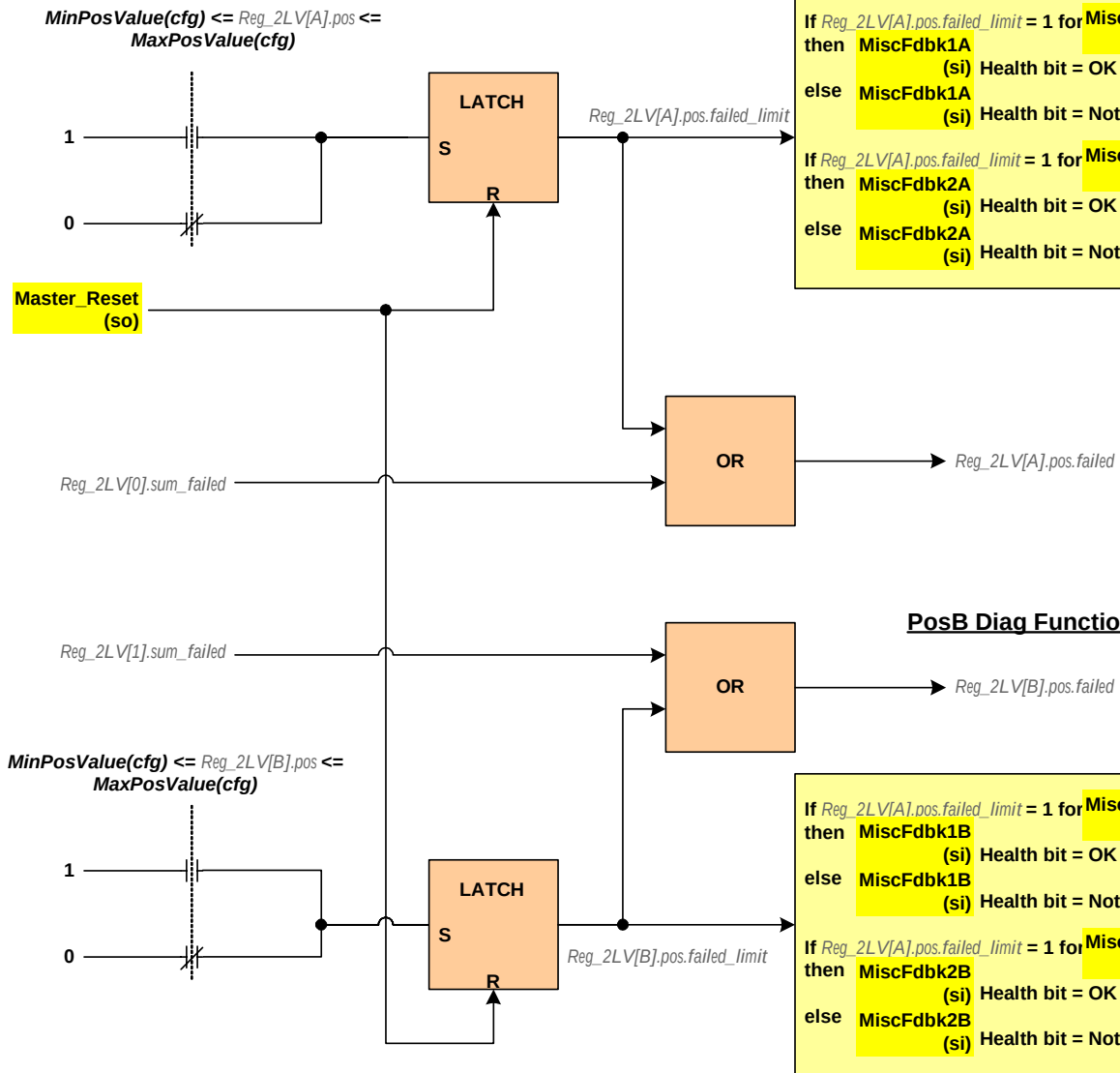
Digital Servo Regulator

RegType = 4 LV_LM



Position A & B Diagnostic Function

PosA Diag Function

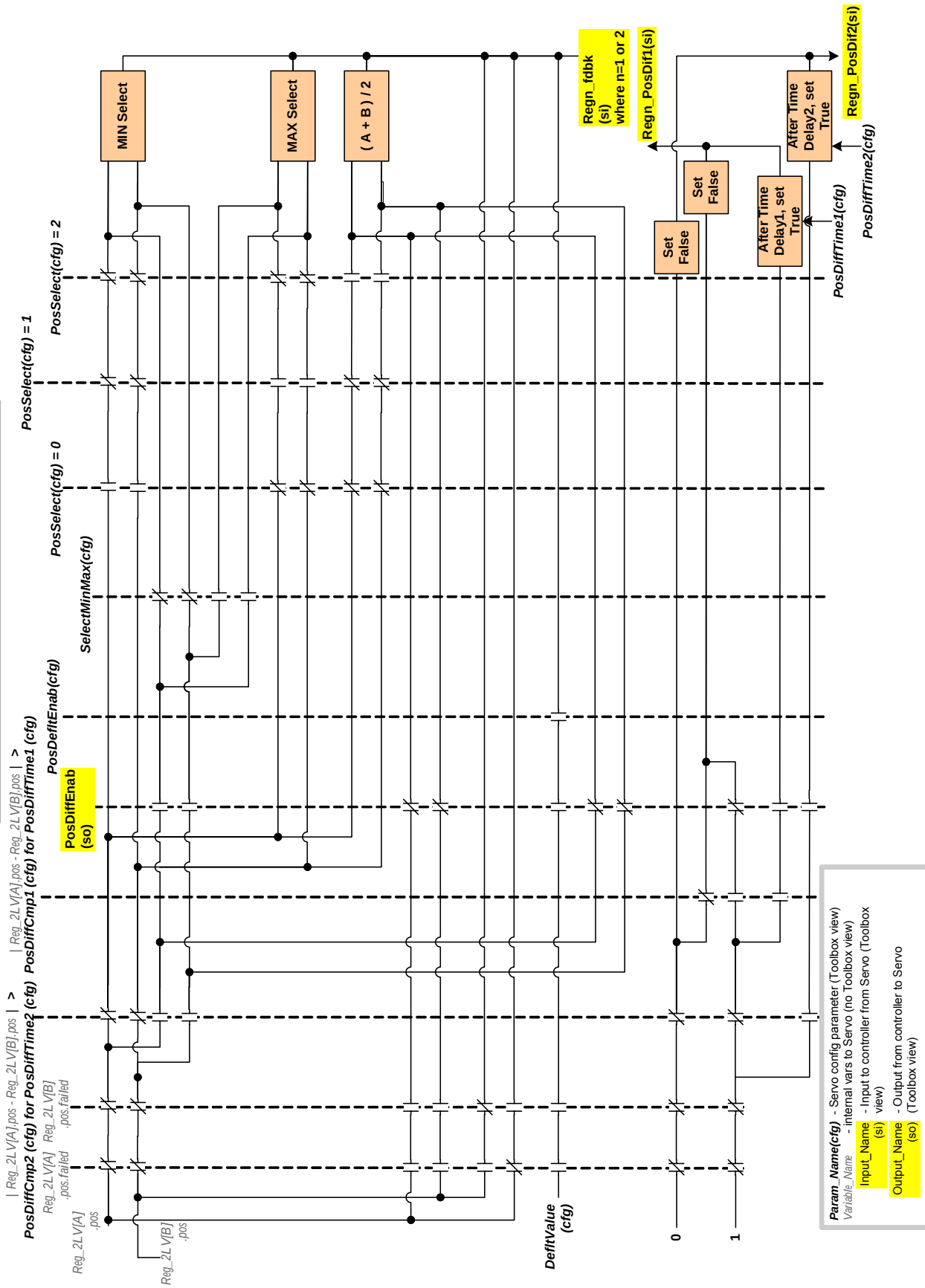


Param_Name(cfg) - Servo config parameter (Toolbox view)
Signal_Name - signal from A/D in (no Toolbox view)
Variable_Name - internal vars to Servo (no Toolbox view)
 * - indicates a detailed drawing with title per block name.

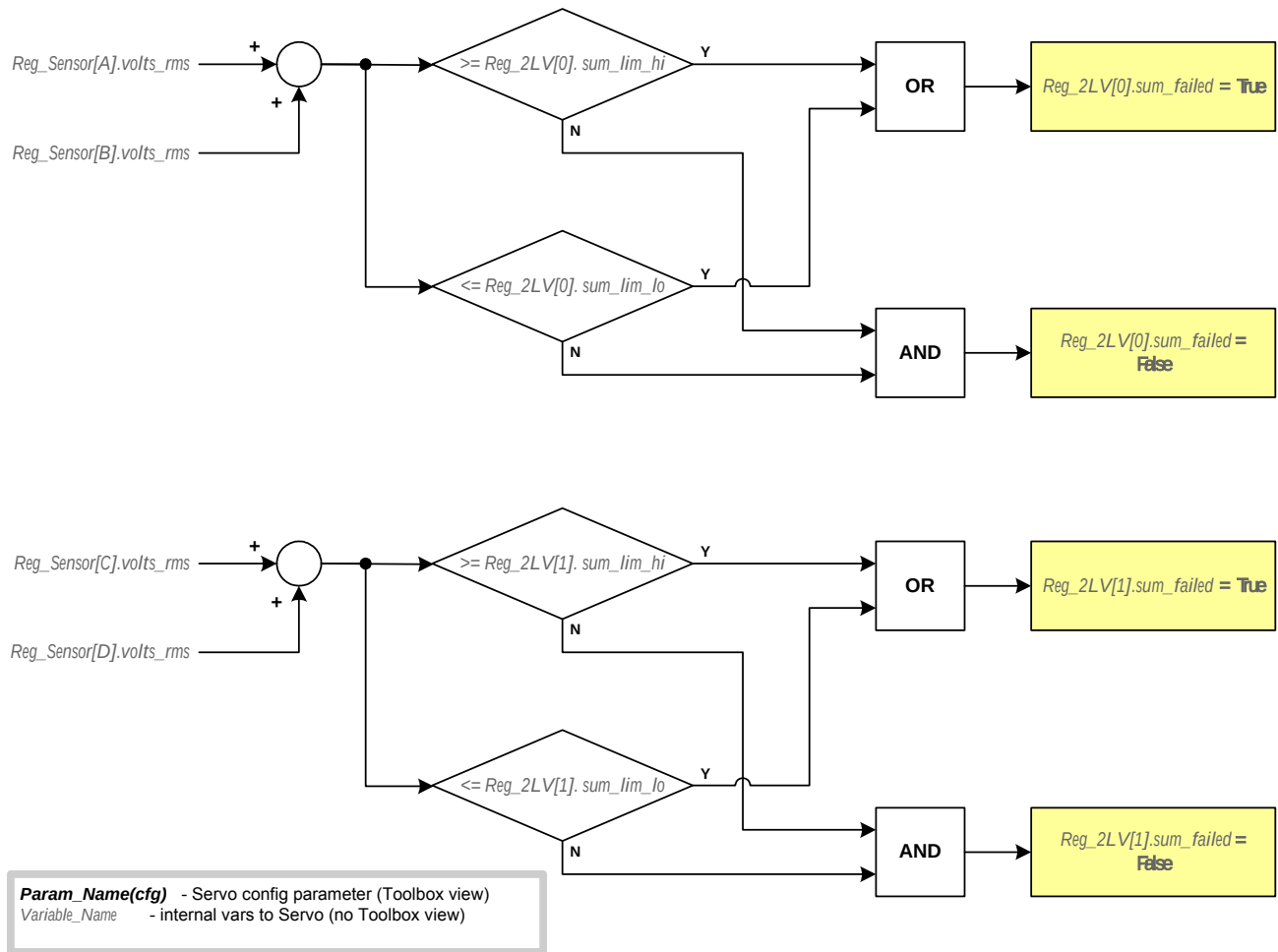
Input_Name - Input to controller from Servo (Toolbox view)
 (si)

Output_Name - Output from controller to Servo (Toolbox view)
 (so)

Position Feedback Selection Function



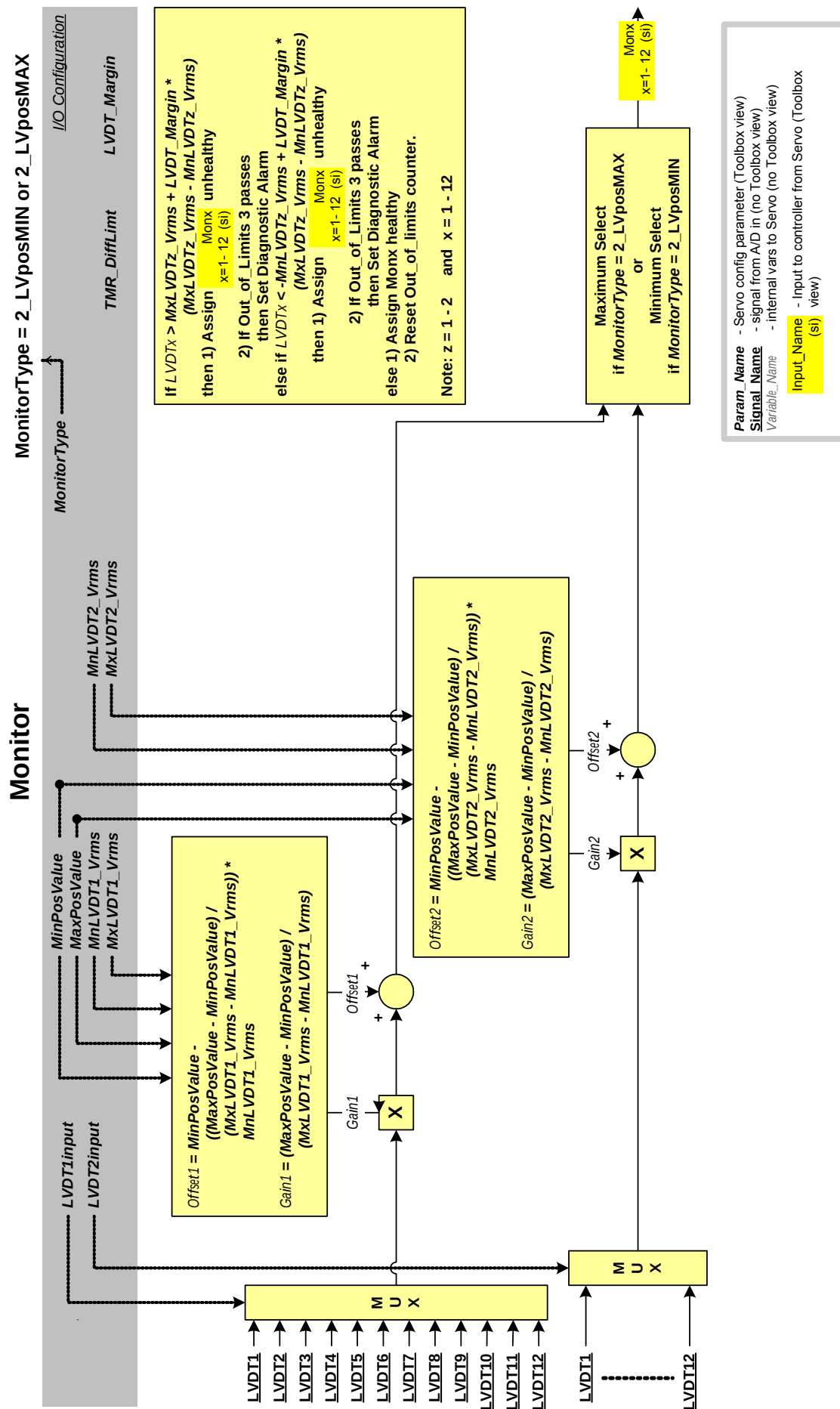
Sum Check Calc



Monitors - 1 LVposition, 2 LVposMIN, 2LVposMAX, 3LVposMID

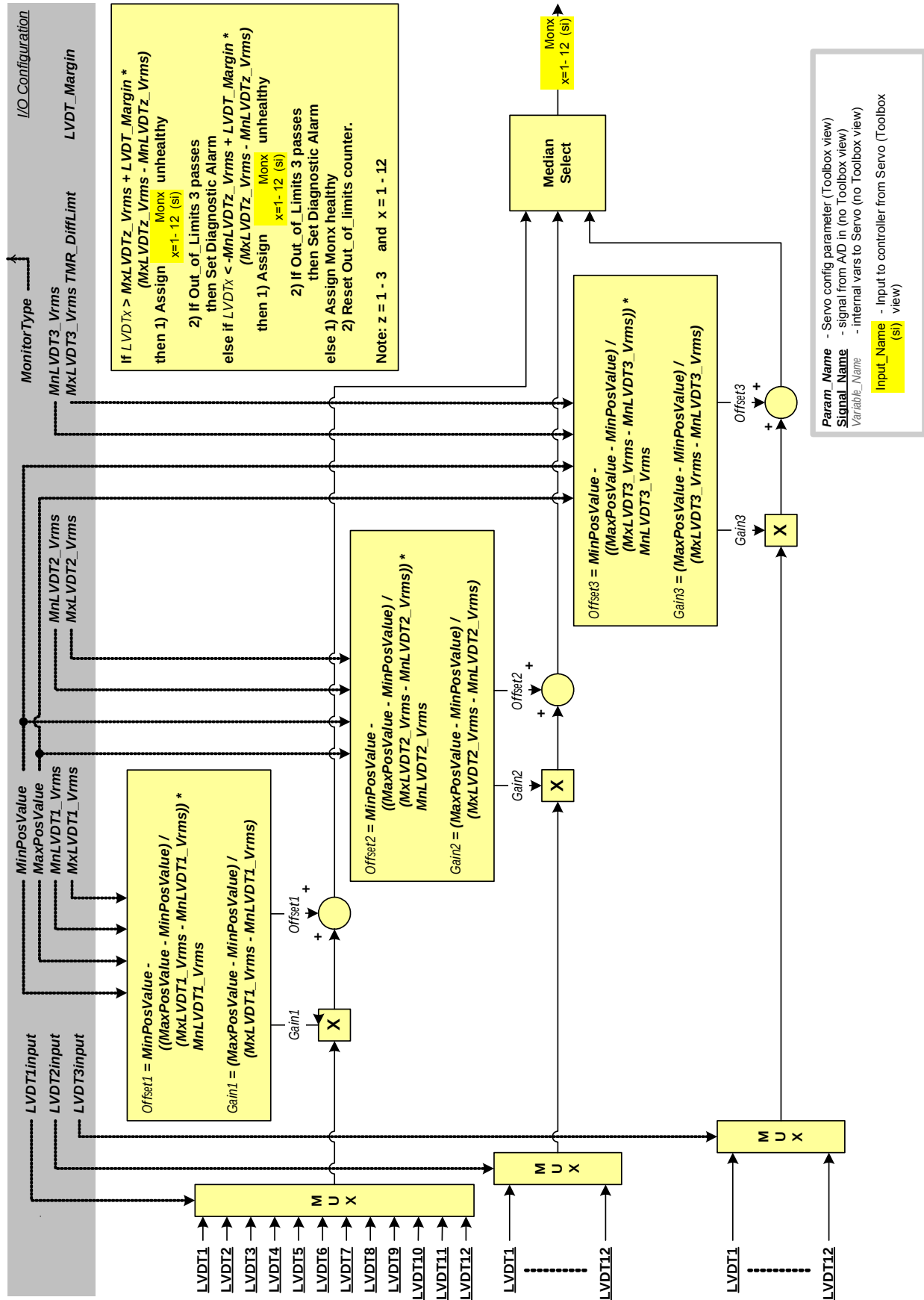
The following Monitor configurations are available:

- 1_LVposition – one LVDT signal is used as the position feedback.
- 2_LVposMIN – the minimum of two LVDT signals is selected as the position feedback.
- 2_LVposMAX – the maximum of two LVDT signals is selected as the position feedback.
- 3_LVposMID – the median of three LVDT signals is selected as the position feedback.



Monitor

MonitorType = 3 LVposMID



Specifications

Item	Specification
Number of inputs (per TSVO)	6 LVDT windings 2 pulse rate signals (total of 2 per VSVO) External trip signal
Number of outputs (per TSVO)	2 servo valves (total of 4 per VSVO board) 4 excitation sources for LVDTs 2 excitation sources for pulse rate transducers
Internal sample rate	200 Hz
Power supply voltage	Nominal 24 V dc
LVDT accuracy	1% with 14-bit resolution
LVDT input filter	Low pass filter with 3 down breaks at 50 rad/sec $\pm 15\%$
LVDT common mode rejection	CMR is 1 V, 60 dB at 50/60 Hz
LVDT excitation output	Frequency of 3.2 ± 0.2 kHz Voltage of 7.00 ± 0.14 V rms
Pulse rate accuracy	0.05% of reading with 16-bit resolution at 50 Hz frame rate Noise of acceleration measurement is less than ± 50 Hz/sec for a 10,000 Hz signal being read at 10 ms
Pulse rate input	Minimum signal for proper measurement at 2 Hz is 70 mVpk, and at 12 kHz is 827 mVpk.
Magnetic PR pickup signal	Generates 150 V p-p into 60 k Ω
Active PR Pickup Signal	Generates 5 to 27 V p-p into 60 k Ω
Servo valve output accuracy	2% with 12-bit resolution Dither amplitude and frequency adjustable
Fault detection	Suicide servo outputs initiated by: Servo current out of limits or not responding Regulator feedback signal out of limits

Diagnostics

Three LEDs at the top of the VSVO front panel show status information. The normal RUN condition is a flashing green, and FAIL is solid red. The third LED is STATUS and is normally off but displays a steady orange if an alarm condition exists on the board. Diagnostic checks include the following:

- The output servo current is out of limits or not responding, which creates a fault.
- The regulator feedback (LVDT) signal is out of limits. A fault is created and if the associated regulator has two sensors, the bad sensor is removed from the feedback calculation and the good sensor is used.
- The servo has suicided. This creates a fault.
- The A/D converter calibration voltage is out of limits and a default value is being used.
- The LVDT excitation voltage is out of range. A fault is created
- The input signal varies from the voted value by more than the TMR differential limit. This causes a fault to be created indicating a problem with this sensor input.
- If any one of the above signals go unhealthy a composite diagnostic alarm, L#DIAG_VSVO, occurs. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and reset with the RESET_DIA signal if they go healthy.
- Connectors JR1, JS1, JT1 on the terminal board have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location. When the chip is read by VSVO and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Parameter	Description	Choices
Configuration		
System Limits	Select system limits	Enable, disable
Regulator 1	LVDT/R calibration	Online LVDT calibration, yes/no
RegType	Algorithm used in the regulator	Unused 1_PulseRate 2_PlsRateMAX 1_LVposition 2_LVposMIN 2_LVposMAX 3_LVposMID 2_LvpilotCyl 4_LVp/cylMAX 4_LV_LM no_fbK
RegGain	Position loop gain in (%current/%position)	-200 to 200
RegNullBias	Null bias in % current, balances servo spring force	-100 to 100
DitherAmpl	Dither in % current (minimizes hysteresis)	Dither amp: 0 to 10
MinPOSvalue	Position at Min End Stop in engineering units.	-15 to 150
MaxPOSvalue	Position at Max End Stop in engineering units.	-15 to 150
MnLVDT1_Vrms	LVDT1_Vrms at Min End Stop (Normally set by the Calibration function)	0 to 7.1
MxLVDT1_Vrms	LVDT1_Vrms at Max End Stop (Normally set by the Calibration function)	0 to 7.1
:		
MnLVDT4_Vrms	LVDT4_Vrms at Min End Stop (Normally set by the Calibration function)	0 to 7.1
MxLVDT4_Vrms	LVDT4_Vrms at Max End Stop (Normally set by the Calibration function)	0 to 7.1

Parameter	Description	Choices
LVDT_Margin	Used in the calibration function to calculate the internal variables, Reg_Sensor_Hdwr_Lo and Reg_Sensor_Hdwr_Hi for LVDT sensor check.	0 to 7.1
TMR_DiffLimt	Difference limit off voted pulse inputs (EU)	0 to 12000
Monitor 1		
Monitor type	Monitor algorithm	Unused 1_LVposition 2_LVposMIN 2_LVposMAX 3_LVposMID
MinPOSvalue	Position at Min End Stop in engineering units.	-15 to 150
MaxPOSvalue	Position at Max End Stop in engineering units.	-15 to 150
MnLVDT1_Vrms	LVDT1_Vrms at Min End Stop (not set by the Calibration function)	0 to 7.1
MxLVDT1_Vrms	LVDT1_Vrms at Max End Stop (not set by the Calibration function)	0 to 7.1
:		
MnLVDT4_Vrms	LVDT4_Vrms at Min End Stop (not set by the Calibration function)	0 to 7.1
MxLVDT4_Vrms	LVDT4_Vrms at Max End Stop (not set by the Calibration function)	0 to 7.1
LVDT_Margin	Used in the calibration function to calculate the internal variables, Reg_Sensor_Hdwr_Lo and Reg_Sensor_Hdwr_Hi for LVDT sensor check done by the Monitor function.	0 to 7.1
TMR_DiffLimt	Difference limit off voted pulse inputs (EU)	0 to 12000
J3:IS200TSVOH1A	Terminal board 1 connected to VSVO through J3	Connected, not connected
Servo Output1	Measured output current in percent – Board point	Point edit (input FLOAT)
Reg Number	Identify regulator number	Unused, Reg1, Reg2, Reg3, Reg4
Servo_MA_Out	Select current output for coil windings	10, 20, 40, 80, 120 mA
EnableCurSuic	Select Suicide function based on current	Enable, disable
Curr_Suicide	Percent current error to initiate suicide	0 to 100% (output current error)
EnablFbkSuic	Select Suicide function based on position feedback	Enable, disable
Fdbk_Suicide	Percent position error to initiate suicide	0 to 100% (actuator position error)
Servo Output2	Measured output current in percent - Board point	Point edit (input FLOAT)
J4:IS200TSVOH1A	Terminal Board 2 connected to VSVO via J4	Connected, not connected
Servo Output3	Servo current output wired to valve - Board point	Point edit (input FLOAT)
Servo Output4	Servo current output wired to valve - Board point	Point edit (input FLOAT)
J5:IS00TSVOH1A	Pulse Rate inputs cabled to J5 connector	Connected, not connected
FlowRate1	Pulse rate input selected - Board point	Point edit (input FLOAT)
PRTtype	Select speed or flow type signal	Unused, Speed, Flow, Speed_High, Speed_LM
PRScale	Convert Hz to engineering units	0 to 1,000
SysLim1Enabl	Select system limit	Enable, disable
SysLim1Latch	Select whether alarm will latch	Latch, not latch
SysLim1Type	Select type of alarm initiation	>= or <=
SysLimit	Select alarm level in GPM or RPM	0 to 12,000
SystemLim2	Same as above	Same as above
TMR_DiffLimt	Difference limit off voted pulse inputs (EU)	0 to 12,000
FlowRate2	Pulse rate input selected - Board point (as above)	Point edit (input FLOAT)

Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VSVOR	Board diagnostic	Input	BIT
L3DIAG_VSVOS	Board diagnostic	Input	BIT
L3DIAG_VSVOT	Board diagnostic	Input	BIT
R1_SuicideNVR	Regulator 1 Suicide relay status, non-voted for VSVO-R	Input	BIT
R1_SuicideNVS	Regulator 1 Suicide relay status, non-voted for VSVO-S	Input	BIT
R1_SuicideNVT	Regulator 1 Suicide relay status, non-voted for VSVO-T	Input	BIT
R2_SuicideNVR	Regulator 2 Suicide relay status, non-voted for VSVO-R	Input	BIT
R2_SuicideNVS	Regulator 2 Suicide relay status, non-voted for VSVO-S	Input	BIT
R2_SuicideNVT	Regulator 2 Suicide relay status, non-voted for VSVO-T	Input	BIT
R3_SuicideNVR	Regulator 3 Suicide relay status, non-voted for VSVO-R	Input	BIT
R3_SuicideNVS	Regulator 3 Suicide relay status, non-voted for VSVO-S	Input	BIT
R3_SuicideNVT	Regulator 3 Suicide relay status, non-voted for VSVO-T	Input	BIT
R4_SuicideNVR	Regulator 4 Suicide relay status, non-voted for VSVO-R	Input	BIT
R4_SuicideNVS	Regulator 4 Suicide relay status, non-voted for VSVO-S	Input	BIT
R4_SuicideNVT	Regulator 4 Suicide relay status, non-voted for VSVO-T	Input	BIT
SysLim1PR1	System Limit 1 indication for Pulse Rate 1	Input	BIT
SysLim2PR1	System Limit 2 indication for Pulse Rate 1	Input	BIT
SysLim1PR2	System Limit 1 indication for Pulse Rate 2	Input	BIT
SysLim2PR2	System Limit 2 indication for Pulse Rate 2	Input	BIT
Reg1Suicide	Regulator 1 suicide relay status	Input	BIT
:	:	Input	BIT
Reg4Suicide	Regulator 4 suicide relay status	Input	BIT
Reg1_PosAFIt	Reg1, LM machine only, position A failure	Input	BIT
:	:	Input	BIT
Reg4_PosAFIt	Reg4, LM machine only, position A failure	Input	BIT
Reg1_PosBFIt	Reg1, LM machine only, position B failure	Input	BIT
:	:	Input	BIT
Reg4_PosBFIt	Reg4, LM machine only, position B failure	Input	BIT
Reg1_PosDif1	Reg1, LM machine only, position difference failure	Input	BIT
:	:	Input	BIT
Reg4_PosDif1	Reg4, LM machine only, position difference failure	Input	BIT
Reg1_PosDif2	Reg1, LM machine only, position difference failure	Input	BIT
:	:	Input	BIT
Reg4_PosDif2	Reg4, LM machine only, position difference failure	Input	BIT
RegCalMode	Regulator under calibration	Input	BIT
Reg1_Fdbk	Regulator 1 feedback	Input	FLOAT
:	:	Input	FLOAT
Reg4_Fdbk	Regulator 4 feedback	Input	FLOAT
MiscFdbk1a	Reg1, PosA when 4_LV_LM or Pilot when 2_LvpilotCy or 4_LVp/cylMax	Input	FLOAT
MiscFdbk1b	Reg1, PosB when 4_LV_LM or otherwise not used.	Input	FLOAT
MiscFdbk2a	Reg2, PosA when 4_LV_LM or Pilot when 2_LvpilotCy or 4_LVp/cylMax	Input	FLOAT
MiscFdbk2b	Reg2, PosB when 4_LV_LM or otherwise not used.	Input	FLOAT
MiscFdbk3a	Reg3, PosA when 4_LV_LM or Pilot when 2_LvpilotCy or 4_LVp/cylMax	Input	FLOAT
MiscFdbk3b	Reg3, PosB when 4_LV_LM or otherwise not used.	Input	FLOAT
MiscFdbk4a	Reg4, PosA when 4_LV_LM or Pilot when 2_LvpilotCy or 4_LVp/cylMax	Input	FLOAT

Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
MiscFdbk4b	Reg4, PosB when 4_LV_LM or otherwise not used.	Input	FLOAT
Reg1_Error	Regulator 1 position or flow rate error	Input	FLOAT
:	:	Input	FLOAT
Reg4_Error	Regulator 4 position or flow rate error	Input	FLOAT
Accel1	GPM/sec based on Pulse Rate 1	Input	FLOAT
Accel2	GPM/sec based on Pulse Rate 2	Input	FLOAT
Mon1	Position feedback based on Monitor 1	Input	FLOAT
:	:	Input	FLOAT
Mon12	Position feedback based on Monitor 12	Input	FLOAT
ServoOut1NVR	Servo Current Output 1, non-voted for VSVO-R	Input	FLOAT
ServoOut1NVS	Servo Current Output 1, non-voted for VSVO-S	Input	FLOAT
ServoOut1NVT	Servo Current Output 1, non-voted for VSVO-T	Input	FLOAT
ServoOut2NVR	Servo Current Output 2, non-voted for VSVO-R	Input	FLOAT
ServoOut2NVS	Servo Current Output 2, non-voted for VSVO-S	Input	FLOAT
ServoOut2NVT	Servo Current Output 2, non-voted for VSVO-T	Input	FLOAT
ServoOut3NVR	Servo Current Output 3, non-voted for VSVO-R	Input	FLOAT
ServoOut3NVS	Servo Current Output 3, non-voted for VSVO-S	Input	FLOAT
ServoOut3NVT	Servo Current Output 3, non-voted for VSVO-T	Input	FLOAT
ServoOut4NVR	Servo Current Output 4, non-voted for VSVO-R	Input	FLOAT
ServoOut4NVS	Servo Current Output 4, non-voted for VSVO-S	Input	FLOAT
ServoOut4NVT	Servo Current Output 4, non-voted for VSVO-T	Input	FLOAT
CalibEnab1	Enable calibration Reg 1	Output	BIT
:	:	Output	BIT
CalibEnab4	Enable calibration Reg 4	Output	BIT
SuicideForce1	Force suicide on Reg 1	Output	BIT
:	:	Output	BIT
SuicideForce4	Force suicide on Reg 4	Output	BIT
PossDiffEnab1	Position difference enable reg 1, LM only	Output	BIT
:	:	Output	BIT
PossDiffEnab4	Position difference enable reg 4, LM only	Output	BIT
Reg1_Ref	Reg 1 position reference	Output	FLOAT
:	:	Output	FLOAT
Reg4_Ref	Reg 4 position reference	Output	FLOAT
Reg1-GainMod	Reg 1 gain modifier (don't use)	Output	FLOAT
:	:	Output	FLOAT
Reg4-GainMod	Reg 4 gain modifier (don't use)	Output	FLOAT
Reg1_NullCor	Reg 1 null bias correction	Output	FLOAT
:	:	Output	FLOAT
Reg4_NullCor	Reg 4 null bias correction	Output	FLOAT
Internal Variables	Internal variables to service the auto-calibration display, not configurable		

Alarms

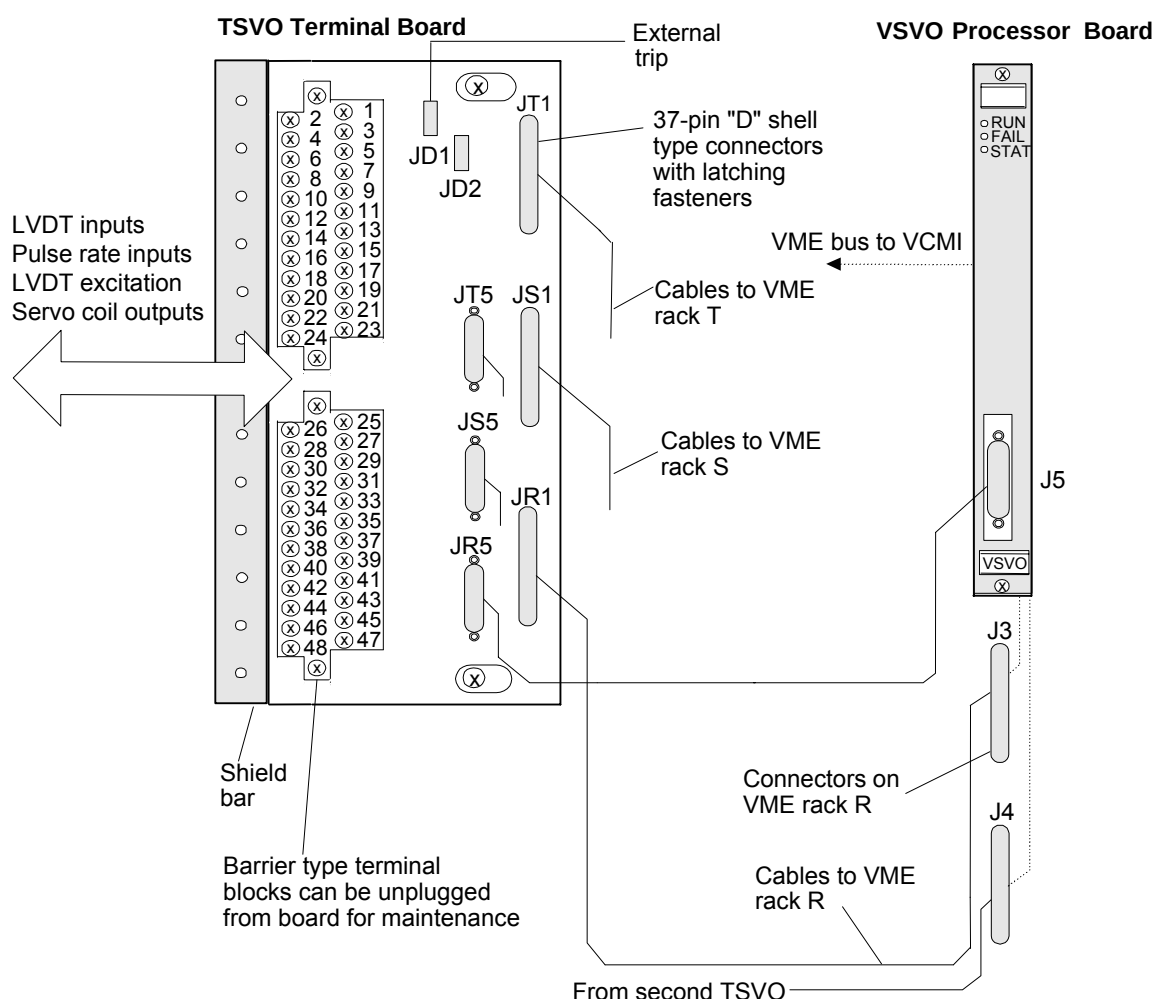
Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration.
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
33-44	LVDT # RMS Voltage Out of Limits. Minimum and maximum LVDT limits are configured	The LVDT may need recalibration.
45	Calibration Mode Enabled	The VSVO was put into calibration mode.
46	VSVO Board Not Online, Servos Suicided. The servo is suicided because the VSVO is not on-line	The controller (R, S, T) or IONet is down, or there is a configuration problem with the system preventing the VCMI from bringing the board on line.
47-51	Servo Current # Disagrees with Reference, Suicided. The servo current error (reference - feedback) is greater than the configured current suicide margin	A cable/wiring open circuit, or board problem.
52-56	Servo Current # Short Circuit. This is not currently used	NA
57-61	Servo Current # Open Circuit. The servo voltage is greater than 5V and the measured current is less than 10%	A cable/wiring open circuit, or board problem.
62-66	Servo Position # Feedback Out of Range, Suicided. Regulator number # position feedback is out of range, causing the servo to suicide	LVDT or board problem
67-71	Configuration Message Error for Regulator Number #. There is a problem with the VSVO configuration and the servo will not operate properly	The LVDT minimum and maximum voltages are equal or reversed, or an invalid LVDT, regulator, or servo number is specified.
72	Onboard Calibration Voltage Range Fault. The A/D calibration voltages read from the FPGA are out of limits, and the VSVO will use default values instead	A problem with the Field Programmable Gate Array (FPGA) on the board
73-75	LVDT Excitation # Voltage out of range	There is a problem with the LVDT excitation source on the VSVO board.

Fault	Fault Description	Possible Cause
77	Servo output assignment mismatch. Regulator types 8 & 9 use two servo outputs each. They have to be consecutive pairs, and they have to be configured as the same range	Fix the regulator configurations.
128-191	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
224-259	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TSVO Servo Input/Output

Functional Description

The Servo Input/Output (TSVO) terminal board interfaces with two electro-hydraulic servo valves that actuate the steam/fuel valves. Valve position is measured with LVDTs. Two cables connect to VSVO using the J5 plug on the front of VSVO and the J3 or J4 connector on the VME rack. TSVO provides simplex signals through the JR1 connector, and fans out TMR signals to the JR1, JS1, and JT1 connectors. Plugs JD1 or JD2 are for an external trip from the protection module.

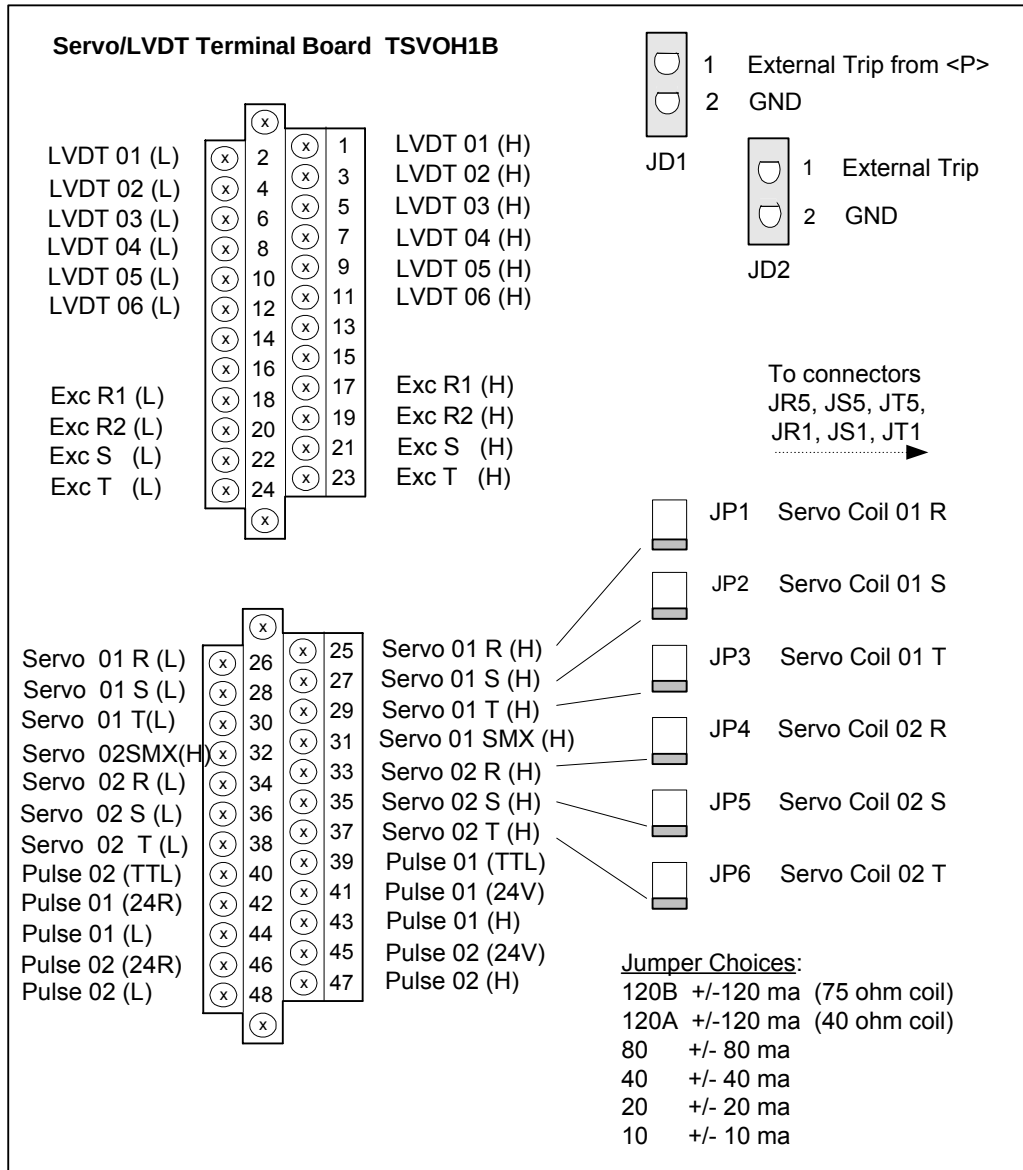


TSVO Servo Terminal Board and VSVO Processor Board

Installation

Connect the wires for the sensors and servo valves directly to two I/O terminal blocks on the terminal board, as displayed in the figure *Servo Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wiring. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block. Connect the wires for the external trip into JD1 or JD2. Cable the J5 connectors to the front of VSVO boards in racks <R>, <S>, and <T>. Cable the J1 connectors to the VME rack below VSVO in <R>, <S>, and <T>.

Each servo output can have three coils in TMR configuration. Each coil current is jumper selected using JP1-6.



Up to two #12 AWG wires per point with 300 V insulation

Terminal blocks can be unplugged from terminal board for maintenance

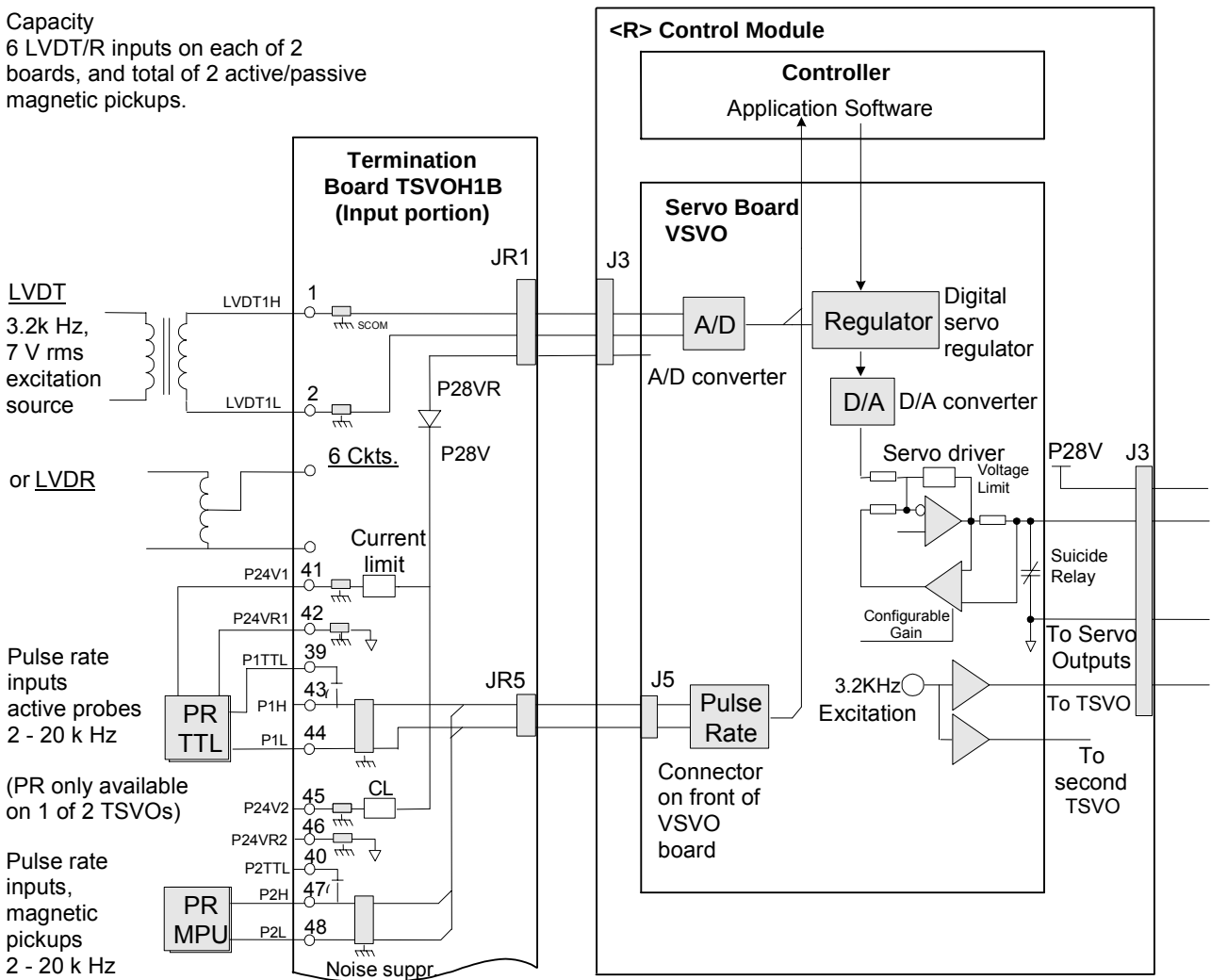
Servo Terminal Board Wiring

Operation

VSVO provides four channels consisting of bi-directional servo current outputs, LVDT position feedback, LVDT excitation, and pulse rate flows inputs. The TSVO provides excitation for, and accepts inputs from, up to six LVDT valve position inputs. There is a choice of one, two, three, or four LVDTs for each servo control loop. If three inputs are used they are available for gas turbine flow measuring applications. These signals come through TSVO and go directly to the VSVO board front at J5.

Each servo output is equipped with an individual suicide relay under firmware control that shorts the VSVO output signal to signal common when de-energized, and recovers to nominal limits after a manual reset command is issued. Diagnostics monitor the output status of each servo voltage, current, and suicide relay.

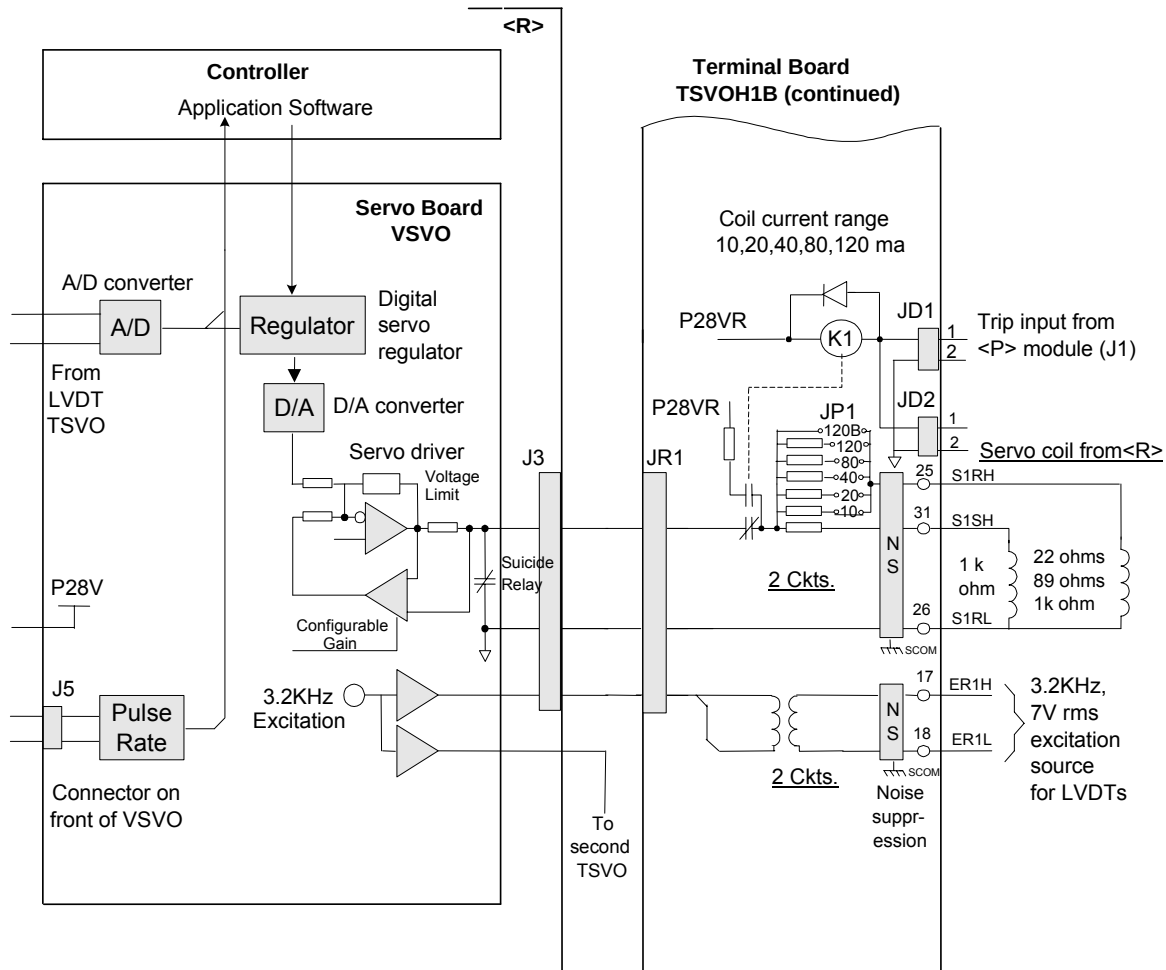
Capacity
6 LVDT/R inputs on each of 2
boards, and total of 2 active/passive
magnetic pickups.



LVDT and Pulse Rate Inputs, Simplex (Part 1 of 2)

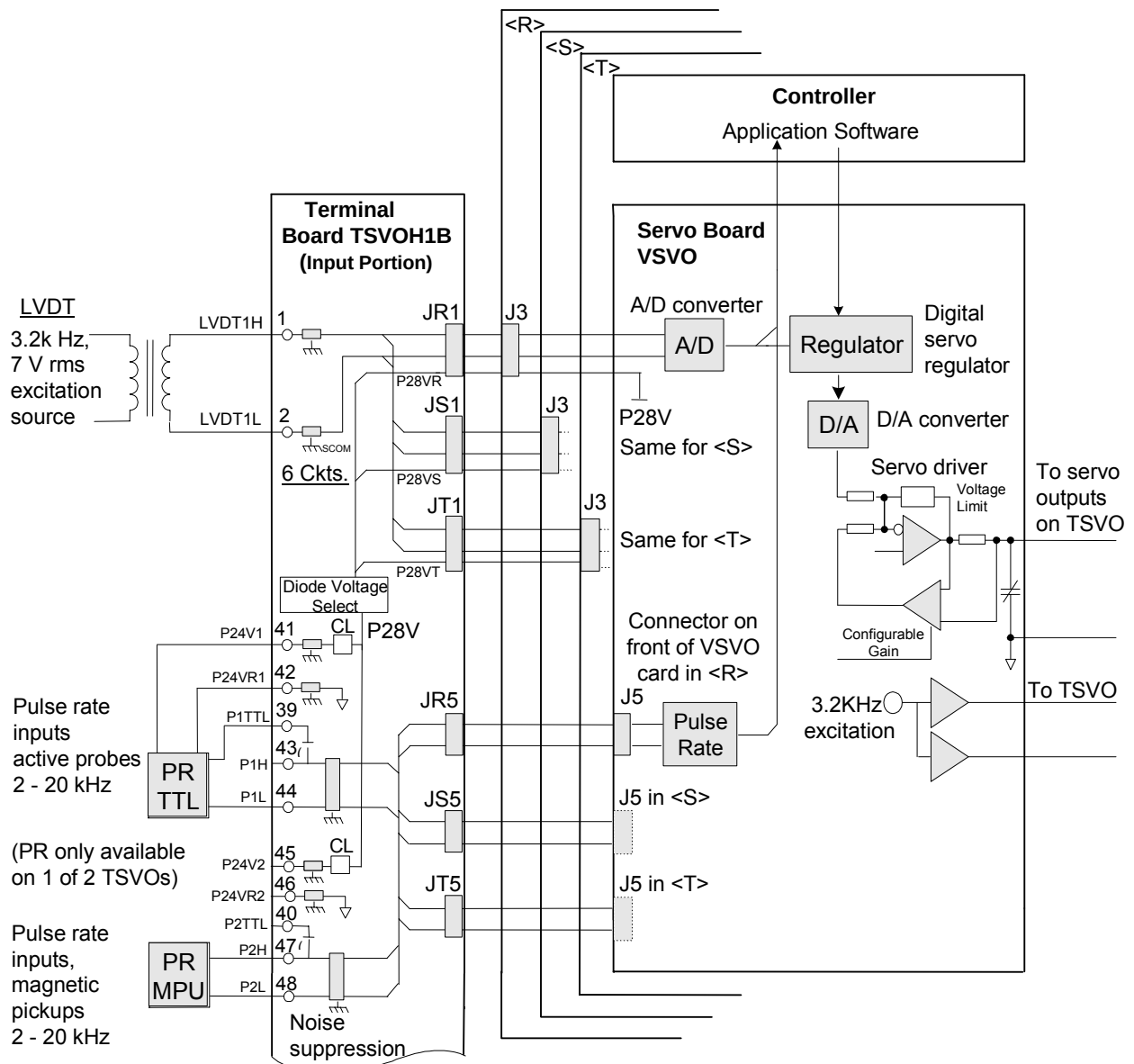
Each servo output channel can drive one or two-coil servos in simplex applications, or two or three-coil servos in TMR applications. The two-coil TMR applications are for 200# oil gear systems where each of two control modules drive one coil each, and the third control module has no servo coil interface. Servo cable lengths up to 300 meters (984 feet) are supported with a maximum two-way cable resistance of 15 Ω . Because there are many types of servo coils, a variety of bi-directional current sources are selectable by configuring jumpers.

Another trip override relay K1 is provided on each terminal board and is driven from the <P> Protection Module. If an emergency overspeed condition is detected in the Protection Module, the K1 relay energizes and disconnects the VSVO servo output from the terminal block and applies a bias to drive the control valve closed. This is only used on simplex applications to protect against the servo amplifier failing high, and is functional only with respect to the servo coils driven from <R>.



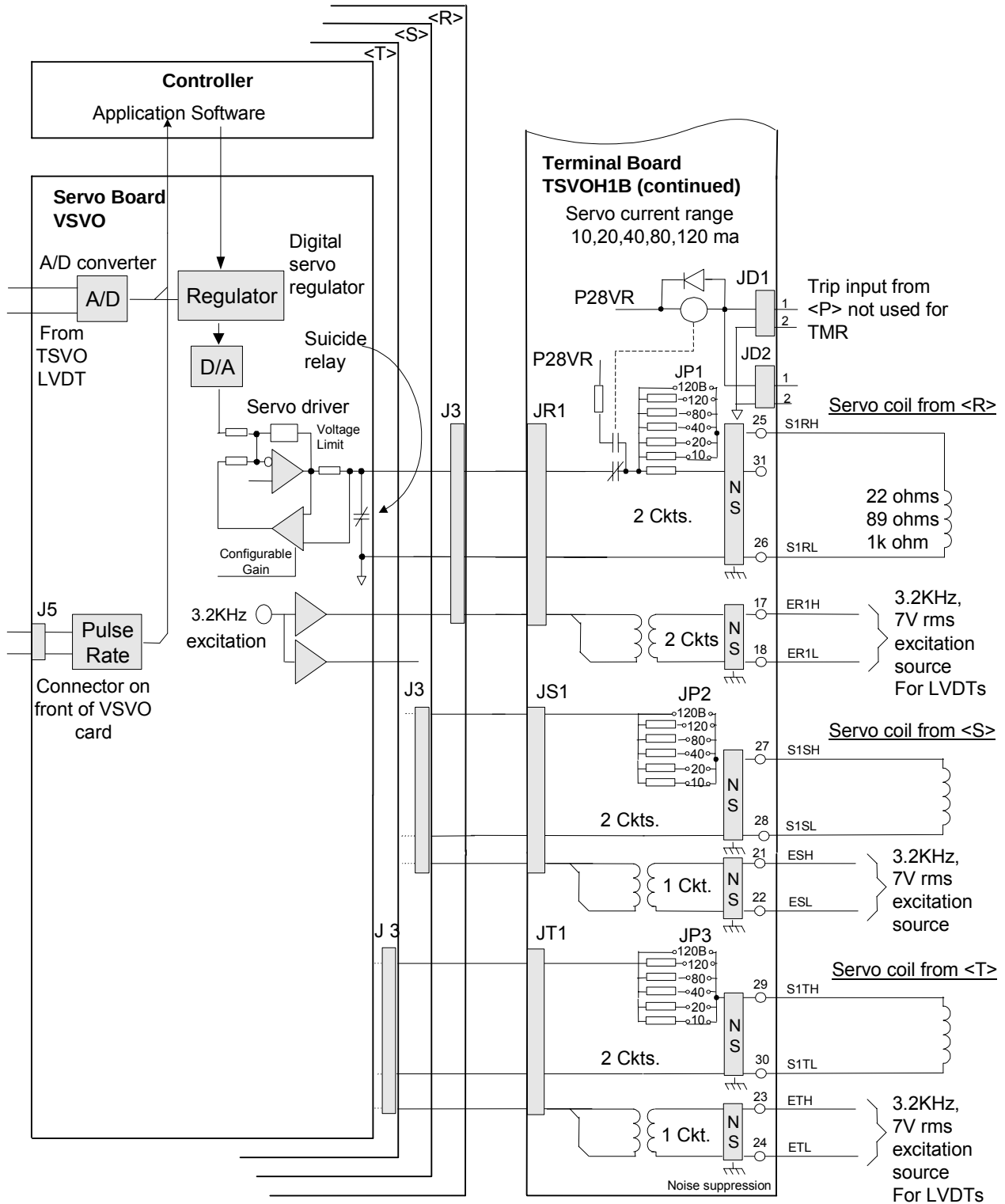
Servo Coil and LVDT Outputs, Simplex (Part 2 of 2)

In TMR applications, the LVDT signals on TSVO fan out to three racks through JR1, JS1, and JT1. Three connectors also bring power into TSVO where the three voltages are diode high-selected and current limited to supply 24 V dc to the pulse rate active probes.



LVDT and Pulse Rate Inputs, TMR (Part 1 of 2)

For TMR systems, each servo channel has connections to three output coils with a range of current ratings up to 120 mA, selected by jumper.



Servo Coil Outputs and LVDT Excitation, TMR System (Part 2 of 2)

The following table defines the standard servo coil resistance and their associated internal resistance, selectable with the terminal board jumpers shown in the figure above. In addition to these standard servo coils, it is possible to drive non-standard coils by using a non-standard jumper setting. For example, an 80 mA, 125 Ω coil could be driven by using a jumper setting 120B.

Servo Coil Ratings

Jumper Label	Nominal Current	Coil Resistance (Ohms)	Internal Resistance (Ohms)	Application
10	± 10 mA	1,000	180	Simplex and TMR
20	± 20 mA	125	442	Simplex
40	± 40 mA	62	195	Simplex
40	± 40 mA	89	195	TMR
80	± 80 mA	22	115	TMR
120A	± 120 mA (A)	40	46	Simplex
120B	± 120 mA (B)	75	10	TMR

The control valve position is sensed with either a four-wire LVDT or a three-wire LVDR. Redundancy implementations for the feedback devices are determined by the application software to allow the maximum flexibility. LVDT/Rs can be mounted up to 300 meters (984 feet) from the turbine control with a maximum two-way cable resistance of 15 Ω .

Each terminal board has two LVDT/R excitation sources for simplex applications and four for TMR applications. Excitation voltage is 7 V rms and the frequency is 3.2 kHz with a total harmonic distortion of less than 1% when loaded.

Note The excitation source is isolated from signal common (floating) and is capable of operation at common mode voltages up to 35 V dc, or 35 V rms, 50/60 Hz.

A typical LVDT/R has an output of 0.7 V rms at the zero stroke position of the valve stem, and an output of 3.5 V rms at the designed maximum stroke position (these are reversed in some applications). The LVDT/R input is converted to dc and conditioned with a low pass filter. Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check.

Two pulse rate inputs connect to a single J5 connector on the front of VSVO. This dedicated connection minimizes noise sensitivity on the pulse rate inputs.

Both passive magnetic pickups and active pulse rate transducers (TTL type) are supported by the inputs and are interchangeable without configuration. Pulse rate inputs can be located up to 300 meters (984) from the turbine control cabinet; this assumes shielded-pair cable is used with typically 70 nF single ended or 35 nF differential capacitance and 15 ohms resistance.

A frequency range of 2 to 30 kHz can be monitored at a normal sampling rate of either 10 or 20 ms. Magnetic pickups typically have an output resistance of 200 Ω and an inductance of 85 mH excluding cable characteristics. The transducer is a high impedance source, generating energy levels insufficient to cause a spark.

Note The maximum short circuit current is approximately 100 mA with a maximum power output of 1 W.

Specifications

Item	Specification
Number of inputs	6 LVDT windings 2 pulse rate signals (total of 2 per VSVO) External trip signal
Number of outputs	2 servo valves (total of 4 per VSVO board) 4 excitation sources for LVDTs 2 excitation sources for pulse rate transducers
Power supply voltage	Nominal 24 V dc
LVDT excitation output	Frequency of 3.2 $\pm$ 0.2 kHz Voltage of 7.00 $\pm$ 0.14 V rms
Pulse rate input	Minimum signal for proper measurement at 2 Hz is 33 mVpk, and at 12 kHz is 827 mVpk.
Magnetic PR pickup signal	Generates 150 V p-p into 60 k Ω
Active PR Pickup Signal	Generates 5 to 27 V p-p into 60 k Ω
Fault detection	Servo current out of limits or not responding Regulator feedback signal out of limits Failed ID chip
Size	17.8 cm high x 33.02 cm wide (7 in. x 13 in.)
Technology	Surface mount

Diagnostics

VSVO performs diagnostic checks on the terminal board, including the following:

- If the output servo current is out of limits or not responding, a fault is created.
- If the regulator feedback (LVDT) signal is out of limits, a fault is created and if the associated regulator has two sensors, the bad sensor is removed from the feedback calculation and the good sensor is used.
- If any one of the above signals go unhealthy a composite diagnostic alarm, L#DIAG_VSVO occurs. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and reset with the RESET_DIA signal if they go healthy.
- Each cable connector on the terminal board has its own ID device that is interrogated by the I/O processor. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the J connector location. When this chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

For a simplex system, jumper JP1 configures the coil current of Servo 1, and jumper JP4 configures the coil current of Servo 2. Refer to the table *Servo Coil Ratings* for more information.

In a TMR system, each servo output can have three coils. Jumpers JP 1 – 3 configure the coil current for Servo 1, and Jumpers JP 4 – 6 configure the coil current for Servo 2. All other configuration is done from the toolbox.

DSVO Simplex Servo Input/Output

Functional Description

The Simplex Servo Input/Output (DSVO) terminal board is a compact terminal board designed for DIN-rail mounting. This board has two servo outputs, I/O for six LVDT position sensors, and two active pulse rate inputs for flow measurement. Servo coil currents ranging from 10 to 120 mA can be selected using jumpers. DSVO connects to the VSVO processor board with a 37-pin cable, which is identical to those used on the larger TSVO board. The terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space. Two DSVO boards can be connected to the VSVO, if required. Only a simplex version of this board is available.

The on-board functions and high frequency decoupling to ground are the same as those on the TSVO. High density Euro-Block type terminal blocks are permanently mounted to the board with six screws for the ground connection (SCOM). Connectors JR1 and J5 connect to signals from on-board ID chips that identify the board to the VSVO for system diagnostic purposes.

Two versions of the DSVO, H1B and H2B, are available. The H1B is a direct replacement for the previous H1A design. The H2B is certified by UL for Class 1 Division 2 applications.

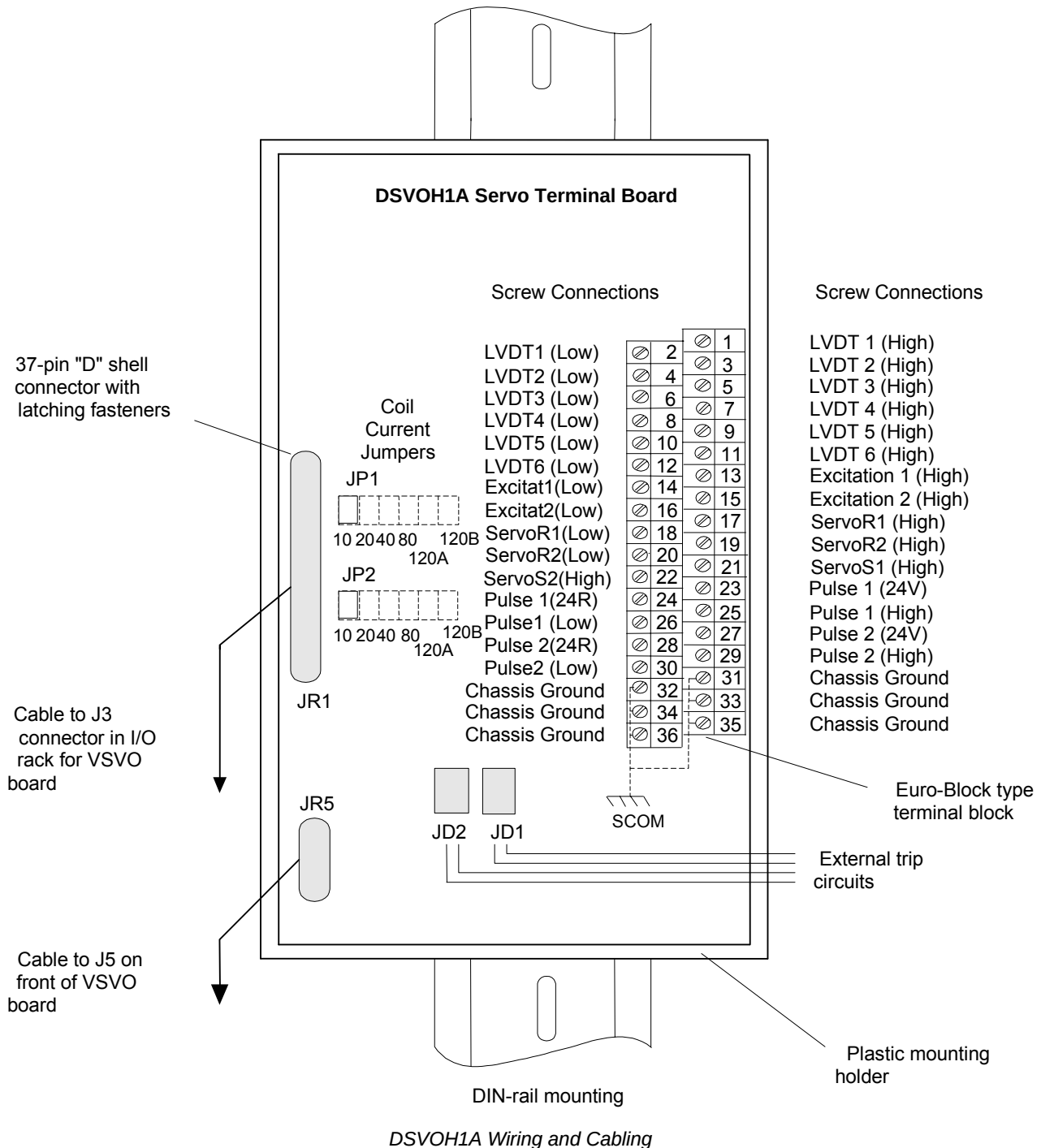
DSVOH1B vs. DSVOH2B

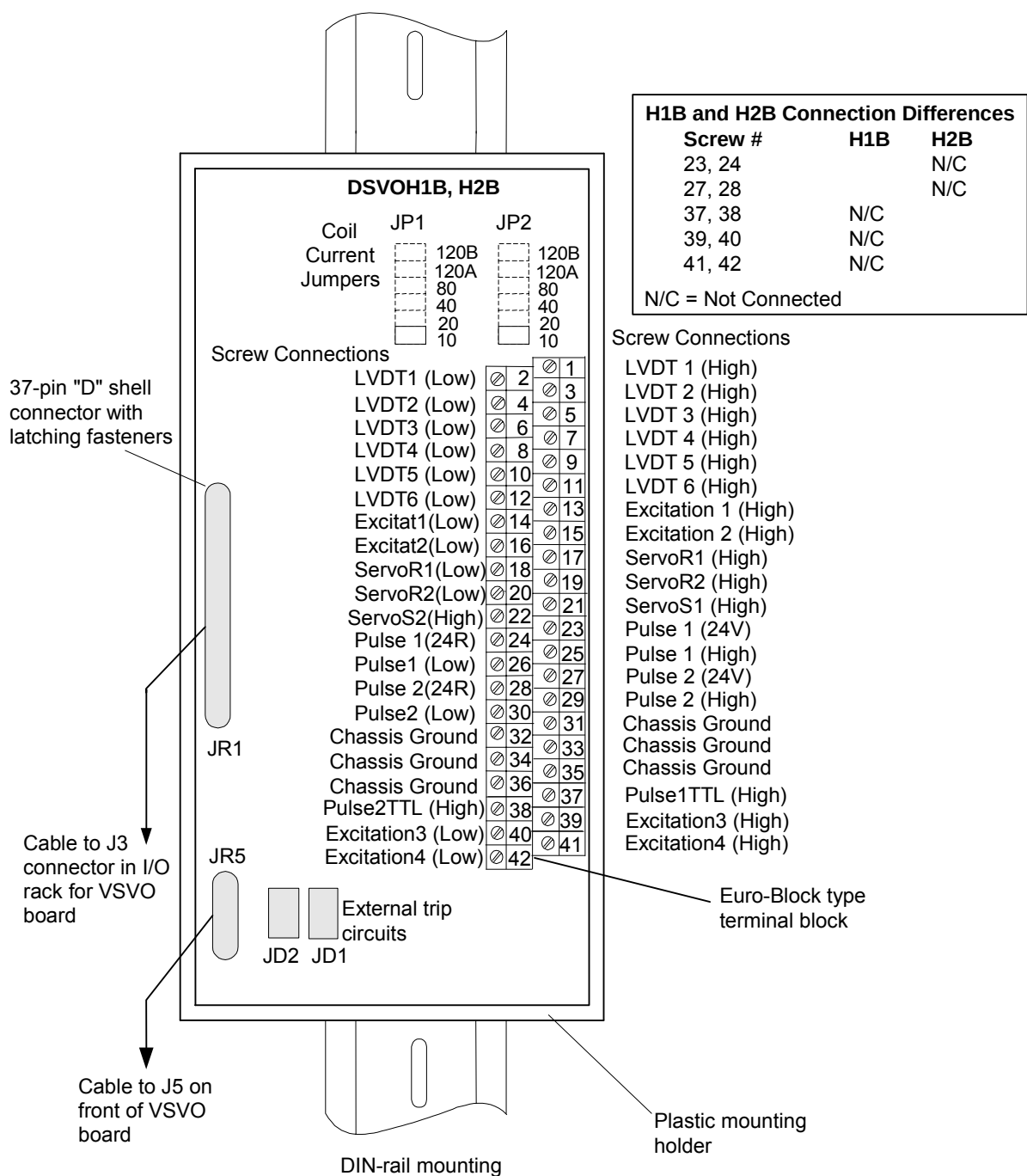
Function	H1B	H2B
Class 1, Div. 2 certification	No	Yes
Servo valves accommodated	75, 40, 22, 62, 89, 125, 1 k Ω	1 k Ω (10 mA)
LVDT excitation outputs	2 at 120 mA each	4 at 60 mA each
Excitation for pulse rate probes	2 at 24 V dc, 100 mA each	No
Additional pulse rate inputs for TTL No signals		2

Installation

Mount the plastic holder on the DIN-rail and slide the DSVO board into place. Connect the wires for the servo I/O directly to the terminal block. The Euro-Block type terminal block has 36 terminals (DSVOH1A) or 42 terminals (DSVOH1B,H2B) and is permanently mounted on the terminal board. Typically #18 AWG shielded twisted pair wiring is used. Six screws, 31 – 36, are provided for SCOM (ground) connection, which should be as short as distance as possible.

Note There is no shield termination strip with this design.



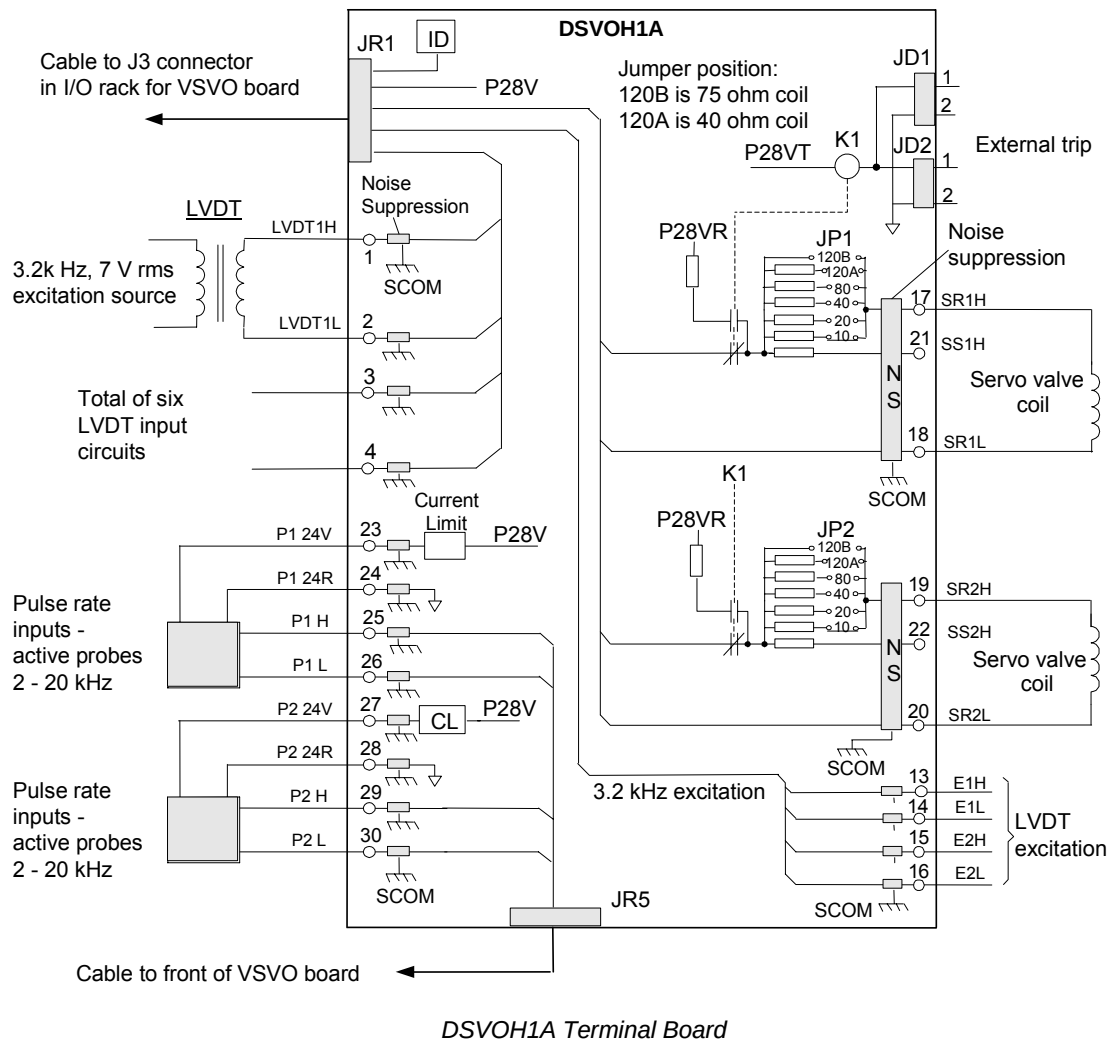


DSVOH1B, H2B Wiring and Cabling

Operation

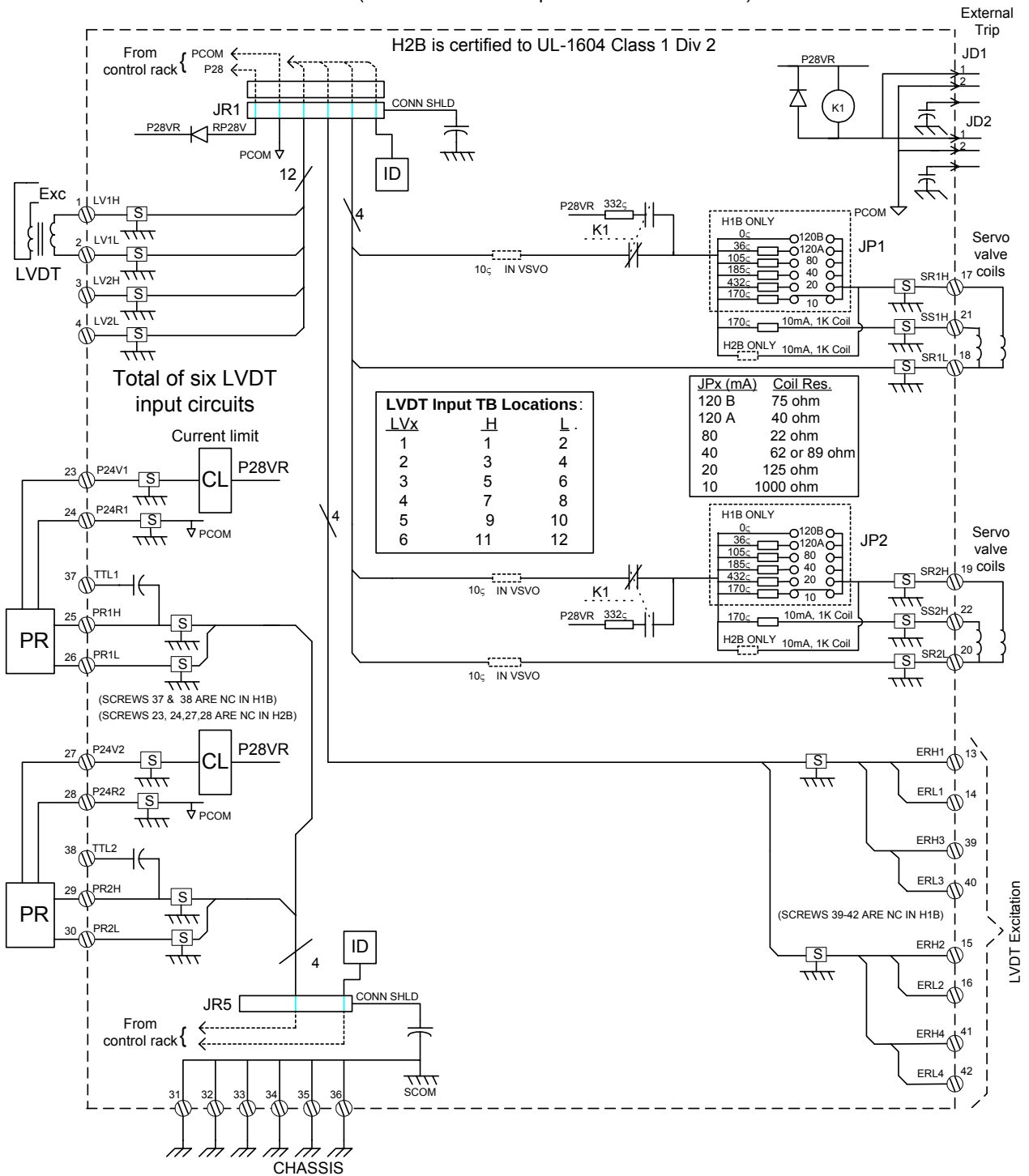
DSVO Version H1A

The following figures show operation of two versions of the DSVO board.



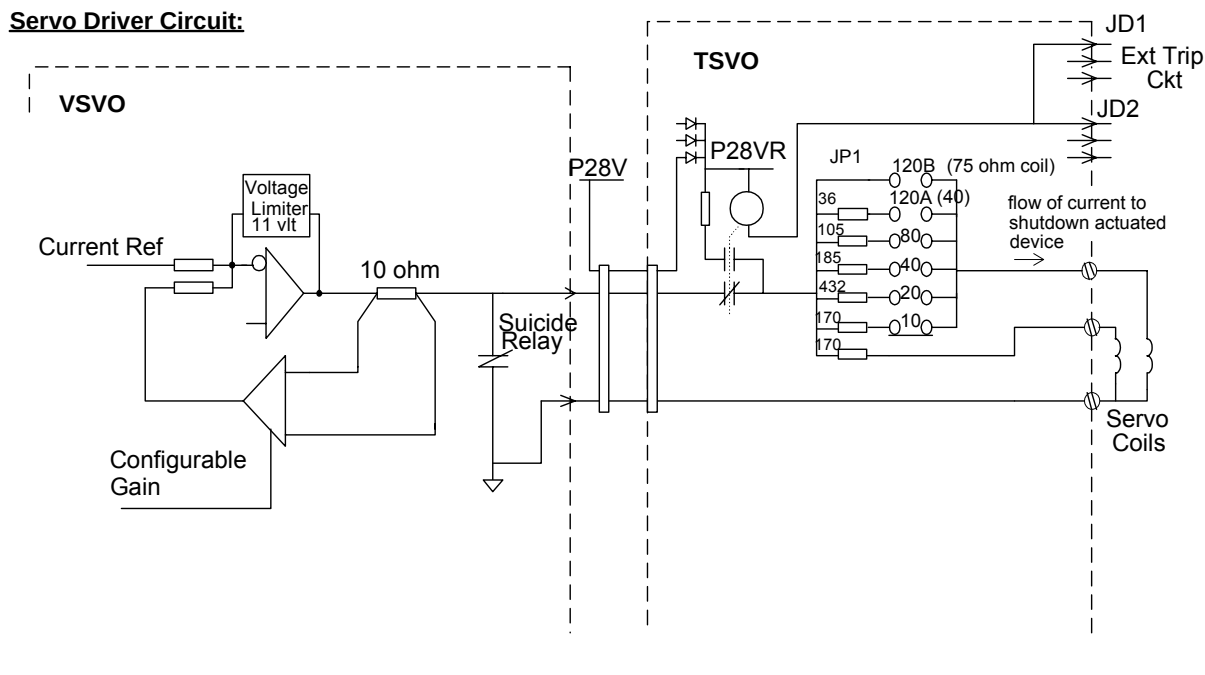
DSVO Versions H1B, H2B

(IS200DSVOH1B Replaces IS200DSVOH1A)



DSVOH1B, H2B Board (Part 1 of 2)

Servo Driver Circuit:



DSVOH1B, H2B board (Part 2 of 2)

Specifications

Item	Specification
Number of inputs	6 LVDT windings
	2 pulse rate signals
	External trip signal
Number of outputs	2 servo valves
	2 excitation sources for LVDTs
	2 excitation sources for pulse rate transducers
LVDT excitation output	2 Outputs: Frequency of 3.2 ± 0.2 kHz
	Voltage of 7.00 ± 0.14 V rms
Pulse rate input	Minimum signal for proper measurement at 2 Hz is 33 mVpk, and at 12 kHz is 827 mVpk.
Magnetic PR pickup signal	Generates 150 V p-p into 60Ω , used on DSVOH2B.
Active PR Pickup Signal	Generates 5 to 27 V p-p into 60Ω , used on DSVOH1B.
Fault detection	Servo current out of limits or not responding.
	The LVDT excitation is out of range.
	The LVDT feedback is out of limits.
	Failed ID chip.
Size	23.8 cm high x 8.6 cm wide (9.37 in. x 3.4 in.) complete with support plate

Diagnostics

VSVO performs diagnostic checks on DSVO including the following:

- If the output servo current is out of limits or not responding, a fault is created.
- If the regulator feedback (LVDT) signal is out of limits, a fault is created and if the associated regulator has two sensors, the bad sensor is removed from the feedback calculation and the good sensor is used.
- If any one of the above signals go unhealthy a composite diagnostic alarm, L#DIAG_VSVO, occurs. Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and reset with the RESET_DIA signal if they go healthy.
- Connector JR1 on the terminal board has its own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the connector location. When the chip is read by VSVO and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

On DSVOH1B, jumpers JP1 and JP2 select the desired coil current and servo valve coil resistance, which varies from 22 W to 1,000 W. The following table shows the coil currents and resistances (for example, jumper 120B provides a ± 120 mA coil current).

Jumper J1/2 Label (mA)	Coil Resistance
120B	75 Ω
120A	40 Ω
80	22 Ω
40	62 or 89 Ω
20	125 Ω
10	1,000 Ω

With DSVOH2B, only a 1,000 Ω , 10 mA coil can be driven, so there are no jumper settings.

Notes

VTCC Thermocouple Input

VTCC Thermocouple Input

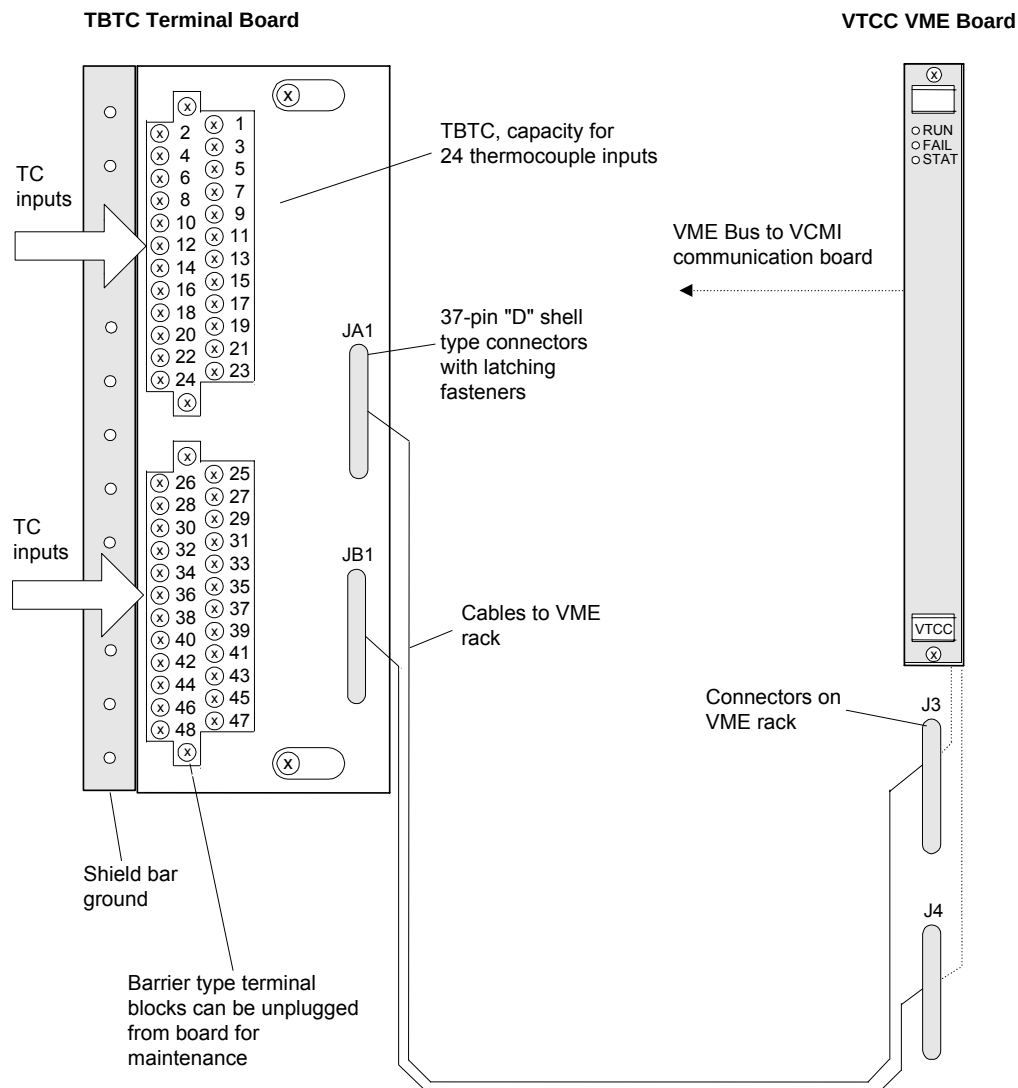
Functional Description

The Thermocouple Input (VTCC) board accepts 24 thermocouple inputs. These inputs are wired to the TBTC or DTTC terminal boards. Cables with molded plugs connect the terminal board to the VME rack where the VTCC thermocouple processor board is located. The TBTC can provide both simplex (TBTCH1C) or triple module redundant (TMR) control (TBTCHIB). Two groups of the VTCC provide different temperature ranges optimized for gas turbine control applications (VTCCH1) and general-purpose applications (VTCCH2). The same terminal boards are used with both groups of the VTCC card.

VTCCH1 supports E, J, K, S, and T types of thermocouples and mV inputs. The mV span is -8mV to +45mV.

VTCCH2 supports E, J, K, S, T as well as B, N, and R types of standard thermocouples and mV inputs. The mV span for VTCCH2 is -20mV to +95mV.

Note Input data is transferred over the VME backplane from VTCC to the VCMI and then to the controller.



Thermocouple Input Terminal Board, I/O Board, and Cabling

Installation

➤ To install the V-type board

- 1 Power down the VME processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel

Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the section on diagnostics in this document.

Operation

Type E, J, K, S, and T thermocouples can be used with VTCCH1, and they can be grounded or ungrounded. Type E, J, K, S, T, B, N and R thermocouples can be used with VTCCH2, and they can be grounded or ungrounded. They can be located up to 300 m (984 ft) from the turbine control cabinet with a maximum two-way cable resistance of 450 Ω . High frequency noise suppression and two cold junction (CJ) reference devices are mounted on the terminal board.

Linearization for individual thermocouple types is performed in software by VTCC. A thermocouple that is determined to be out of the hardware limits is removed from the scanned inputs to prevent adverse affects on other input channels.

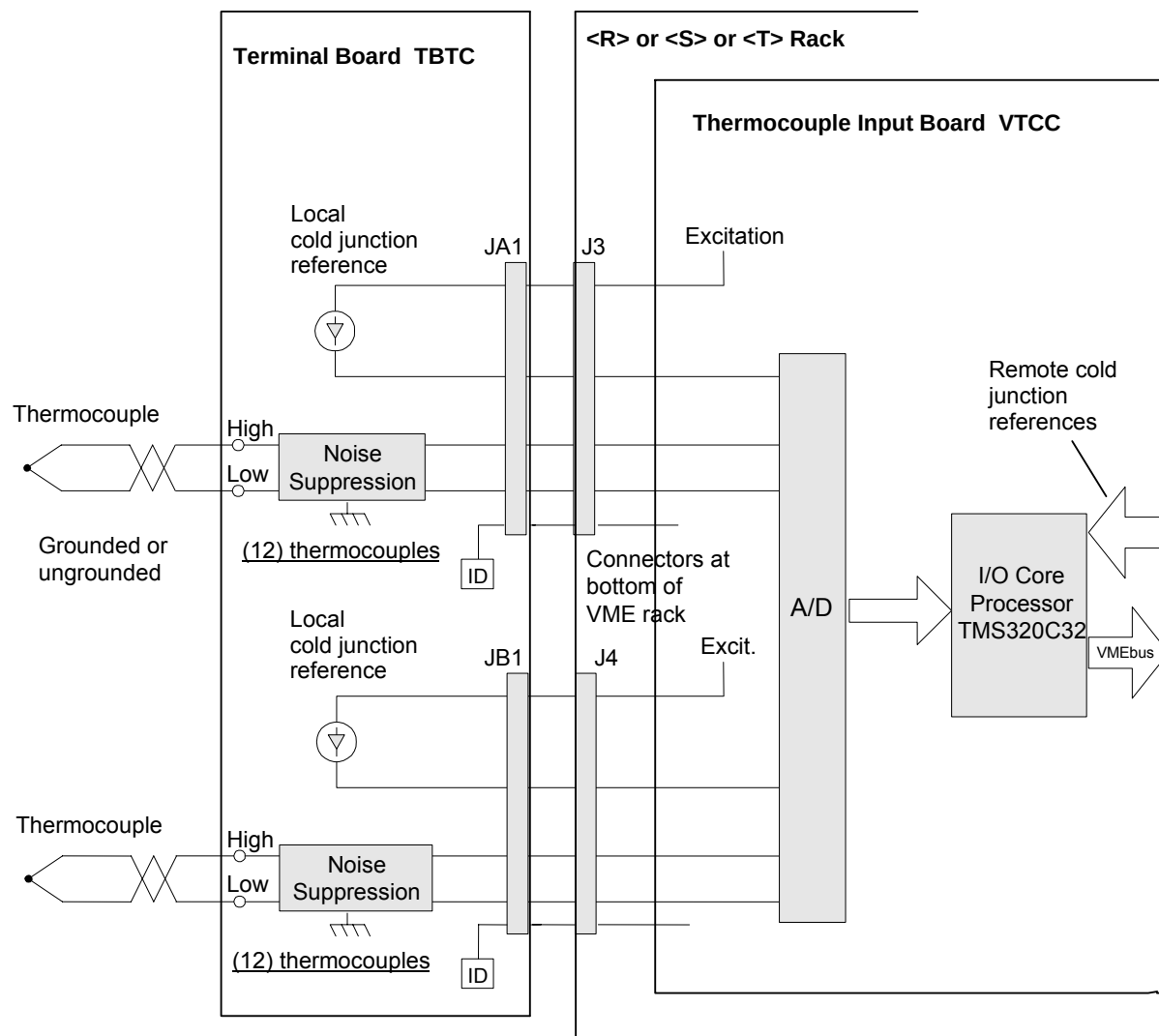
Cold Junctions

If both CJ devices are within the configurable limits, then the average of the two is used for CJ compensation. If only one CJ device is within the configurable limits, then that CJ is used for compensation. If neither CJ device is within the configurable limits, then a default value is used. The thermocouple inputs and cold junction inputs are automatically calibrated using the filtered calibration reference and zero voltages.

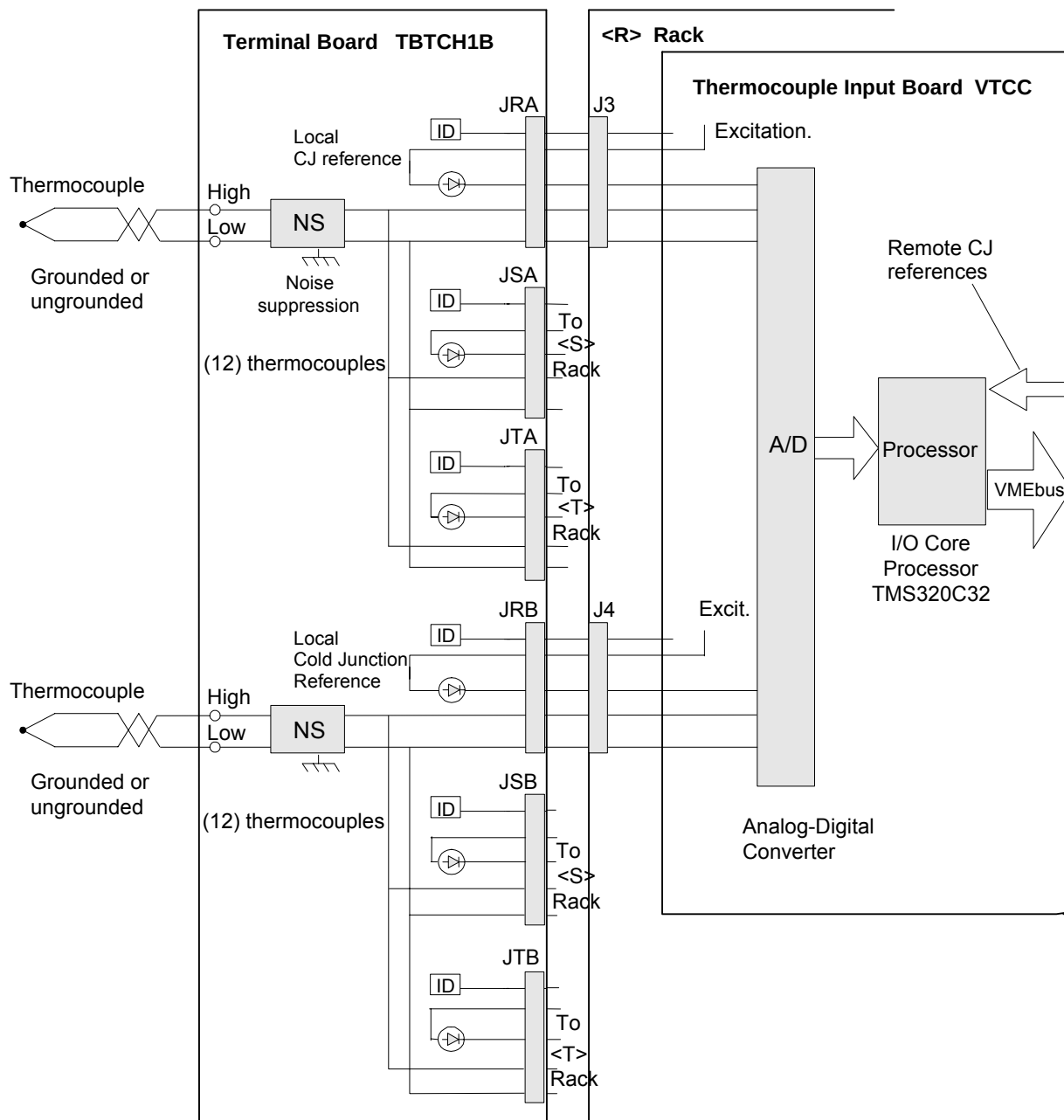
Note VTCC boards manufactured after software version VTCC-100100C and higher have additional thermocouple and cold junction features. The newly designed boards permit the use of S-type thermocouples, in addition to all previous types. They also provide for a remote CJ compensation feature for thermocouple inputs. This allows the user to select whether CJ compensation is done based on a temperature reading at a remote location or at the terminal board as explained above. The calculations are the same as previous VTCC boards, only the source of the CJ reading changes.

Two CJ references are used per VTCC, one each for connectors J3 and J4. Each reference can be selected as either remote (from VME bus) or local (from associated terminal board, T-type or D-type). All references are then treated as sensor inputs (for example, averaged, limits configured). The two references can be mixed, one local and one remote. CJ signals go into signal space and are available for monitoring. Normally the average of the two is used. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation causes a 1 °F error in the thermocouple reading.

Hard coded limits are set at 32 to 158 °F, and if a CJ goes outside this range, it is regarded as bad. Most CJ failures are open or short circuit. If one CJ fails, the good one is used. If both CJs fail, the backup value is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value.



Simplex Thermocouple Inputs to VTCC Processor Board



TMR Thermocouple Inputs to VTCC Processor Boards

Thermocouple inputs are supported over a full-scale input range of -8.0 mV to +45.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from +32 to +158 °F.

Thermocouple	E	J	K	S	T
Low range, °F / °C	-60 / -51	-60 / -51	-60 / -51	0 / -17.78	-60 / -51
mV at low range with reference at 158 °F (70°C)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F / °C	1100 / 593	1400 / 798	2000 / 1093	3200 / 1760	750 / 399
mV at high range with reference at 32 °F (0°C)	44.547	42.922	44.856	18.612	20.801

VTCCCH1 Thermocouple Range

Thermocouple inputs are supported over a full-scale input range of -8.0 mV to +45.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from 0 to 70°C (+32 to +158 °F).

Thermocouple Type VTCCCH1	E	J	K	S	T
Low range, °F	-60	-60	-60	0	-60
°C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1100	1400	2000	3200	750
°C	593	760	1093	1760	399
mV at high range with reference at 0°C (32 °F)	44.547	42.922	44.856	18.612	20.801

VTCCCH2 Thermocouple Range

Thermocouple inputs support a full-scale input range of -20.0 mV to + 95.0 mV. The following table shows typical input voltages for different thermocouple types versus the minimum and maximum temperature range. The CJ temperature is assumed to range from 0 to 70°C (+32 to +158 °F).

Thermocouple Type VTCCCH2	E	J	K	S	T
Low range, °F	-60	-60	-60	0	-60
°C	-51	-51	-51	-17.78	-51
mV at low range with reference at 70°C (158 °F)	-7.174	-6.132	-4.779	-0.524	-4.764
High range, °F	1832	2192	2372	3200	752
°C	1000	1200	1300	1760	400
mV at high range with reference at 0°C (32 °F)	76.373	69.553	52.41	18.612	20.869

Thermocouple Type VTCCCH2	B	N	R
Low range, °F	32	-60	0
°C	0	-51	-17.78
mV at low range with reference at 70°C (158 °F)	-0.0114	-3.195	-0.512
High range, °F	3272	2282	3092
°C	1800	1250	1700
mV at high range with reference at 0°C (32 °F)	13.593	45.694	20.220

Specifications

Item	Specifications
Number of channels	24 channels per terminal board and I/O board
Thermocouple types	E, J, K, S, T thermocouples, and mV inputs for VTCCH1 E, J, K, S, T, B, N, R thermocouples, and mV inputs for VTCCH2
Span	-8 mV to +45 mV for VTCCH1 -20 mV to +95 mV for VTCCH2
A/D converter	Sampling type 16-bit A/D converter with better than 14-bit resolution
CJ compensation	Reference junction temperature measured at two locations on each terminal board (option for remote CJs). TMR board has six CJ references.
Cold junction temperature accuracy	Cold junction accuracy 1.1°C (2 °F)
Conformity error	Maximum software error 0.14°C (0.25 °F)
Measurement accuracy	VTCCH1 = 53 µV (excluding cold junction reading). Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 3 °F VTCCH1 = 115 µV (excluding cold junction reading). Example: For type K, at 1000 °F, including cold junction contribution, RSS error= 6 °F
Common mode rejection	Ac common mode rejection 110 dB @ 50/60 Hz, for balanced impedance input
Common mode voltage	±5 V
Normal mode rejection	Rejection of 250 mV rms is 80 dB @ 50/60 Hz
Scan time	All inputs are sampled at 120 times per second for 60 Hz operation; for 50 Hz operation it is 100 times per second
Fault detection	High/low (hardware) limit check High/low system (software) limit check Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings

Diagnostics

Three LEDs at the top of the front panel provide status information. The normal run condition is a flashing green, and fail is a solid red. The third LED shows a steady orange if a diagnostic alarm condition exists in the board. Diagnostic checks include the following:

- Each thermocouple type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded a logic signal is set and the input is no longer scanned. If any one of the 24 inputs hardware limits is set it creates a composite diagnostic alarm, L3DIAG_VTCC, referring to the entire board. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.
- Each thermocouple input has system limit checking based on configurable high and low levels. These limits can be used to generate alarms, and can be configured for enable/disable, and as latching/non-latching. RESET_SYS resets the out of limit signals.
- In TMR systems, if one signal varies from the voted value (median value) by more than a predetermined limit, that signal is identified and a fault is created. This can provide early indication of a problem developing in one channel.
- Each terminal board and I/O board has its own ID device, which is interrogated by the I/O board. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the JA1/JB1 connector location. When the chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created. Details of diagnostic faults are in the *Alarms* section of this document.

Configuration

Note The following information is extracted from the toolbox and represents a sample of the configuration information for this board. Refer to the actual configuration file within the toolbox for specific information.

Parameter	Description	Choices
Configuration		
SysFreq	System frequency (used for noise rejection)	50 or 60 Hz
SystemLimits	Enables or disables all system limit checking	Enable, disable
Auto Reset	Automatic Restoring of Thermocouples removed from scan	Enable, disable
J3J4:I200TBTC1A	Terminal board	Connected, Not Connected
ThermCpl1	First of 24 thermocouples - board point signal	Point edit (input FLOAT)
ThermoCpl Type	Thermocouples supported by VTCC; unused inputs are removed from scanning, mV inputs are primarily for maintenance. When configured for mV input, the signal span is –8 mV to +45 mV. The input is not compensated for CJ and is a straight reading of the terminal board mV input. In order to detect open wires, each input is biased using plus and minus 0.25 V through 10 Ω resistors. This should be taken into account if high impedance mV signals are to be read.	Unused, mV, S, T, K, J, E
LowPassFiltr	Enable 2 Hz low pass filter	Enable, disable
SysLim1 Enabl	Enables or disables a temperature limit which can be used to create an alarm.	Enable, disable
SysLim1 Latch	Determines whether the limit condition will latch or unlatch; reset used to unlatch.	Latch, unlatch
SysLim1 Type	Limit occurs when the temperature is greater than or equal ($\geq$), or less than or equal to ($\leq$) a preset value.	Greater than or equal, less than or equal

Parameter	Description	Choices
SysLimit 1	Enter the desired value.	Engineering units
SysLim2 Enabled	Enables or disables a temperature limit which can be used to create an alarm.	Enable, disable
SysLim2 Latch	Determines whether the limit condition will latch or unlatch; reset used to unlatch.	Latch, unlatch
SysLim2 Type	Limit occurs when the temperature is greater than or equal (>=), or less than or equal to (<=) a preset value.	Greater than or equal, less than or equal
SysLimit 2	Enter the desired value.	Engineering units
TMR Diff Limt	Limit condition occurs if 3 temperatures in R, S, T differ by more than a preset value (deg F); this creates a voting alarm condition.	-60 to 2,000
ColdJunc1	First CJ reference - Board point signal (similar configuration as for thermocouples but no low pass filter or CJ type choices of local or remote).	As above (input FLOAT)
ColdJunc2	Second CJ reference - Board point signal (similar configuration as for thermocouples but no low pass filter or CJ type choices of local or remote).	As above (input FLOAT)

Board Points (Signals)	Description-Point Edit (Enter Signal Connection Name)	Direction	Type
L3DIAG_VTCC1	Board diagnostic	Input	BIT
L3DIAG_VTCC2	Board diagnostic	Input	BIT
L3DIAG_VTCC3	Board diagnostic	Input	BIT
SysLim1TC1	System limit 1 for thermocouple	Input	BIT
:	:	Input	BIT
SysLim1TC24	System limit 1 for thermocouple	Input	BIT
SysLim1CJ1	System limit 1 for CJ	Input	BIT
SysLim1JC2	System limit 1 for CJ	Input	BIT
SysLim2TC1	System limit 2 for thermocouple	Input	BIT
:	:	Input	BIT
SysLim2TC24	System limit 2 for thermocouple	Input	BIT
SysLim2CJ1	System limit 2 for CJ	Input	BIT
SysLim2CJ2	System limit 2 for CJ	Input	BIT
CJ Backup	CJ backup	Output	FLOAT
CJ Remote 1	CJ remote 1	Output	FLOAT
CJ Remote 2	CJ remote 2	Output	FLOAT
ThermCpl1	Thermocouple reading	Input	FLOAT
:	:	Input	FLOAT
ThermCpl24	Thermocouple reading	Input	FLOAT
ColdJunc1	CJ for thermocouples (TC) 1-12	Input	FLOAT
ColdJunc2	CJ for TCs 13-24	Input	FLOAT

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration.
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure.	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: []; Tre: [] The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: []; Tre:[] The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32-55	Thermocouple [] Raw Counts High. The [] thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	A condition such as stray voltage or noise caused the input to exceed +63 millivolts.
56-79	Thermocouple [] Raw Counts Low. The [] thermocouple input to the analog to digital converter exceeded the converter limits and will be removed from scan	The board has detected a thermocouple open and has applied a bias to the circuit driving it to a large negative number, or the TC is not connected, or a condition such as stray voltage or noise caused the input to exceed -63 millivolts.
80,81	Cold Junction [] Raw Counts High. CJ device number [] input to the A/D converter has exceeded the limits of the converter. Normally two CJ inputs are averaged; if one is detected as bad then the other is used. If both CJs fail, a predetermined value is used	The CJ device on the terminal board has failed.
82,83	Cold Junction [] Raw Counts Low. CJ device number [] input to the A/D converter has exceeded the limits of the converter. Normally two CJ inputs are averaged; if one is detected as bad then the other is used. If both CJs fail, a predetermined value is used	The CJ device on the terminal board has failed.
84,85	Calibration Reference [] Raw Counts High. Calibration Reference [] input to the A/D converter exceeded the converter limits. If Cal. Ref. 1, all even numbered TC inputs will be wrong; if Cal. Ref. 2, all odd numbered TC inputs will be wrong	The precision reference voltage on the board has failed.
86,87	Calibration Reference [] Raw Counts Low. Calibration Reference [] input to the A/D converter exceeded the converter limits. If Cal. Ref. 1, all even numbered TC inputs will be wrong; if Cal. Ref. 2, all odd numbered TC inputs will be wrong	The precision reference voltage on the board has failed.
88,89	Null Reference [] Raw Counts High	The null reference voltage signal on the board has failed.

Fault	Fault Description	Possible Cause
90,91	Null Reference [] Raw Counts Low. The null (zero) reference number [] input to the A/D converter has exceeded the converter limits. If null ref. 1, all even numbered TC inputs will be wrong; if null ref. 2, all odd numbered TC inputs will be wrong	The null reference voltage signal on the board has failed.
92-115	Thermocouple [] Linearization Table High. The thermocouple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's maximum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the CJ compensation is wrong.
116- 139	Thermocouple [] Linearization Table Low. The thermocouple input has exceeded the range of the linearization (lookup) table for this type. The temperature will be set to the table's minimum value	The thermocouple has been configured as the wrong type, or a stray voltage has biased the TC outside of its normal range, or the CJ compensation is wrong.
160- 255	Logic Signal [] Voting mismatch	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
256- 281	Input Signal [] Voting mismatch, Local [], Voted []. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TBTC Thermocouple Input

Functional Description

The Thermocouple Input (TBTC) terminal board accepts 24-type E, J, K, S, or T thermocouple inputs. It accepts additional B, N and R types of thermocouple inputs only when used with PTCC2 in Mark VIe. These inputs are wired to two barrier-type blocks on the terminal board. TBTC communicates with the I/O processor through DC-type connectors. Two types of the TBTC are available, as follows:

- TBTC1C for simplex applications has two DC-type connectors.
- TBTC1B for TMR applications has six DC-type connectors.

Mark VI Systems

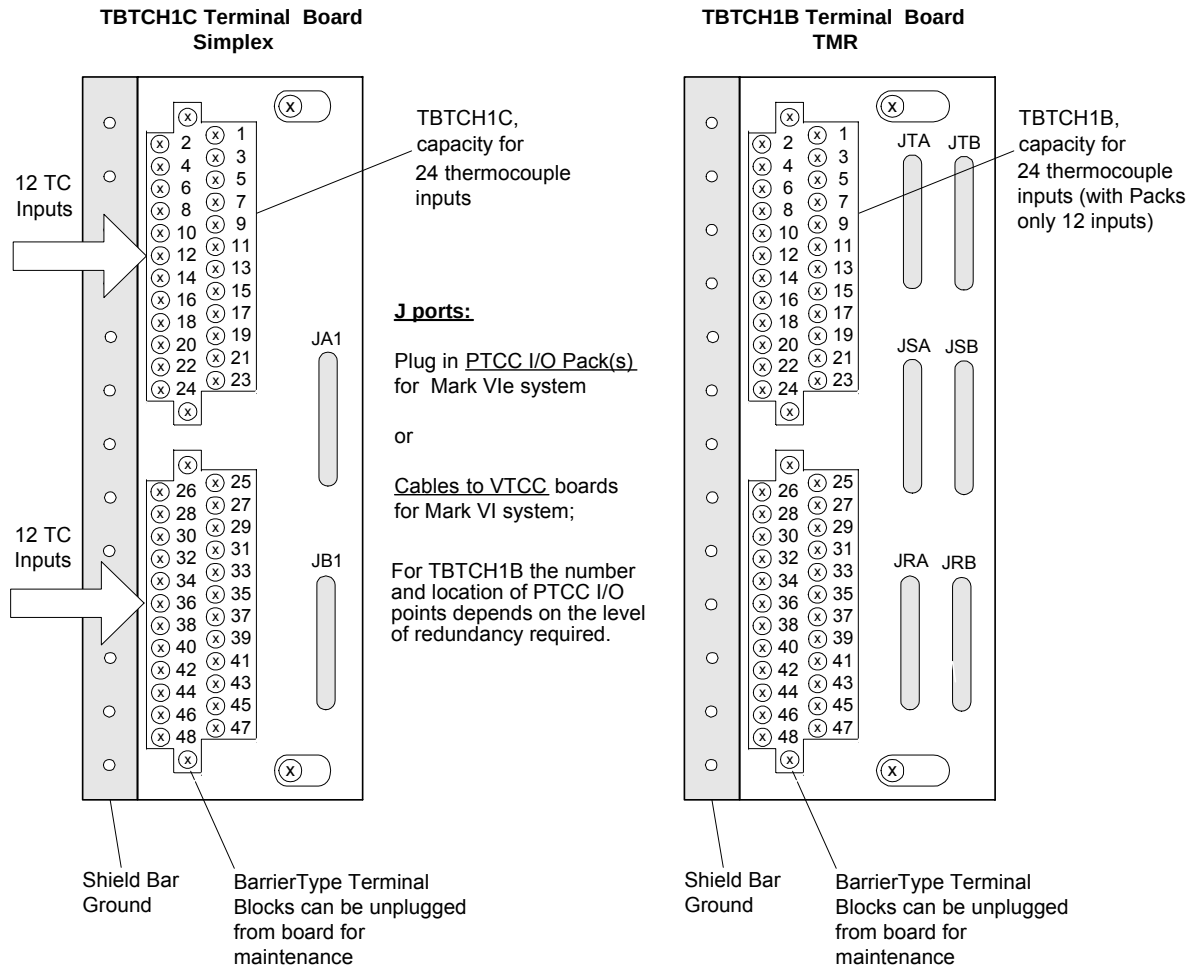
In the Mark VI system, TBTC works with the VTCC processor and supports simplex and TMR applications. One TBTC1C connects to the VTCC with two cables. In TMR systems, TBTC1B connects to three VTCC boards with six cables.

Mark VIe Systems

In the Mark VIe system, TBTC works with the PTCC I/O pack and supports simplex, dual, and TMR applications. In simplex systems, two PTCC packs plug into the TBTC1C for a total of 24 inputs. With the TBTC1B, one, two, or three PTCC packs can be connected, supporting a variety of system configurations.

- Simplex pack – 12 inputs
- Simplex packs – 24 inputs
- TMR packs – 12 inputs

The Thermocouple Input (TBTC) terminal board accepts 24-type E, J, K, S, or T thermocouple inputs for PTCCH1 pack and 24-type E, J, K, S,T,B,N or R thermocouple inputs for PTCCH2 pack.



Thermocouple Terminal Board, I/O Processor, and Cabling

Installation

Connect the thermocouple wires directly to the two I/O terminal blocks. These removable blocks are mounted on the terminal board and held down with two screws. Each block has 24 terminals accepting up to #12 AWG wires. A shield terminal strip attached to chassis ground is located on the left side of each terminal block.

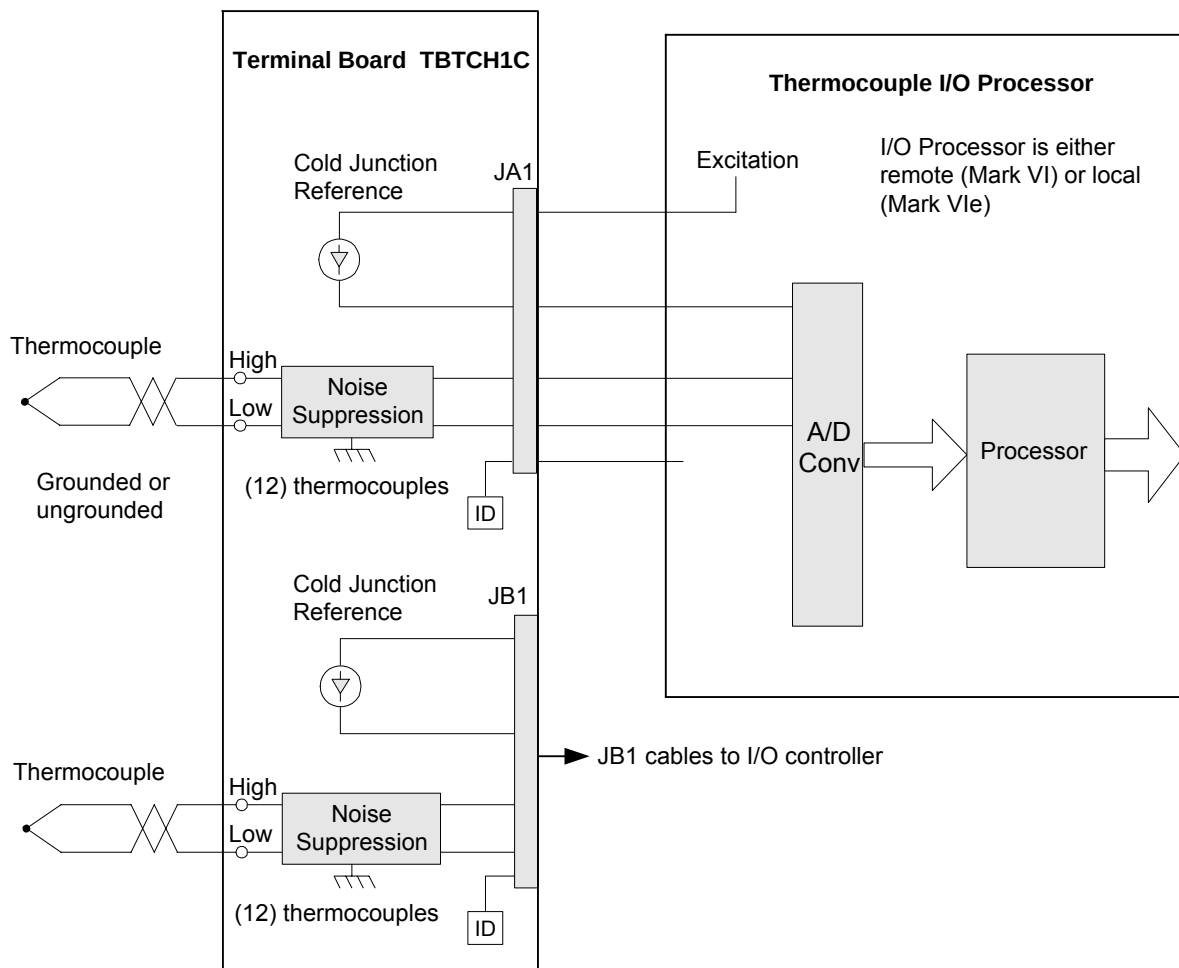
In Mark VI systems, cable the TBTC J-type connectors to the I/O processors in the VME rack.

In Mark VIe systems, plug the I/O packs directly into the TBTC J-type connectors. The number of cables or I/O packs depends on the level of redundancy required.

Operation

The 24 thermocouple inputs can be grounded or ungrounded. They can be located up to 300 m (984 ft) from the turbine control panel with a maximum two-way cable resistance of 450 Ω . TBTC features high-frequency noise suppression and two CJ reference devices, as shown in following figure. The I/O processor performs the analog-to-digital conversion and the linearization for individual thermocouple types.

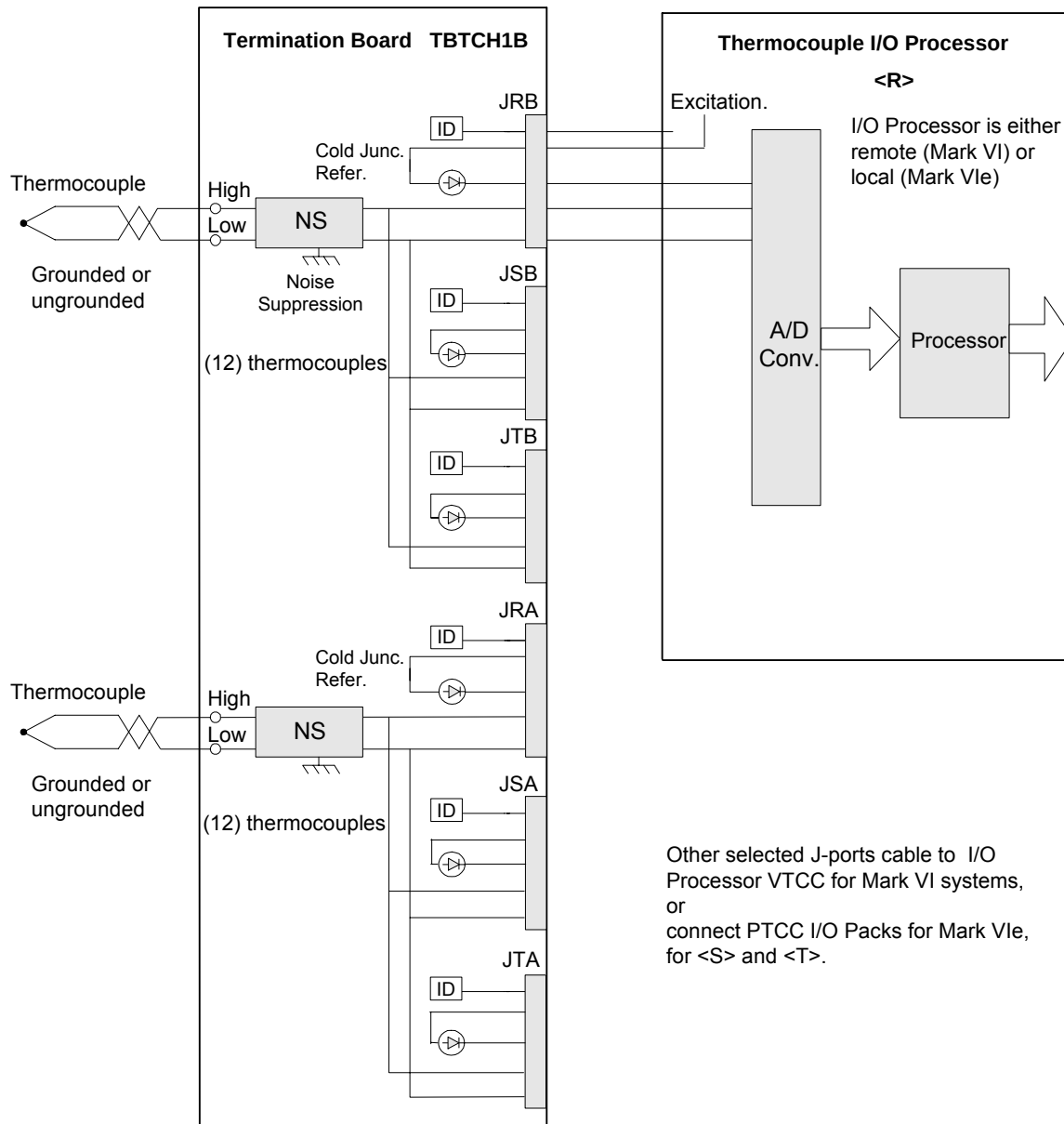
In Mark VI simplex systems using TBTC1C, one VTCC is used. In Mark VIe simplex systems, two PTCC packs plug into TBTC, obtaining 24 thermocouple inputs.



Thermocouple Inputs and I/O Processor, Simplex

For TMR systems using TBTC1B, the thermocouple signals fan out to three J-connectors. The Mark VI system accommodates 24 inputs and the Mark VIe system accommodates 12 inputs.

The TBTC terminal board supports all thermocouple spans documented for the associated thermocouple I/O processor.



Thermocouple Inputs and I/O Processor, TMR systems

Cold Junctions

The CJ signals go into signal space and are available for monitoring. Normally the average of the two is used. Acceptable limits are configured, and if a CJ goes outside the limit, a logic signal is set. A 1 °F error in the CJ compensation will cause a 1 °F error in the thermocouple reading.

Hard-coded limits are set at -40 to 85°C (-40 to +185 °F), and if a CJ goes outside this, it is regarded as bad. Most CJ failures are open or short circuit. If the CJ is declared bad, the backup value is used. This backup value can be derived from CJ readings on other terminal boards, or can be the configured default value (refer to signals in the section, *Configuration*).

Specifications

Item	Specification
Number of channels	24 channels per terminal board
Thermocouple types	E, J, K, S, T thermocouples, and mV inputs if TBTC is connected to PTCCH1 or VTCCH1 E, J, K, S, T, B, N, R thermocouples, and mV inputs if TBTC is connected to PTCCH2 or VTCCH2
Span	-8 mV to +45 mV if TBTC is connected to PTCCH1 or VTCCH1 -20 mV to +95 mV if TBTC is connected to PTCCH2 or VTCCH2
Cold junction compensation	Reference junction temperature measured at two locations on each H1C terminal board TMR H1B board has six CJ references. Only three available with Mark VIe I/O packs.
Cold junction temperature accuracy	CJ accuracy 1.1°C (2 °F)
Fault detection	High/low (hardware) limit check Monitor readings from all TCs, CJs, calibration voltages, and calibration zero readings.

Diagnostics

Diagnostic tests to components on the terminal boards are as follows:

- Each thermocouple type has hardware-limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If this limit is exceeded, a logic signal is set and the input is no longer scanned. If any one of the inputs hardware limits is set, it creates a composite diagnostic alarm.
- Each terminal board connector has its own ID device that is interrogated by the I/O board. The board ID is coded into a read-only chip containing the terminal board serial number, board type, revision number, and the J connector location. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O processor a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a low temperature reading should a thermocouple open.

DTTC Simplex Thermocouple Input

Functional Description

The Simplex Thermocouple Input (DTTC) terminal board is a compact terminal board designed for DIN-rail mounting. The board has 12 thermocouple inputs and connects to the VTCC thermocouple processor board with a single 37-pin cable. This cable is identical to the one used on the larger TBTC terminal board. The on-board signal conditioning and CJ reference are identical to those on the TBTC board.

Note An on-board ID chip identifies the board to the VTCC for system diagnostic purposes.

Two DTTC boards can be connected to the VTCC for a total of 24 inputs. High-density Euro-Block type terminal blocks are permanently mounted to the board with two screw connections for the ground connection (SCOM). Every third screw connection is for the shield. Only the simplex version of the board is available. The terminal boards can be stacked vertically on the DIN-rail to conserve cabinet space.

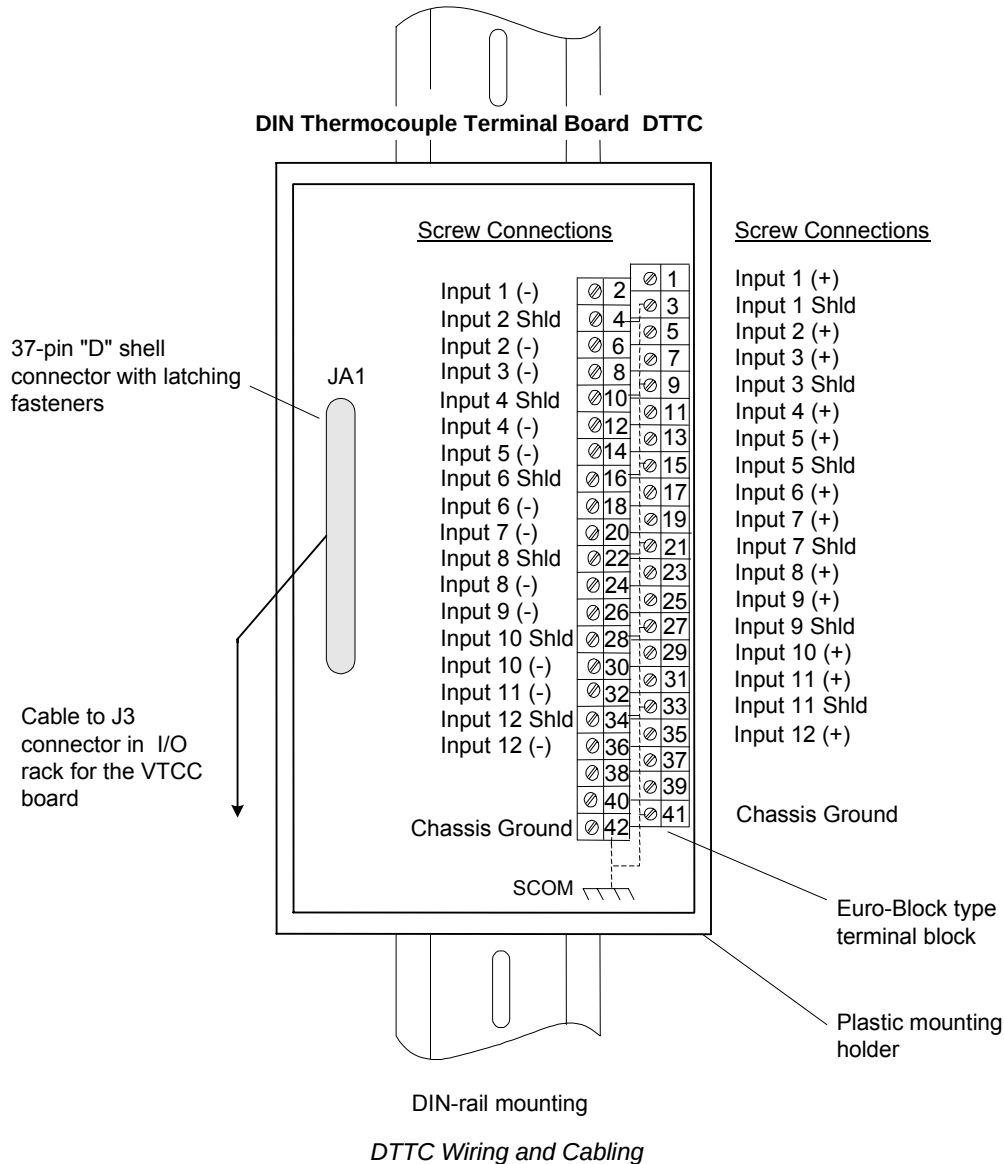
Note The DTTC board does not work with the PTCC I/O pack.

Installation

Note Shield screws are provided on this board and are internally connected to SCOM.

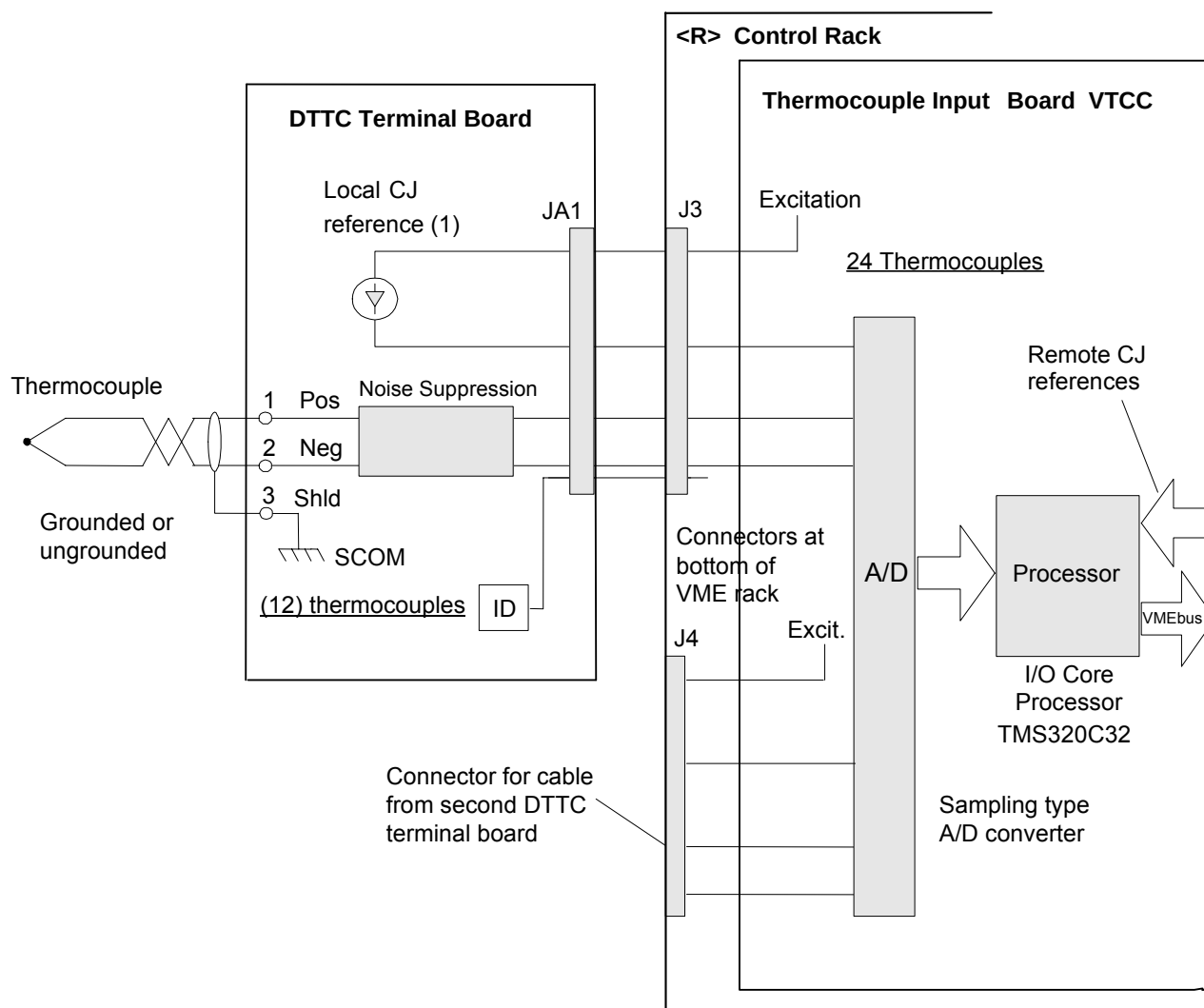
Mount the plastic holder on the DIN-rail and slide the DTTC board into place. Connect the thermocouples wires directly to the terminal block. The Euro-Block type terminal block has 42 terminals and is permanently mounted on the terminal board. Typically #18 AWG wires are used. Two screws, 41 and 42, are provided for the SCOM (ground) connection, which should be as short a distance as possible.

Note SCOM must be connected to ground.



Operation

VTCC provides excitation for the CJ reference on DTTC. The 12 thermocouple signals, the CJ signal, and the connection to the identity chip (ID) come through connector JA1 and are cabled to the VME control rack R. The following figure shows DTTC connected to VTCC, which contains the A/D converter.



DTTC and VTCC for Thermocouple Inputs

Specifications

Item	Specification
Number of Channels	12 channels per terminal board
Cold junction compensation	Reference junction temperature measured at one location
Cold junction temperature accuracy	CJ accuracy 1.1°C (2 °F)
Fault detection	High/low (hardware) limit check. Check ID chip on J3 connector.

Diagnostics

Diagnostic tests are made on the terminal board as follows:

- Each thermocouple type has hardware limit checking based on preset (non-configurable) high and low levels set near the ends of the operating range. If VTCC finds this limit is exceeded a logic signal is set and the input is no longer scanned. If any one of the input hardware limits is set it creates a composite diagnostic alarm, L3DIAG_VTCC, referring to the entire board.
- Each terminal board cable has its own ID device that is interrogated by VTCC. The board ID is coded into a read-only chip containing the terminal board serial number, board type, and revision number. If a mismatch is encountered, a hardware incompatibility fault is created.
- When operating with the I/O processor a very small current is injected into each thermocouple path. This is done to detect open circuits and is of a polarity to create a high temperature reading should a thermocouple open.

Details of the individual diagnostics are available from the toolbox. The diagnostic signals can be individually latched, and then reset with the RESET_DIA signal.

Configuration

There are no jumpers or hardware settings on the board.

VTUR Turbine Specific Primary Trip

VTUR Primary Turbine Protection

Functional Description

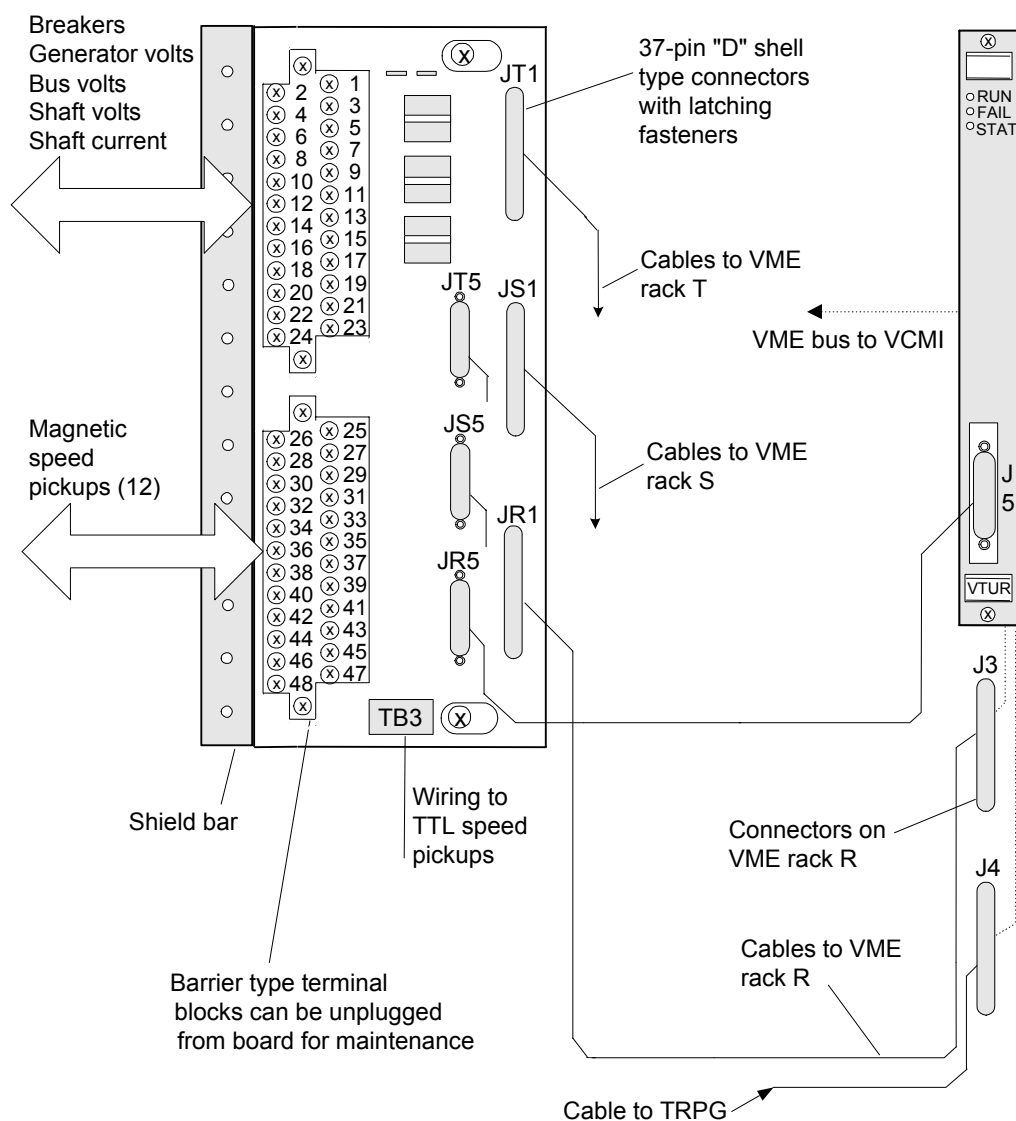
The Primary Turbine Protection (VTUR) board, has the following functions:

- Measures the turbine speed with four passive pulse rate devices and passes the signal to the controller, which generates the primary overspeed trip
- Provides automatic generator synchronizing and closes the main breaker
- Monitors induced shaft voltage and current
- Monitors eight Geiger-Mueller[®] flame detectors on gas turbine applications. The detectors connect to TRPG and use 335 V dc, 0.5 mA from an external supply.
- Controls three primary overspeed trip relays on the TRPx terminal board. The controller generates the trip signal, which is sent to VTUR and then to TRPx to trip the emergency solenoids. The turbine overspeed trip can come from VTUR or VPRO. TRPx contains nine magnetic relays to interface with three trip solenoids, known as the electrical trip devices (ETD). Nine relays are used in TMR systems, three in simplex systems.

Board Versions

There are two board versions as follows:

- VTURH1 drives three trip solenoids using one TRPx board and accepts eight flame detectors
- VTURH2 is a two-slot version that drives six trip solenoids using two TRPx boards, but only accepts eight flame detectors



VTUR Turbine Control Board, Terminal Boards, and Cabling

Installation

➤ To install the V-type board

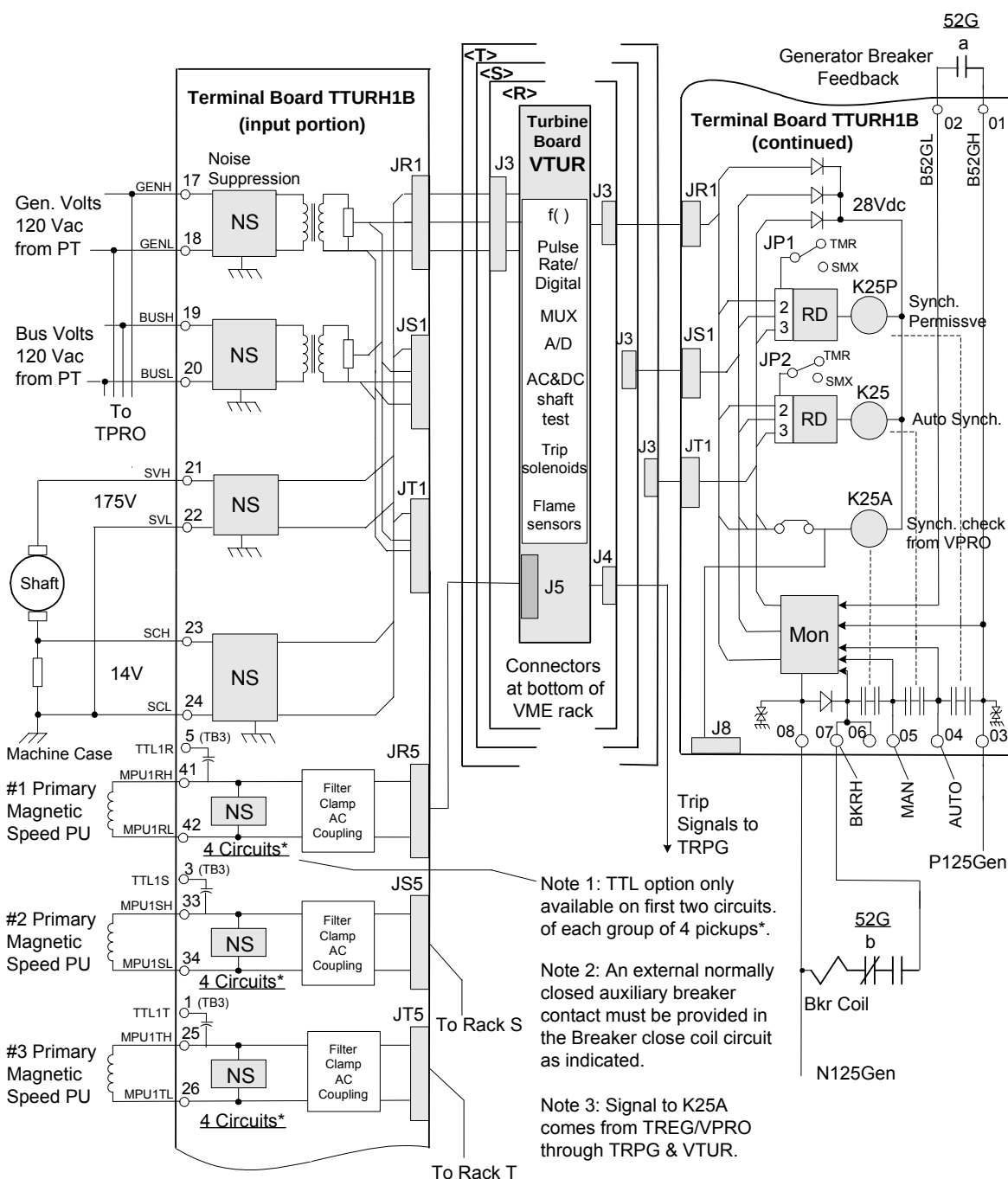
- 1 Power down the VME processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel

Note Cable connections to the terminal boards are made at the J3 connector on the lower portion of the VME rack. These are latching type connectors to secure the cables. Cable connection to the J5 connector on TTUR is made from J5 on the front panel. The cable to TRPG connects at J4. Power up the VME rack and check the diagnostic lights at the top of the front panel, for details refer to the section on diagnostics in this document.

In simplex applications, up to four pulse rate signals can be used to measure turbine speed. Generator and bus voltages are brought into VTUR for automatic synchronizing in conjunction with the turbine controller and excitation system. TTUR has permissive generator synchronizing relays and controls the main breaker relay coil 52G. Shaft voltage is picked up with brushes and monitored along with the current to the machine case.

The following figures show the VTUR simplex and TMR turbine speed inputs and generator synchronizing circuits.





VTUR Turbine Speed Inputs and Generator Synchronizing, TMR

Speed Pickups

Note The median speed signal is used for speed control and for the primary overspeed trip signal.

VTUR interfaces with four passive, magnetic speed inputs with a frequency range of 2 to 20,000 Hz. Using passive pickups on a sixty-tooth wheel, circuit sensitivity allows detection of 2-RPM turning gear speed to determine if the turbine is stopped (zero speed). If automatic turning gear engagement is provided in the turbine control, this signal initiates turning gear operation.

The primary overspeed trip calculations are performed in the controller using algorithms similar to (but not the same as) those in the VPRO protection board. The fast trip option used on gas turbines runs in VTUR.

Primary Trip Solenoid Interface

The normal primary overspeed trip is calculated in the controller and passed to the VTUR and then to the chosen primary trip terminal board. TRPx contains relays to interface with the ETDs. TRPx typically works in conjunction with an emergency trip board (TREx) to form the primary and emergency sides of the interface to the ETDs. VTUR supports up to three ETDs driven from each TRPx/TREx combination.

VTUR supports the following trip boards:

- TRPG is targeted at gas turbine applications and works in conjunction with the TREG board for emergency trip.
- TRPS is used for small and medium size steam turbine systems and works in conjunction with the TRES board for emergency trip.
- TRPL is intended for large steam turbine systems and works in conjunction with the TREL board for emergency trip.

Note Additional trip boards are being developed for other specific applications.

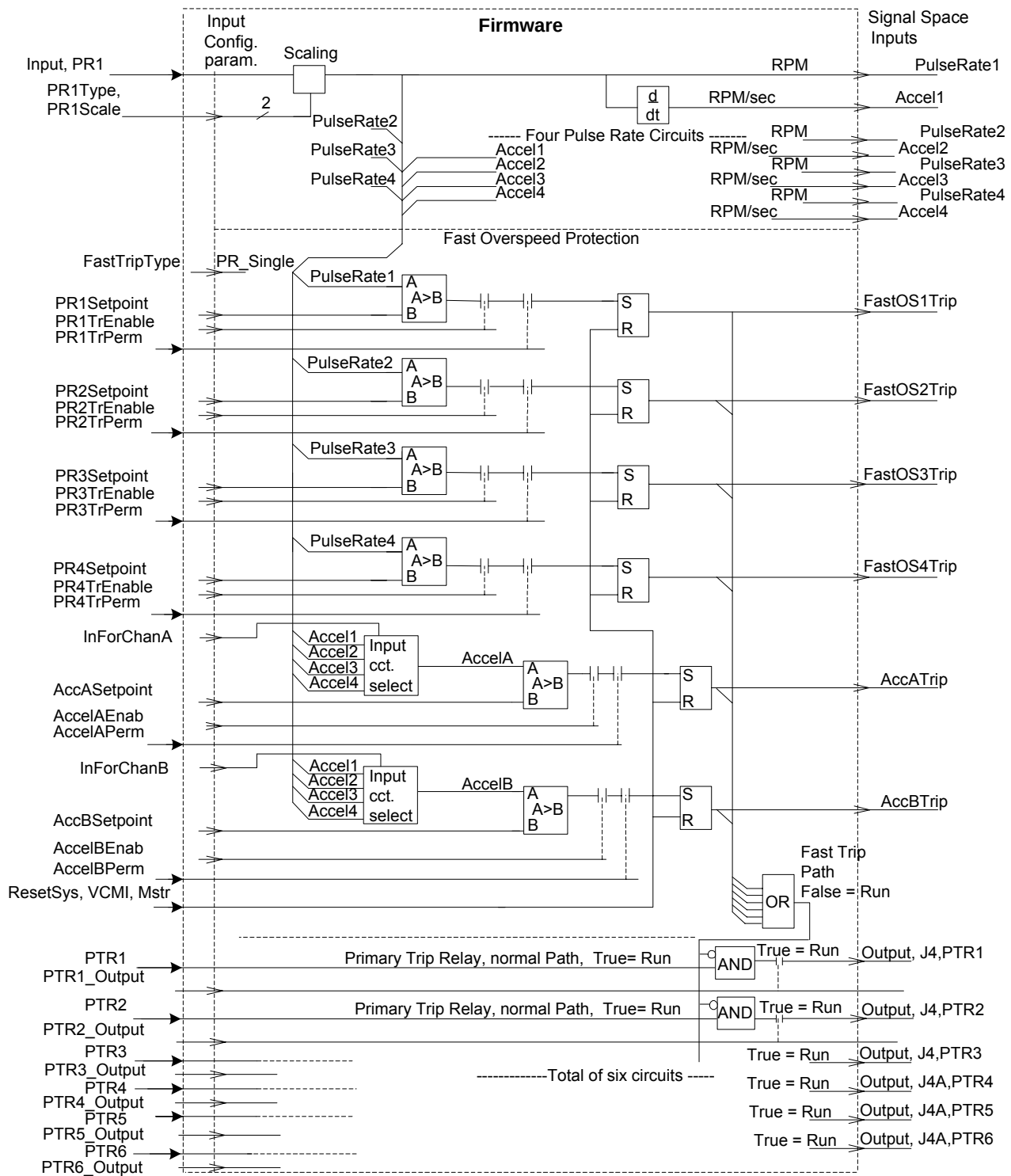
To support trip board operation, VTUR provides discrete inputs used to monitor signals such as trip relay position, synchronizing relay coil drive, and ETD power status.

Fast Overspeed Trip

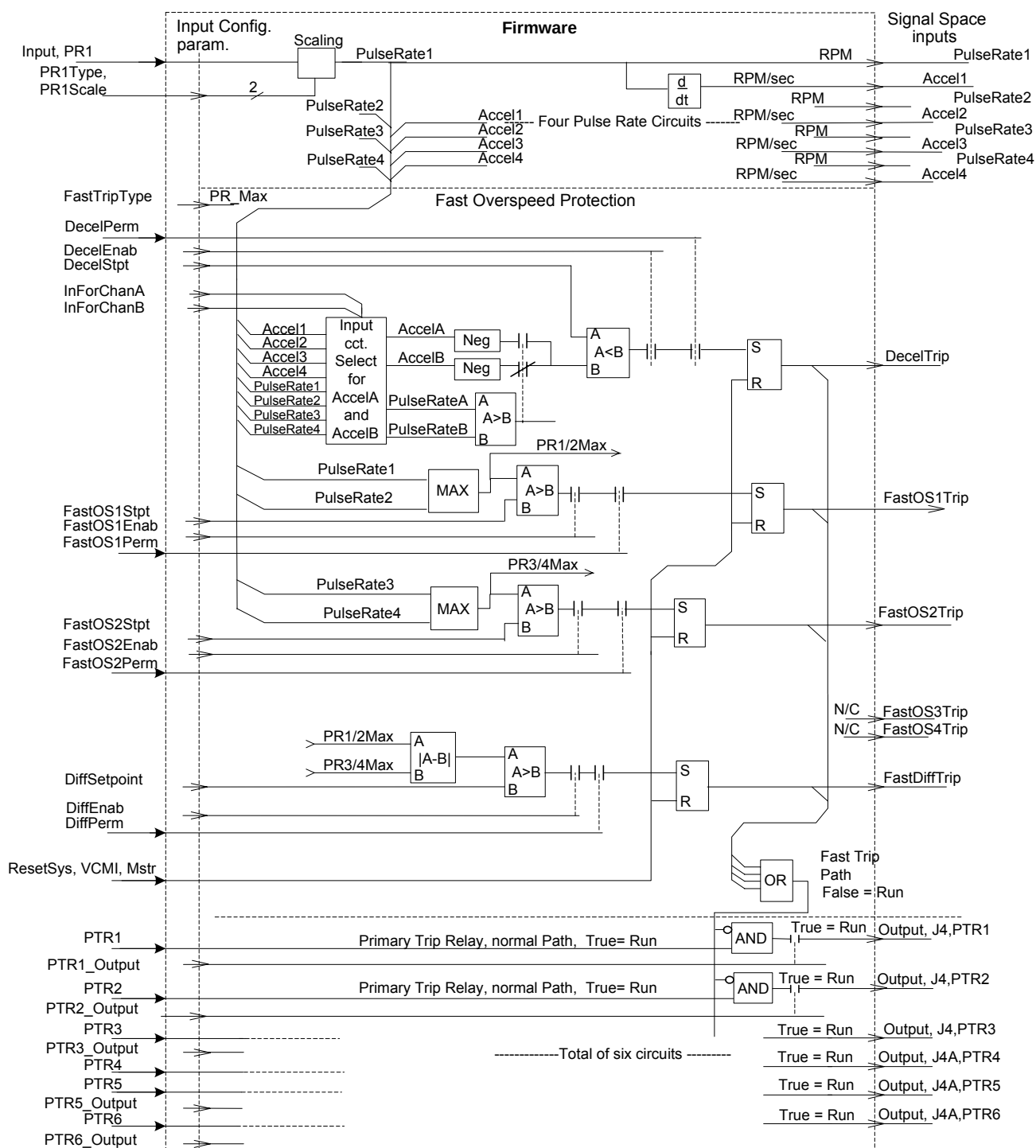
In special cases where a faster overspeed trip system is required, the VTUR Fast Overspeed Trip algorithms can be enabled. The system employs a speed measurement algorithm using a calculation for a predetermined tooth wheel. Two overspeed algorithms are available as follows:

- **PR_Single** uses two redundant VTURs by splitting up the two redundant PR transducers, one to each board. PR_Single provides redundancy and is the preferred algorithm for LM gas turbines.
- **PR_Max** uses one VTUR connected to the two redundant PR transducers. PR_Max allows broken shaft and deceleration protection without the risk of a nuisance trip if one transducer is lost.

The fast trips are linked to the output trip relays with an OR-gate. VTUR computes the overspeed trip instead of the controller, so the trip is very fast. The time from the overspeed input to the completed relay dropout is 30 ms or less.



Fast Overspeed Algorithm, PR-Single



Fast Overspeed Algorithm, PR-Max

Shaft Voltage and Current Monitor

Bearings can be damaged by the flow of electrical current from the shaft to the case. This current can occur for several reasons:

- A static voltage can be caused by droplets of water being thrown off the last stage buckets in a steam turbine. This voltage builds up until a discharge occurs through the bearing oil film.
- An ac ripple on the dc generator field can produce an ac voltage on the shaft with respect to ground through the capacitance of the field winding and insulation. Note that both of these sources are weak, so high impedance instrumentation is used to measure these voltages with respect to ground.
- A voltage can be generated between the ends of the generator shaft due to dissymmetries in the generator magnetic circuits. If the insulated bearings on the generator shaft breakdown, the current flows from one end of the shaft through the bearings and frame to the other end. Brushes can be used to discharge damaging voltage buildup, and a shunt should be used to monitor the current flow.

The turbine control continuously monitors the shaft to ground voltage and current, and alarms excessive levels. There is an ac test mode and a dc test mode. The ac test applies an ac voltage to test the integrity of the measuring circuit. The dc test checks the continuity of the external circuit, including the brushes, turbine shaft, and the interconnecting wire.

Note The dc test is driven from the R controller only. If the R controller is down, this test cannot be run successfully.

Flame Detectors

When used with TRPG, VTUR monitors signals from eight Geiger-Mueller flame detectors. With no flame present, the detector charges up to the supply voltage. The presence of the flame causes the detector to charge to a level and then discharge through TRPG. As the flame intensity increases the discharge frequency increases. When the detector discharges, VTUR and TRPG convert the discharged energy into a voltage pulse. The pulse rate varies from 0 to 1,000 pulses/sec. These voltage pulses are fanned out to all three modules. Voltage pulses above 2.5 V generate a logic high, and the pulse rate over a 40 ms time period is measured in a counter.

Automatic Synchronizing

All synchronizing connections are located on the TTUR terminal board. The generator and bus voltages are provided by two, single phase, potential transformers (PTs) with a fused secondary output supplying a nominal 115 V rms. Measurement accuracy between the zero crossing for the bus and generator voltage circuits is 1 degree.

Turbine speed is matched against the bus frequency. The generator and bus voltages are matched by adjusting the generator field excitation voltage from commands sent between the turbine controller and the EX2000 over the Unit Data Highway (UDH). A command is given to close the breaker when all permissions are satisfied. The breaker is predicted to close within the calculated phase/slip window. Feedback of the actual breaker closing time is provided by a 52G/a contact from the generator breaker (not an auxiliary relay) to update the database. An internal K25A sync check relay is provided on the TTUR; the independent backup phase/slip calculation for this relay is performed in the <P> protection module. Diagnostics monitor the relay coil and contact closures to determine if the relay properly energizes or de-energizes upon command.

Synchronizing Modes

There are three basic synchronizing modes. Traditionally, these modes are selected from a generator panel mounted selector switch:

- **Off** The breaker cannot be closed by the controller. The check relay will not pick up.
- **Manual** The operator initiates breaker close, which is still subject to the K25A Sync Check contacts driven by the VPRO. The manual close is initiated from an external contact on the generator panel, normally connected in series with a sync mode in manual contact.
- **Auto** The system automatically matches voltage and speed, and then closes the breaker at the right time to hit top dead center on the synchroscope. All three of the following functions must agree for this closure to occur:

K25A - sync check relay, checks the allowable slip/phase window, from VPRO

K25 - auto sync relay, provides precision synchronization, from VTUR

K25P - sync sequence permissive, checks the turbine sequence status, from VTUR

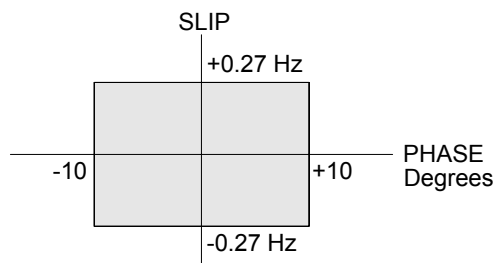
The K25A relay should close before the K25 or else the sync check function will interfere with the auto sync optimizing. If this sequence is not executed, a diagnostic alarm is posted, a lockout signal is set true in signal space, and the application code may prevent any further attempts to synchronize until a reset is issued and the correct coordination is set up. Details of the various checks are discussed in the following sections.

Sync Check

The K25A sync check function is based on phase lock loop techniques. The VPRO performs the calculations for this function, but interfaces to the breaker close circuit are located on the TTUR board, not TPRO. Limit checks are performed against adjustable constants as follows:

- Generator under-voltage
- Bus under-voltage
- Voltage error
- Frequency error (slip), with a maximum value of 0.33 Hz, typically set to 0.27 Hz
- Phase error with a maximum value of 30 °, typically set to 10 °.

In addition, sync check arms logic to enable the function, and provides bypass logic for deadbus closure. The sync window below is based on typical settings:

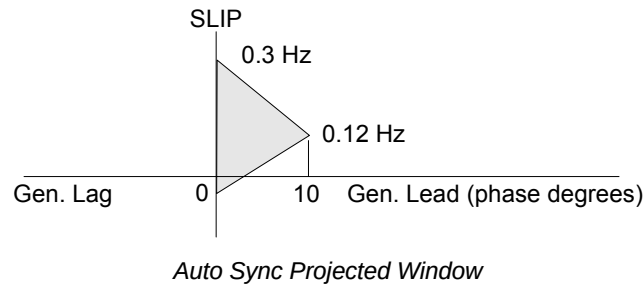


Typical Sync Window

Auto Sync

The Auto Sync K25 function uses zero voltage crossing techniques. It compensates for the breaker time delay, which is defined by two adjustable constants with logic selection between the two (for two breaker applications). VTUR performs the calculations for phase, slip, acceleration, and anticipated time lead for the breaker delay. The time delay parameter is adjusted (up to certain limits) based on the measured breaker close time.

In addition, auto sync arms logic to enable the function, and bypasses logic to provide for deadbus or manual closure. The auto sync projected sync window is shown below, where positive slip indicates that the generator frequency is higher than the bus frequency.



The projected window is based on current phase, current slip, and current acceleration. The generator must currently be lagging and have been lagging for the last 10 consecutive cycles, and projected (anticipated) to be leading when the breaker actually reaches closure. Auto sync does not allow the breaker to close with negative slip; speed matching typically aims at around + 0.12 Hz slip.

Synchronization Display

A special synchronization screen is available on the HMI with a real-time graphical phase display and control pushbutton. The display items are listed in table.

Sync Display	Description
Dynamic Parameters	Voltages: Generator, Bus, Difference
	Frequencies: Generator, Bus, Slip (difference)
	Phase: Difference angle, degrees
Status Indication	Mode: Sync OFF, MANUAL, AUTO
	Sync Monitor: OFF, ON
	Dead bus breaker: Open/close
	Second breaker if applicable: Open/close
	Sync permissive: K25P
	Auto sync enabled
	Speed adjust: Raise/lower
	Voltage adjust: Raise/lower

Sync Display	Description
Sync Permissive	Gen voltage: OK/not OK Bus voltage: OK/not OK Gen frequency: OK/not OK Bus frequency: OK/not OK Difference volts: OK/not OK Difference frequ:OK/not OK Phase: K25, OK/not OK K25A, OK/not OK
Limit Constants	Upper and lower limits for the above permissive
Breaker Performance	Diagnostics: Slow check relay Sync relay lockup Breaker #1 close time out of limits Breaker #2 close time out of limits Relay K25P trouble Breaker closing voltage (125 V dc) missing
Control Pushbuttons	Sync monitor: ON, OFF Speed adjust: RAISE, LOWER Voltage adjust:RAISE, LOWER

Specifications

Item	Specification
Number of inputs	4 passive speed pickups 1 shaft voltage and 1 current measurement 1 generator and 1 bus voltage Generator breaker status 8 flame detectors from first TRPG
Number of outputs	Synch permissive and Auto synch relays. Primary trip solenoid interface, 3 outputs to TRPx Additional 3 trip outputs from second TRPx using VTURH2
MPU pulse rate range	2 Hz to 20 kHz
MPU pulse rate accuracy	0.05% of reading
MPU input circuit sensitivity	27 mV pk (detects 2 rpm speed)
Shaft voltage monitor	Signal is frequency of ± 5 V dc (0 – 1 MHz) pulses from 0 to 2,000 Hz
Shaft voltage wiring	Up to 300 m (984 ft), with maximum two-way cable resistance of 15 Ω
Shaft voltage dc test	Applies a 5 V dc source to test integrity of the external turbine circuit and measures dc current flow. Circuit computes a differential resistance between 0 and 150 Ω within ± 5 Ω and compares against shunt limit and brush limit. Readings above 50 Ω indicate a fault. Return signal is filtered to provide 40 dB of noise attenuation at 60 Hz.
Shaft voltage ac test	Applies a test voltage of 1 kHz to the input of the VTUR shaft voltage circuit (R module only). Shaft voltage monitor circuit on R, S, and T displays an offset of 1000 Hz from normal reading.
Shaft current input	Measures shaft current in amps ac (shunt voltage up to 0.1 V pp)
Generator and bus voltage sensors	Two single phase potential transformers, with secondary output supplying a nominal 115 V rms Each input has less than 3 VA of loading Allowable voltage range for synch is 75 to 130 V rms Each PT input is magnetically isolated with a 1,500 V rms barrier Cable length can be up to 1,000 ft. of 18 AWG wiring

Item	Specification
Synchronizing measurements	Frequency accuracy 0.05% over 45 to 66 Hz range Zero crossing of the inputs is monitored on the rising slope Phase difference measurement is better than ± 1 degree
Contact voltage sensing	20 V dc indicates high and 6 V dc indicates low Each circuit is optically isolated and filtered for 4 ms
Trip solenoids	6 per VTURH2 (3 per TRPx terminal board) 3 per VTURH1
Flame detectors	8 per VTUR

Diagnostics

Three LEDs at the top of the VTUR front panel provide status information. The normal RUN condition is a flashing green, FAIL is a solid red. The third LED is STATUS and is normally off but shows a steady orange if a diagnostic alarm condition exists in the board. VTUR makes diagnostic checks including:

- If feedback from the solenoid relay drivers differs with the control signal a fault is created
- If feedback from the relay contacts differs with the control signal a fault is created
- Loss of solenoid power creates a fault
- High and low flame detector voltage creates a fault
- Slow synch check relay, slow auto synch relay, and locked up K25 relay; all of these condition creates a fault
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VTUR occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy
- Terminal board connectors JR1, JS1, JT1, JR5, JS5, JT5 have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VTUR and a mismatch is encountered, a hardware incompatibility fault is created

Configuration

Note The following information is extracted from the toolbox and represents a sample of the configuration information for this board. Refer to the actual configuration file within the toolbox for specific information.

Parameter	Description	Choices
Configuration		
VTUR system limits	Select system limits	Enable, disable
SMredundancy	Select Simplex or TMR system	Simplex or TMR
AccelCalType	Select acceleration calculation type	Slow, medium, fast
FastTripType	Select Fast Trip algorithm	Unused, PR_Single, PR_Max
J3J5:IS200TTURH1A	TTUR connected to VTUR through J3 and J5	Connected, not connected
PulseRate1	Pulse rate input 1 - board point	Point edit (input FLOAT)
PRType	Select Speed or Flow type input	Unused, speed, flow, Speed_LM
PRScale	Select pulses per revolution	0 to 1,000
SysLim1Enable	Select system limit 1	Enable, disable
SysLim1Latch	Select whether alarm will latch	Latch, not latch

Parameter	Description	Choices
SysLim1Type	Select type of alarm initiation	>= or <=
SysLimit1	Select alarm level in GPM or RPM	0 to 20,000
SysLim2Enable	Select system limit 2 (as above)	Enable, disable
TMRDiffLimit	Difference limit for voted PR inputs EU	0 to 20,000
ShVoltMon	Shaft voltage monitor - board point	Point edit (input FLOAT)
SysLim1Enable	Select System Limit 1	Enable, disable
SysLim1Latch	Select whether alarm will latch	Latch, not latch
SysLim1Type	Select type of alarm initiation	>= or <=
SysLimit1	Select alarm level in frequency	0 to 100
SysLim2Enable	Select system limit 2 (as above)	Enable, disable
ShCurrMon	Shaft current monitor - board point	Point edit (input FLOAT)
ShuntOhms	Shunt resistance	0 to 100
Shunt limit	Shunt maximum ohms	0 to 100
Brush limit	Shaft brush maximum ohms	0 to 100
SysLim1Enable	Select system limit 1	Enable, disable
SysLim1Latch	Select whether alarm will latch	Latch, not latch
SysLim1Type	Select type of alarm initiation	>= or <=
SysLimit1	Select alarm level in amps	0 to 100
SysLim2Enable	Select system limit 2	Enable, disable
GenPT_KVolts	Generator potential transformer - board point	Point edit (input FLOAT)
PT_Input	PT input in kVrms for PT output	0 to 1,000
PT_Output	PT output in Vrms, nominal 115 V rms	0 to 150
SysLim1	Select alarm level in kVrms	0 to 1,000
SysLim2	Select alarm level in kVrms	0 to 1,000
BusPT_Kvolts	Bus potential transformer - board point	Point edit (input FLOAT)
Ckt_Bkr	Circuit breaker - board point	Point edit (input BIT)
System Frequency	Select frequency in Hz	50 or 60
CB1CloseTime	Breaker 1 closing time, ms	0 to 1,000
CB1 AdaptLimit	Breaker 1 self adaptive limit, ms	0 to 1,000
CB1 AdaptEnabl	Select breaker 1 self adaptive limit	Enable, disable
CB1FreqDiff	Breaker 1 special window frequency difference, Hz	0 to 10
CB1PhaseDiff	Breaker 1 special window phase difference, degrees	0 to 30
CB2CloseTime	Breaker 2 closing time, ms (as above)	0 to 1,000
J4:IS200TRPGH1A	TRPG terminal board, 8 flame detectors	Connected, not connected

Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VTUR1	Board diagnostic	Input	BIT
L3DIAG_VTUR2	Board diagnostic	Input	BIT
L3DIAG_VTUR3	Board diagnostic	Input	BIT
ShShntTst_OK	Shaft voltage monitor shunt test OK	Input	BIT
ShBrshTst_OK	Shaft voltage brush test OK	Input	BIT
CB_Volts_OK	L3BKR_VLT circuit breaker coil voltage available	Input	BIT
CB_K25P_PU	L3BKR_PERM sync permissive relay picked up	Input	BIT
CB_K25_PU	L3KBR_GES auto sync relay picked up	Input	BIT
CB_K25A_PU	L3KBR_GEX sync check relay picked up	Input	BIT

Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
Gen_Sync_LO	Generator sync trouble (lockout)	Input	BIT
L25_Command	-----	Input	BIT
Kq1_Status	-----	Input	BIT
:	:	Input	BIT
Kq6_Status	-----	Input	BIT
FD1_Flame	-----	Input	BIT
:	:	Input	BIT
FD16_Flame	-----	Input	BIT
SysLim1PR1	-----	Input	BIT
:	:	Input	BIT
SysLim1PR4	-----	Input	BIT
SysLim1SHV	Ac shaft voltage frequency high L30TSVH	Input	BIT
SysLim1SHC	Ac shaft current high L30TSCH	Input	BIT
SysLim1GEN	-----	Input	BIT
SysLim1BUS	-----	Input	BIT
SysLim2PR1	(same set as for Limit1 above)	Input	BIT
GenFreq	Hz frequency	Input	FLOAT
BusFreq	Hz frequency	Input	FLOAT
GenVoltsDiff	KiloVolts rms-Gen Low is negative	Input	FLOAT
Gen Freq Diff	Slip Hz-Gen Slow is negative	Input	FLOAT
Gen Phase Diff	Phase Degrees-Gen Lag is negative	Input	FLOAT
CB1CloseTime	Breaker #1 close time in milliseconds	Input	FLOAT
CB2CloseTime	Breaker #2 close time in milliseconds	Input	FLOAT
Accel1	RPM/SEC	Input	FLOAT
:	:	Input	FLOAT
Accel4	RPM/SEC	Input	FLOAT
FImDetPwr1	335 V dc	Input	FLOAT
ShTestAC	L97SHAFT_AC SVM_AC_TEST	Output	BIT
ShTestDC	L97SHAFT_DC SVM_DC_TEST	Output	BIT
FD1_Level	1 = high detection counts level	Output	BIT
:	:	Output	BIT
FD16_Level	1 = high detection counts level	Output	BIT
Sync_Perm_AS	L83AS - auto sync permissive	Output	BIT
Sync_Perm	L25P - sequencing sync permissive	Output	BIT
Sync_Monitor	L83S_MTR - monitor mode	Output	BIT
Sync_Bypass1	L25_BYP-1 = auto aync bypass	Output	BIT
Sync_Bypass0	L25_BYPZ-0 = auto sync permissive	Output	BIT
CB2_Selected	L43SAUT2 - 2nd breaker selected	Output	BIT
AS_Win_Sel	L43AS_WIN - special window selected	Output	BIT
Sync_Reset	L86MR_SYNC - sync trouble reset	Output	BIT
Kq1	L20PTR1 - primary trip relay	Output	BIT
:	:	Output	BIT
Kq6	L20PTR6 - primary trip relay	Output	BIT

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board
30	ConfigCompatCode mismatch; Firmware: []; Tre:[] The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: []; Tre:[] The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32-37	Solenoid [] Relay Driver Feedback Incorrect. Solenoid (1-6) relay driver feedback is incorrect as compared to the command; VTUR cannot drive the relay correctly until the hardware failure is corrected	The solenoid relay driver on the TRPG/L/S board has failed, or the cabling between VTUR and TRPG/L/S is incorrect.
38-43	Solenoid [] Contact Feedback Incorrect. Solenoid (1-6) relay contact feedback is incorrect as compared to the command; VTUR cannot drive the relay correctly until the hardware failure is corrected	The solenoid relay driver or the solenoid relay on the TRPG/L/S board has failed, or the cabling between VTUR and TRPG/L/S is incorrect.
44-45	TRPG [] Solenoid Power Absent. P125/24 V dc power is not present on TRPG terminal board; VTUR cannot energize trip solenoids 1 through 3, or 4 through 6 until power is present	Power may not be coming into TRPG/L/S on the J1 connector, or the monitoring circuit on TRPG/L/S is bad, or the cabling between TRPG/L/S and VTUR is at fault.
46,48	TRPG [] Flame Detector Volts Low at Y Volts. TRPG 1 or 2 flame detect voltage is low; the ability to detect flame by detectors 1 through 8, or 9 through 16 is questionable	Power comes into TRPG through J3, J4, and J5. If the voltage is less than 314.9 V dc, this should be investigated. If the voltage is above this value, the monitoring circuitry on TRPG or the cabling between TRPG and VTUR is suspect.
47,49	TRPG [] Flame Detector Volts High at Y Volts. TRPG 1 or 2 flame detect voltage is high; the ability to detect flame by detectors 1 through 8, or 9 through 16 is questionable because the excitation voltage is too high and the devices may be damaged	This power comes into TRPG through J3, J4, and J5. If the voltage is greater than 355.1 V dc, this should be investigated. If the voltage is below this value, the monitoring circuitry on TRPG or the cabling between TRPG and VTUR is suspect.
50	L3BKRGSX – Synch Check Relay is Slow. The auto synchronization algorithm has detected that during synchronization with no dead bus closure (synch bypass was false) the auto synch relay I3BKRGES closed before synch relay I3BKRGEEX closed	The synch check relay I3BKRGSX, known as K25A, on TTUR is suspect; also the cabling between VTUR and TTUR may be at fault.

Fault	Fault Description	Possible Cause
51	L3BKRGES – Auto Synch Relay is Slow. The auto synchronization algorithm has detected that the auto synch relay I3BKRGES had not closed by two cycle times after the command I25 was given	The Auto synch relay I3BKRGES also known as K25, on TTUR is suspect; also the cabling between VTUR and TTUR may be at fault.
52-53	Breaker [] Slower than Adjustment Limit Allows. Breaker 1 or 2 close time was measured to be slower than the auto synch algorithms adaptive close time adjustment limit allows	The breaker is experiencing a problem, or the operator should consider changing the configuration (both nominal close time and self-adaptive limit in ms can be configured).
54	Synchronization Trouble - K25 Relay Locked Up. The auto synchronization algorithm has determined that the auto synch relay I3BKRGES, also known as K25, is locked up. Auto synch will not be possible until the relay is replaced	K25 on TTUR is most likely stuck closed, or the contacts are welded.
55	Card and Configuration File Incompatibility. You are attempting to install a VTUR board that is not compatible with the VTUR TRE file you have installed	Install the correct TRE file from the factory
56	Terminal Board on J5X and Config File Incompatibility. VTUR detects that the terminal board that is connected to it through J5 is different than the board that is configured	Check your configuration.
57	Terminal Board on J3 and Config File Incompatibility. VTUR detects that the terminal board that is connected to it through J3 is different than the board that is configured	Check your configuration.
58	Terminal Board on J4 and Config File Incompatibility. VTUR detects that the terminal board that is connected to it through J4 is different than the board that is configured	Check your configuration.
59	Terminal Board on J4A and Config File Incompatibility. VTUR detects that the terminal board that is connected to it through J4A is different than the board that is configured	Check your configuration.
60	Terminal Board TTUR and card VTUR Incompatibility. VTUR detects that the TTUR connected to it is an incompatible hardware revision	The TTUR or VTUR must be changed to a compatible combination.
61	TRPL or TRPS Solenoid Power Bus "A" Absent	Cabling problem or solenoid power source
62	TRPL or TRPS Solenoid Power Bus "B" Absent	Cabling problem or solenoid power source
63	TRPL or TRPS Solenoid Power Bus "C" Absent	Cabling problem or solenoid power source
64-66	TRPL/S J4 Solenoid [] Voltage mismatch. The voltage feedback disagrees with the PTR or ETR feedback	PTR or ETR relays, or defective feedback circuitry
128- 223	Logic Signal [] Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
224- 251	Input Signal [] Voting mismatch, Local [], Voted []. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TTURH1B Primary Turbine Protection Input

Functional Description

The Primary Turbine Protection Input (TTURH1B) terminal board works with VTUR and has the following inputs and outputs:

- Twelve passive pulse rate devices sensing a toothed wheel to measure the turbine speed
- Generator voltage and bus voltage signals from potential transformers
- 125 V dc output to the main breaker coil for automatic generator synchronizing
- Inputs from the shaft voltage and current sensors to measure induced shaft voltage and current

TTUR has three relays, K25, K25P, and K25A, that all have to close to provide 125 V dc power to close the main breaker, 52G. The speed signal cable to VTUR uses the JR5 connector, and the other signals use the JR1 connector. For TMR systems, signals fan out to the JR5, JS5, JT5, JR1, JS1, and JT1 connectors.

Mark VI Systems

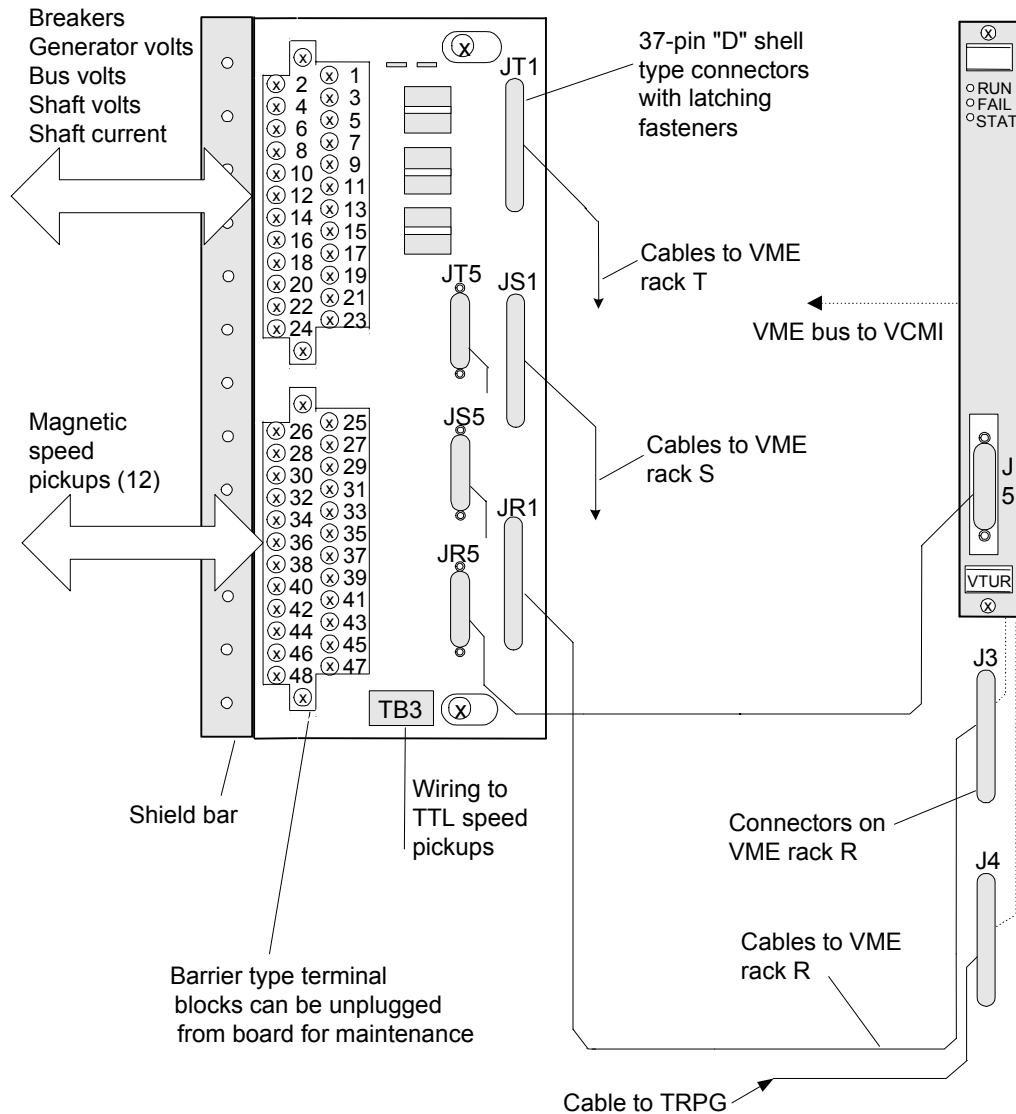
In the Mark* VI system, the TTUR works with the VTUR processor and supports simplex and TMR applications. In TMR systems, TTURH1B connects to three VTUR boards.

Note TTURH1B does not support I/O packs, see Mark VIe below.

Mark VIe Systems

For the Mark VIe system, a new design board, the TTURH1C, is used.

Note This document does not describe TTURH1C. For details, refer to *GEI-100575 PTUR Turbine Specific Primary Trip*.



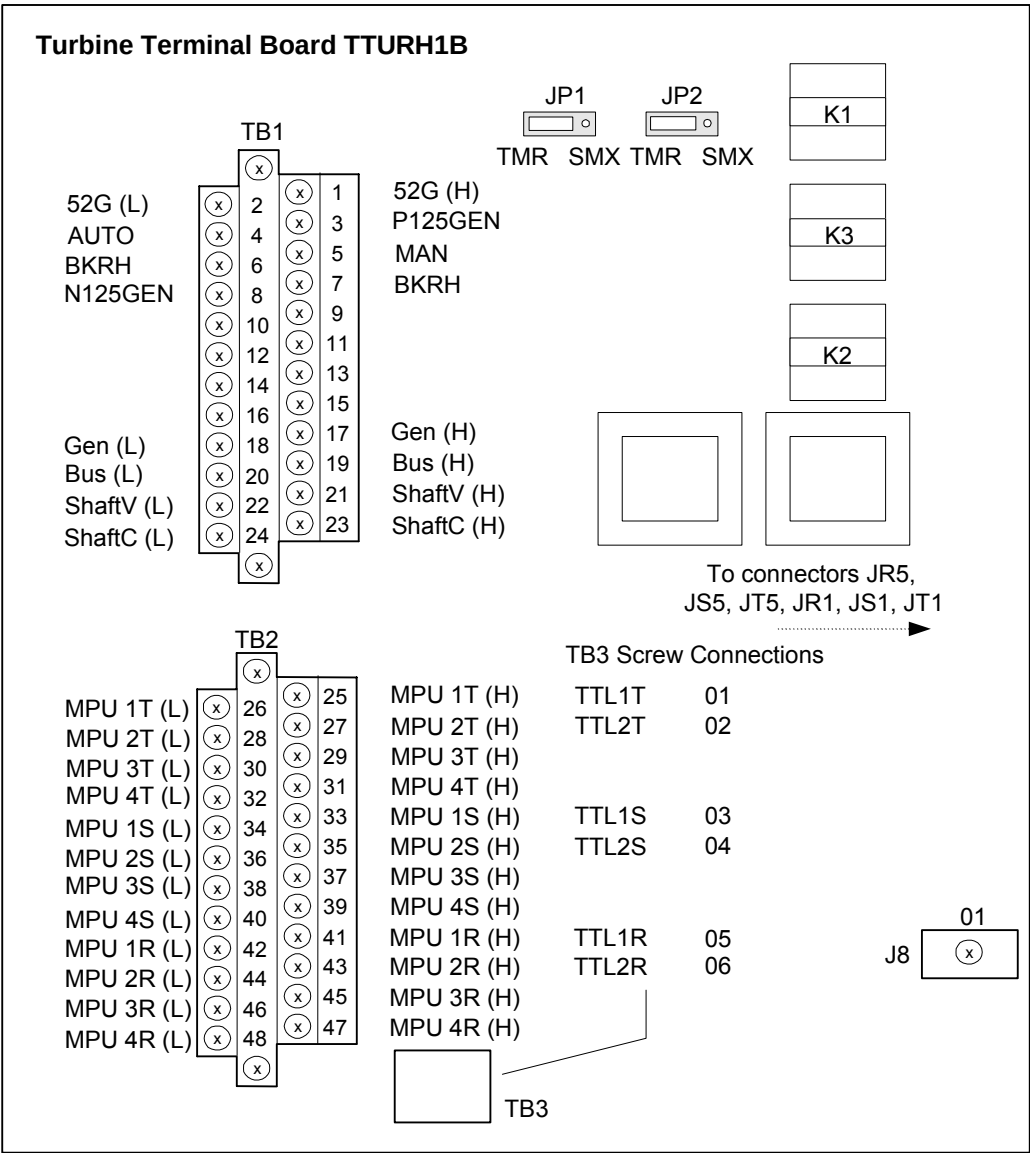
TTUR Turbine Terminal Board, Processor Board, and Cabling

Installation

Connect the wires for the magnetic pick ups, shaft pick ups, potential transformers, and breaker relays to the two I/O terminal blocks TB1 and TB2, as shown in the figure, *TTUR Terminal Board Wiring*. Each block is held down with two screws and has 24 terminals accepting up to #12 AWG wires. A shield termination strip attached to chassis ground is located immediately to the left of each terminal block.

Use jumpers JP1 and JP2 to select either SMX or TMR for relay drivers K25 and K25P. If used, connect the wires for optional TTL active speed pick ups to TB3; these require an external power supply.

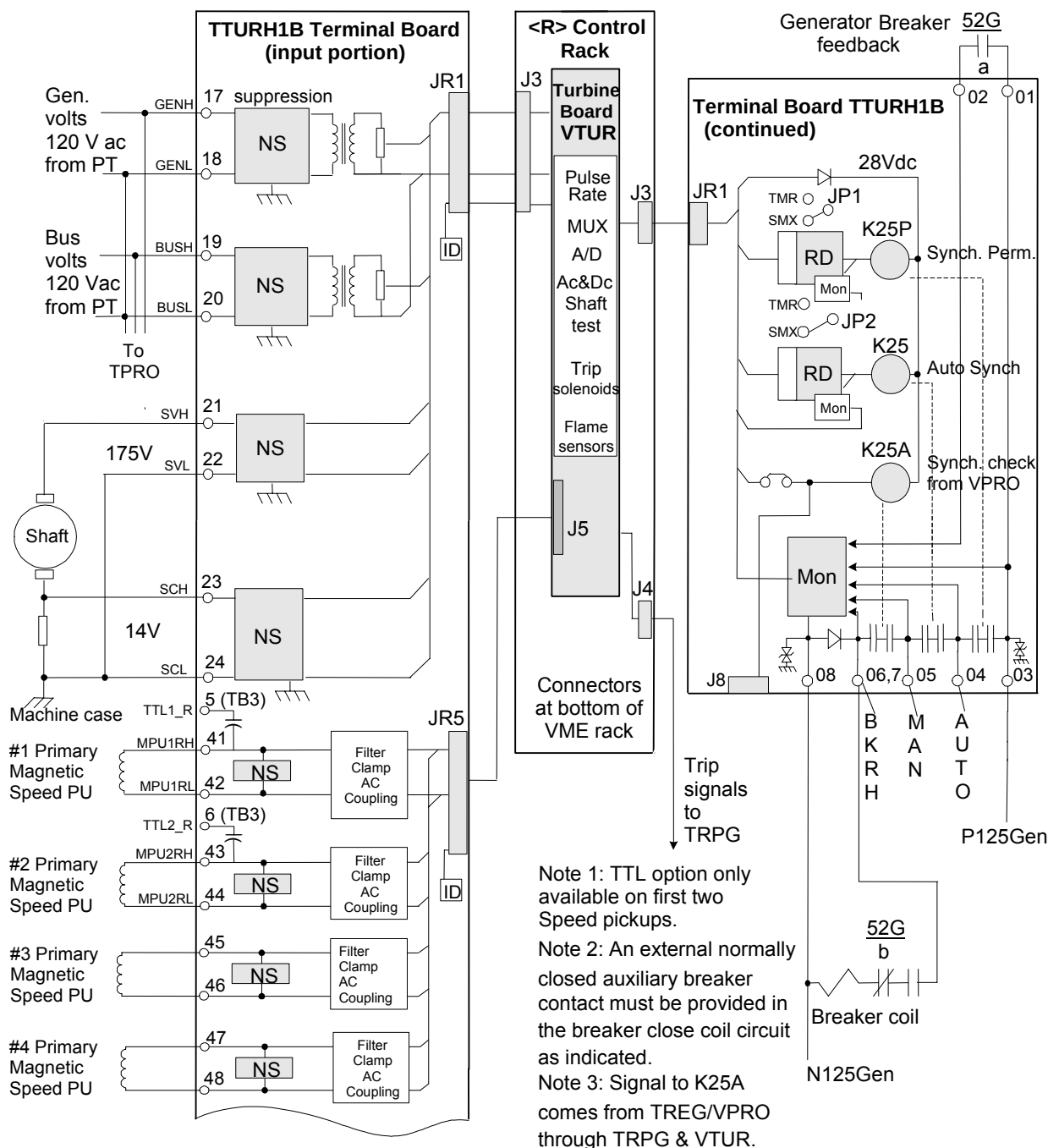
Simplex systems use cable connectors JR5 and JR1. TMR systems use all six cable connectors.



TTUR Terminal Board Wiring

Operation

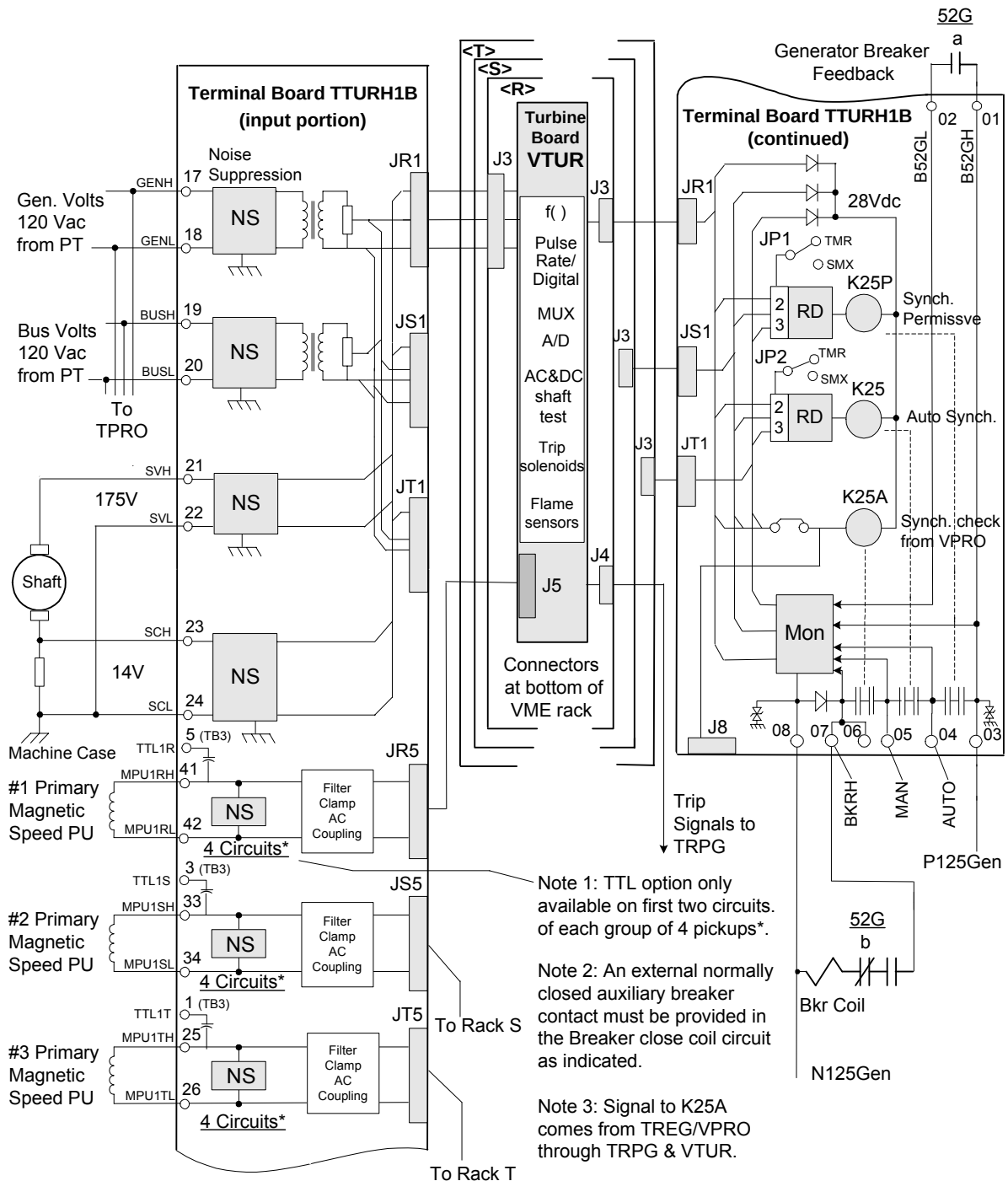
In simplex applications, up to four pulse rate signals can be used to measure turbine speed. Generator and bus voltages are brought into TTUR for automatic synchronizing in conjunction with VTUR, the turbine controller, and excitation system. TTUR has permissive generator synchronizing relays and controls the main breaker relay coil, 52G.



TTUR Control I/O and VTUR Board, Simplex

In TMR applications all inputs fan to the three control racks. Control signals coming into TTUR from R, S, and T are voted before they actuate permissive relays K25 and K25P. Relay K25A is controlled by the VPRO and TREG boards.

Note All three relays have two normally open contacts in series with the breaker close coil.



TTUR Control I/O and VTUR Board, TMR

Specifications

Item	Specification
Number of inputs	12 passive speed pickups. 1 shaft voltage and 1 shaft current measurement. 1 generator and 1 bus voltage. Generator breaker status contact. Signal to K25A relay.
Number of outputs	Generator breaker coil, 5 A at 125 V dc
Power supply voltage	Nominal 125 V dc to breaker coil
MPU pulse rate range	2 Hz to 20 kHz
MPU pulse rate accuracy	0.05% of reading
MPU input circuit sensitivity	27 mV pk (detects 2 rpm speed)
Shaft voltage monitor	Signal is frequency of ± 5 V dc (0 – 1 MHz) pulses from 0 to 2,000 Hz
Shaft voltage wiring	Up to 300 m (984 ft), with maximum two-way cable resistance of 15 Ω
Shaft voltage dc test	Applies a 5 V dc source to test integrity of the external turbine circuit and measures dc current flow.
Shaft voltage ac test	Applies a test voltage of 1 kHz to the input of the VTUR shaft voltage circuit (R module only).
Shaft current input	Measures shaft current in amps ac (shunt voltage up to 0.1 V pp)
Generator and bus voltage sensors	Two single phase potential transformers, with secondary output supplying a nominal 115 V rms Each input has less than 3 VA of loading Allowable voltage range for synch is 75 to 130 V rms Each PT input is magnetically isolated with a 1,500 V rms barrier Cable length can be up to 1,000 ft. of 18 AWG wiring
Generator breaker circuits (synchronizing)	External circuits should have a voltage range within 20 to 140 V dc. The external circuit must include a NC breaker auxiliary contact to interrupt the current Circuits are rated for NEMA class E creepage and clearance 250 V dc applications require interposing relays
Contact voltage sensing	20 V dc indicates high and 6 V dc indicates low Each circuit is optically isolated and filtered for 4 ms
Size	33.0 cm high x 17.8 cm wide (13 in. x 7 in.)
Technology	Surface mount
Temperature	Operating: -30 to 65°C (-22 to 149 °F)

Diagnostics

VTUR makes diagnostic tests on the terminal board and connections as follows:

- Feedback from the solenoid relay drivers; if they do not agree with the control signal a fault is created.
- Feedback from the relay contacts; if they do not agree with the control signal a fault is created.
- Loss of solenoid power, which creates a fault.
- Slow synch check relay, slow auto synch relay, and locked up K25 relay; all of these create a fault.
- If any one of the above signals goes unhealthy, a composite diagnostic alarm L3DIAG_VTUR occurs. The diagnostic signals can be individually latched and then reset with the RESET_DIA signal if they go healthy.
- Terminal board connectors JR1, JS1, JT1, JR5, JS5, JT5 have their own ID device that is interrogated by the I/O board. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VTUR and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

Jumpers JP1 and JP2 select either simplex or TMR for relay drivers K25 and K25P. There are no switches on the board.

TRPG Turbine Primary Trip

Functional Description

The Gas Turbine Primary Trip (TRPG) terminal board is controlled by the Primary Turbine Protection controller (VTUR or PTUR). TRPG contains nine magnetic relays in three voting circuits to interface with three trip solenoids (ETDs). The TRPG works in conjunction with the TREG to form the primary and emergency sides of the interface to the ETDs. TRPG also accommodates inputs from eight Geiger-Mueller[®] flame detectors for gas turbine applications. There are two board types as follows:

- The H1A and H1B version for TMR applications has three voting relays per trip solenoid.
- The H2A and H2B version for simplex applications has one relay per trip solenoid.

Mark VI System

In the Mark* VI system, the TRPG works with the VTUR board and supports simplex and TMR applications. Cables with molded plugs connect TRPG to the VME rack where the VTUR board is located.

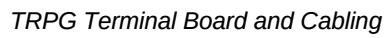
Mark VIe System

In the Mark VIe system, the TRPG is controlled by the PTUR packs on TTURH1C and supports simplex and TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPG.

Version Difference

Board	TMR	Simplex	Output contact, 125 V dc, 1 A	Output contact, 24 V dc, 3 A	28 V Power use
TRPGH1A*	Yes	No	Yes	No	Normal
TRPGH2A*	No	Yes	Yes	No	Normal
TRPGH1B	Yes	No	Yes	Yes	Normal
TRPGH2B	No	Yes	Yes	Yes	Normal
TRPGH3B	Yes	No	Yes	Yes	Special

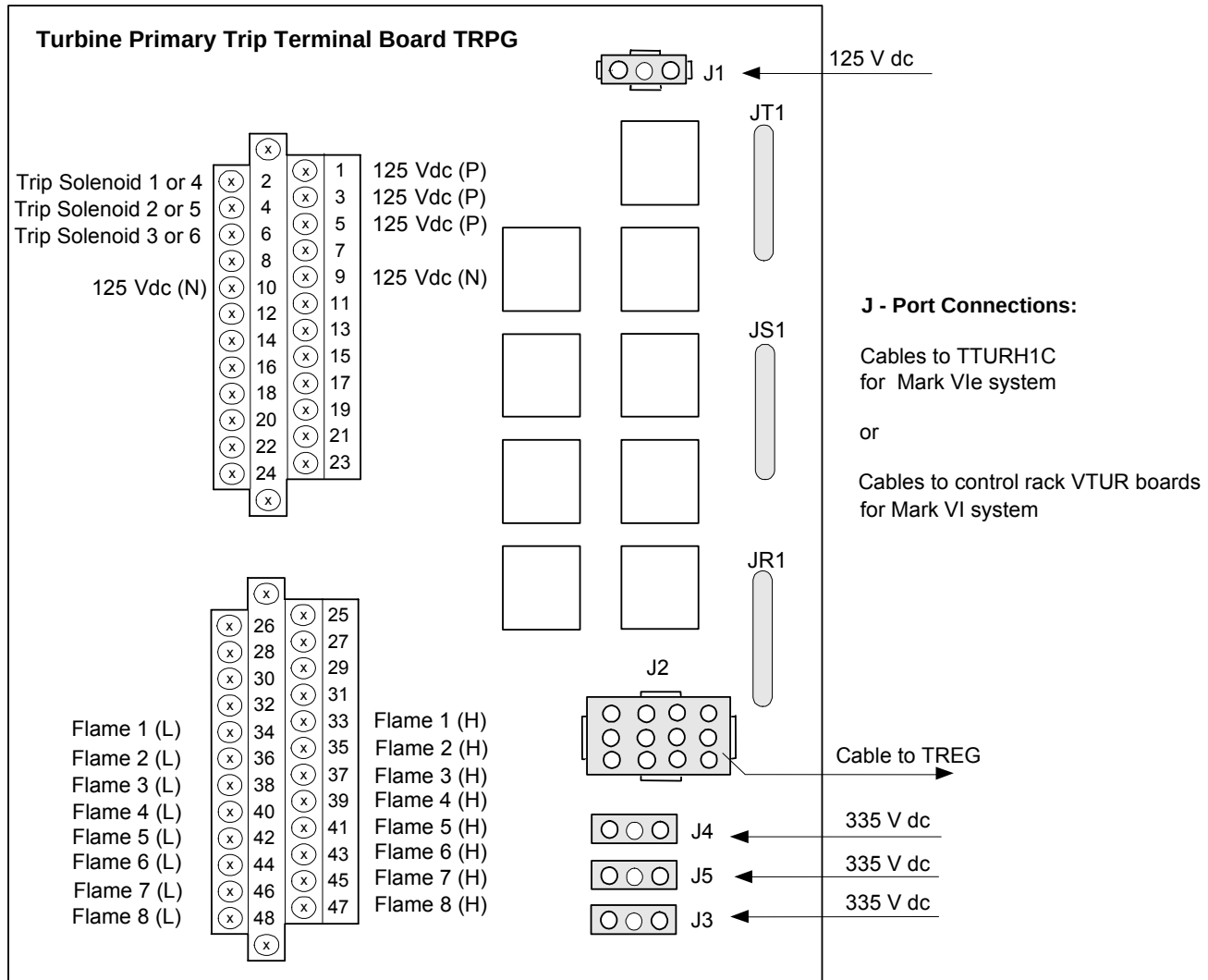
* H1A and H2A are not used for new applications. TRPGH3B features special handling of 28 V control power and is otherwise identical to a TRPGH1B. Consult factory for additional details.



Installation

Connect the wires for the three trip solenoids directly to the first I/O terminal block.
Connect the wires for the flame detectors (if used) to the second terminal block.
Connect the power for the flame detectors to the J3, J4, and J5 plug.

Connect the 125 V dc power for the trip solenoids to the J1 plug. Transfer power to the TREG board using the J2 plug.



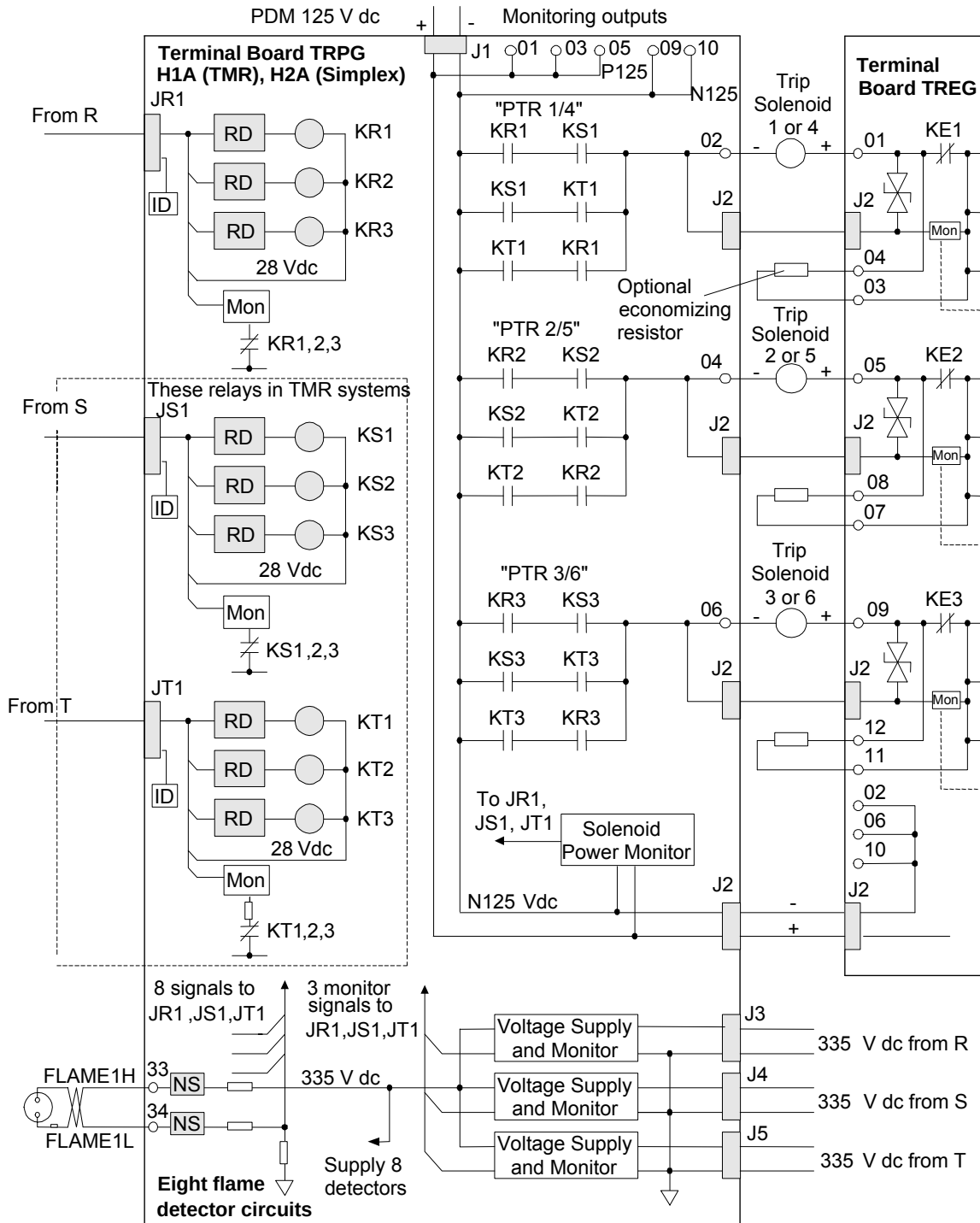
Up to two #12 AWG wires per
point with 300 V insulation

Terminal blocks can be unplugged
from terminal board for maintenance

TRPG Terminal Board Wiring

Operation

The I/O pack/board provides the primary trip function by controlling the relays on TRPG, which trip the main protection solenoids. In TMR applications, the three inputs are voted in hardware using a relay ladder logic two-out-of-three voting circuit. The I/O pack/board monitors the current flow in its relay driver control line to determine its energize or de-energize vote/status of the relay coil contact status. Supply voltages are monitored for diagnostic purposes. A normally closed contact from each relay on TRPG is monitored by the diagnostics to determine its proper operation.



TRPG and Connections to Controller and Trip Solenoids

Note A metal oxide varister (MOV) and a current limiting resistor are used in each ETD circuit

The primary overspeed trip comes from the controller and is passed to the I/O pack/board, and then to TRPG. TRPG works in conjunction with the TREG board, which is controlled by the emergency overspeed system. This TRPG/TREG combination can drive three ETDs.

Flame Detectors

The primary protection system monitors signals from eight Geiger-Mueller[®] flame detectors. With no flame present, the detector charges up to the supply voltage. The presence of flame causes the detector to charge to a level and then discharge through TRPG. As the flame intensity increases, the discharge frequency increases. When the detector discharges, the I/O pack/board and TRPG convert the discharged energy into a voltage pulse. The pulse rate varies from 0 to 1,000 pulses/sec. These voltage pulses are fanned out to all three modules. Voltage pulses above 2.5 volts generate a logic high, and the pulse rate over a 40 ms time period is measured in a counter.

Specifications

Item	Specification
Trip solenoids	3 solenoids per TRPG
Solenoid rated voltage/current	125 V dc standard with up to 1 A draw 24 V dc is alternate with up to 1 A draw (H1B, H2B, H3B)
Solenoid response time	L/R time constant is 0.1 sec
Current suppression	MOV on TREG
Current economizer	Terminals for optional 10 Ω , 70 W economizing resistor on TREG
Control relay coil voltage supply	Relays are supplied with 28 V dc from JR1, JS1, and JT1
Flame detectors	8 detectors per TRPG
Flame detector supply voltage/current	335 V dc with 0.5 mA per detector

Diagnostics

The I/O board runs the TRPG diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid power bus, and the flame detector excitation voltage too low or too high. A diagnostic alarm is created if any one of the signals go unhealthy (beyond limits). Connectors JR1, JS1, and JT1 on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

Configuration

There are no jumpers or hardware settings on the board.

TRPL Turbine Primary Trip

Functional Description

The Large Steam Turbine Primary Trip (TRPL) terminal board is used for the primary overspeed protection of large steam turbines. TRPL is controlled by the turbine Primary Turbine Protection controller (VTUR or PTUR), and contains nine magnetic relays in three voting circuits to interface with three trip solenoids (ETDs). TRPL works in conjunction with the TREL terminal board to form the primary and emergency sides of the interface to the ETDs. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications.

Up to three trip solenoids can be connected between the TREL and TRPL terminal boards. TREL provides the positive side of the 125 V dc to the solenoids and TRPL provides the negative side. In addition, two manual emergency stop functions can be connected.

Mark VI Systems

In the Mark* VI system, the TRPL works with the VTUR board and only supports TMR systems applications. Cables with molded plugs connect TRPL to the VME rack where the VTUR board is located.

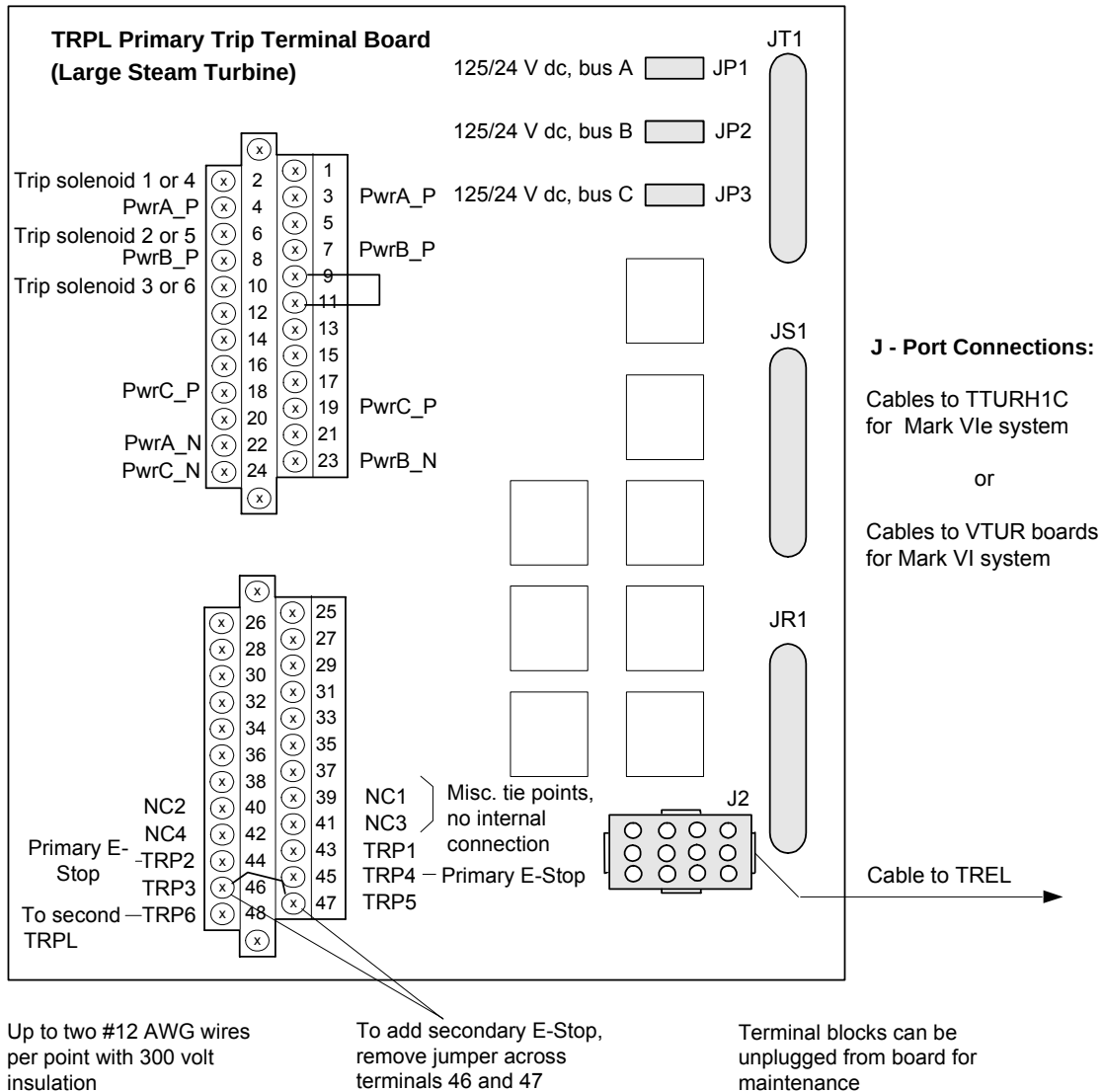
Mark VIe Systems

In the Mark VIe system, the TRPL is controlled by the PTUR I/O packs on TTURH1C and only supports TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPL.

Installation

Connect the wires for the three trip solenoids directly to the first I/O terminal block. Connect the wires for the primary emergency stop and optional secondary emergency stop to the second terminal block. Connect the trip solenoid power to plugs JP1, JP2, and JP3. The wiring connections are shown in the following figure.

Install a jumper across terminals 9 and 11 for the PTR3 trip. If a second emergency stop is required, remove the jumper from terminals 46 and 47 and connect the wires here.



TRPL Terminal Board Wiring

Operation

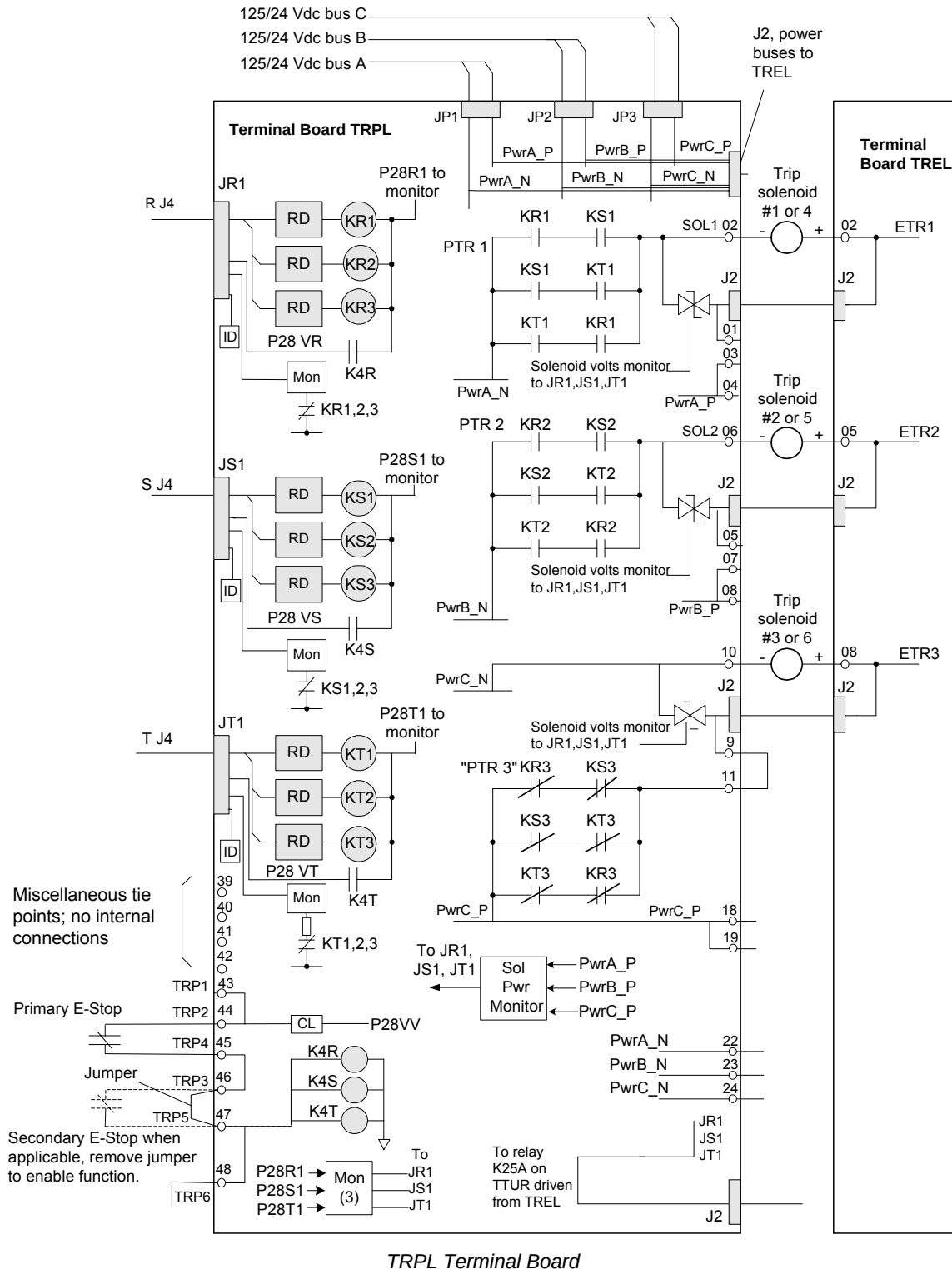
TRPL is used for TMR applications only. Three separate power buses, PwrA, PwrB, and PwrC for solenoid power, are brought in through connectors JP1, JP2, and JP3, and then distributed to TREL through connector J2.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 A.

Each of the three trip solenoids is controlled by three relays using 2/3 contact voting. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 ms, with suppression
- At 125 V dc, 1.0 A, L/R = 100 ms, with suppression

The trip circuits include solenoid suppression, associated solenoid voltage monitoring, and trip relay contact monitoring. In the TRPL, the hardwired trip (E-STOP) and associated monitoring provides approximately 6.6 V dc to the I/O board when the K4 relays are picked up.



Specifications

Item	Specification
Trip solenoids	3 solenoids per TRPx
Solenoid rated voltage/current	125 V dc standard with up to 1 A draw 24 V dc is alternate with up to 3 A draw
Solenoid response time	L/R time constant is 0.1 sec with suppression
Current suppression	MOVs
Control relay coil voltage supply	Relays are supplied with 28 V dc from JR1, JS1, and JT1
Primary Emergency Stop, manual	One with optional secondary E-stop

Diagnostics

Note The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

The I/O controller runs the TRPx diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid voltage, and solenoid power bus. A diagnostic alarm is created if any one of the signals goes unhealthy (beyond limits).

The Jx1 connectors on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no switches or hardware settings on the terminal board. Terminals 9 and 11 must use a jumper to include the PTR 3 trip. Terminals 46 and 47 must use a jumper if only one manual emergency stop is required.

TRPS Turbine Primary Trip

Functional Description

The Small Steam Turbine Primary Trip (TRPS) terminal board is used for the primary overspeed protection of small and medium size steam turbines. TRPS is controlled by the Primary Turbine Protection controller (VTUR or PTUR), and contains three magnetic relays to interface with three trip solenoids (ETDs). TRPS works in conjunction with the TRES terminal board to form the primary and emergency sides of the interface to the ETDs. These two terminal boards are used in a similar way as TRPG and TREG are used on gas turbine applications, except with the following differences:

- Two-out-of-three voting is done in the relay drivers and not using relay contacts as with TRPG and TRPL.
- In a simplex application, the voting is bypassed and the relay drivers are controlled by a single signal from JA1.
- There are no economizing relays.
- There are no flame detector inputs.

Up to three trip solenoids can be connected between the TRES and TRPS terminal boards. TRES provides the positive side of the 125 V dc to the solenoids and TRPS provides the negative side. In addition, two manual emergency stop functions can be connected.

Mark VI Systems

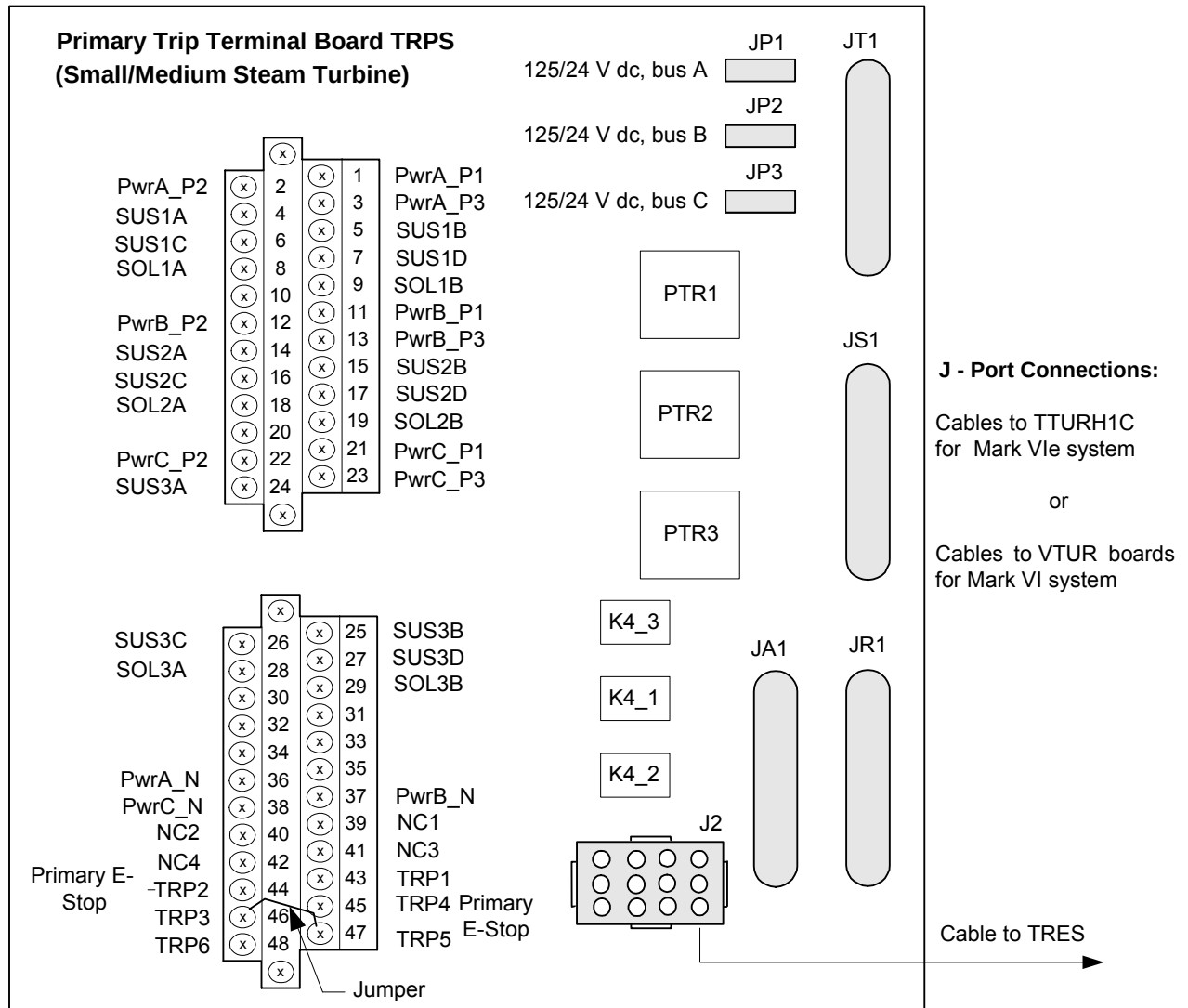
In the Mark* VI system, the TRPS works with the VTUR board and supports simplex and TMR applications. Cables with molded plugs connect TRPS to the VME rack where the VTUR board is located.

Mark VIe Systems

In the Mark VIe system, TRPS is controlled by the PTUR I/O packs on TTURH1C and supports simplex and TMR applications. The I/O packs plug into the D-type connectors on TTURH1C, which is cabled to TRPS.

Installation

Connect the wires for the three trip solenoids to the first I/O terminal block. Connect the wires for the primary emergency stop and optional secondary emergency stop to the second terminal block. Connect the trip solenoid power to plugs JP1, JP2, and JP3. If a second emergency stop is required, remove the jumper from terminals 46 and 47, and connect the wires here. The wiring connections are shown in the following figure.



TRPS Terminal Board Wiring

Operation

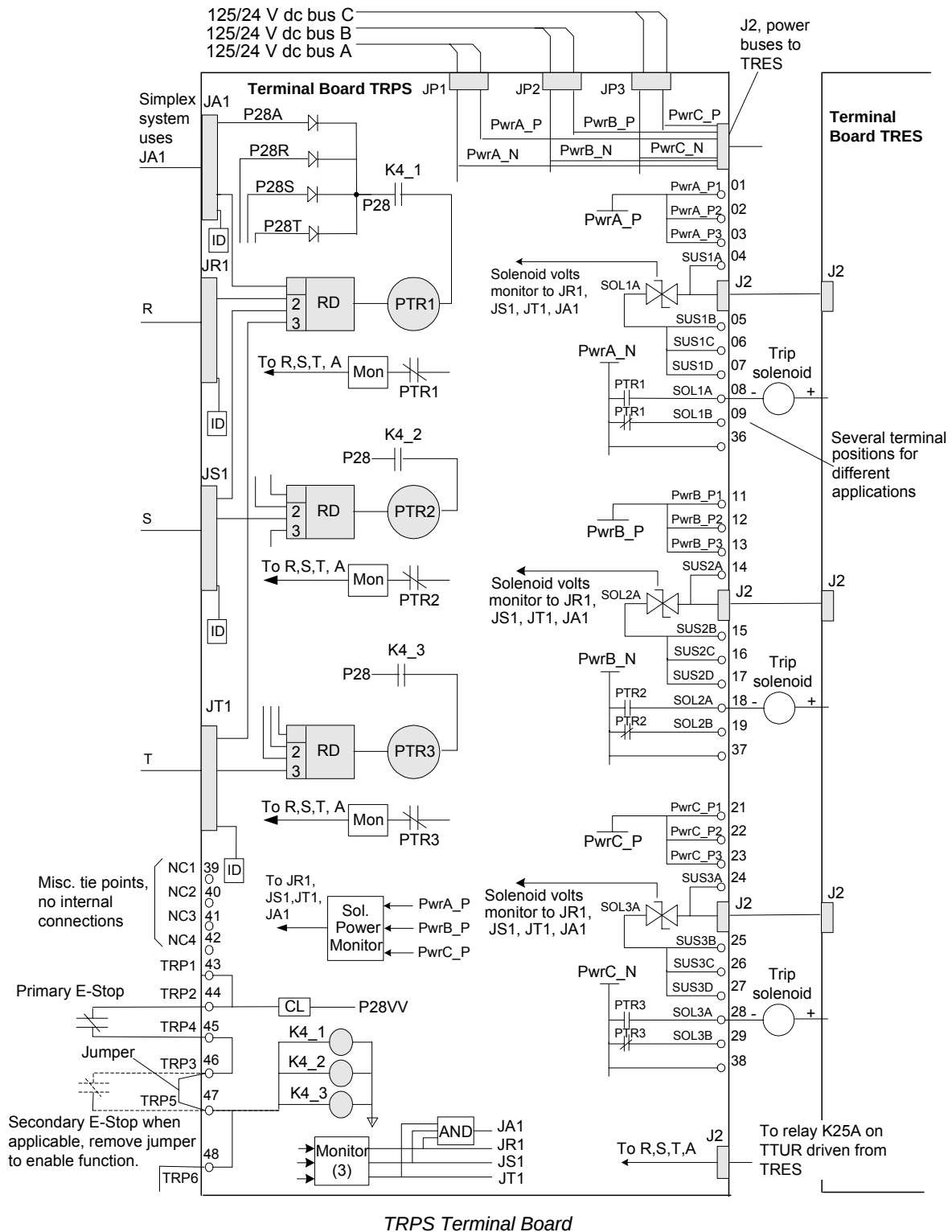
TRPS is used for TMR and simplex applications. Three separate power buses, PwrA, PwrB, and PwrC for solenoid power, are brought in through connectors JP1, JP2, and JP3, and then distributed to TRES through connector J2.

The power buses have a nominal voltage of 125 V dc (70 to 145 V dc) or 24 V dc (18 to 32 V dc). The board includes power bus monitoring (three buses). The maximum current per bus is 3 A.

Each of the three trip solenoids is controlled by a relay driver. The relay output rating (for 100,000 operations) is as follows:

- At 24 V dc, 3 A, L/R = 100 ms, with suppression
- At 125 V dc, 1.0 A, L/R = 100 ms, with suppression

The trip circuits include solenoid suppression, associated solenoid voltage monitoring, and trip relay contact monitoring. In the TRPS, the hardwired trip (E-Stop) and associated monitoring provides approximately 6.6 V dc to the I/O board when the K4 relays are picked up.



Specifications

Item	Specification
Trip solenoids	3 solenoids per TRPx
Solenoid rated voltage/current	125 V dc standard with up to 1 A draw 24 V dc is alternate with up to 3 A draw
Solenoid response time	L/R time constant is 0.1 sec with suppression
Current suppression	MOVs
Control relay coil voltage supply	Relays are supplied with 28 V dc from JR1, JS1, and JT1
Primary Emergency Stop, manual	One with optional secondary E-stop

Diagnostics

Note The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and the plug location.

The I/O controller runs the TRPx diagnostics. These include feedback from the trip solenoid relay driver and contact, solenoid voltage, and solenoid power bus. A diagnostic alarm is created if any one of the signals goes unhealthy (beyond limits).

The Jx1 connectors on the terminal board have their own ID device, which is interrogated by the I/O board, and if a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no switches or hardware settings on the terminal board. Terminals 46 and 47 must use a jumper if only one manual emergency stop is required; remove jumper if secondary E-Stop is used.

TTSA Trip Servo Interface

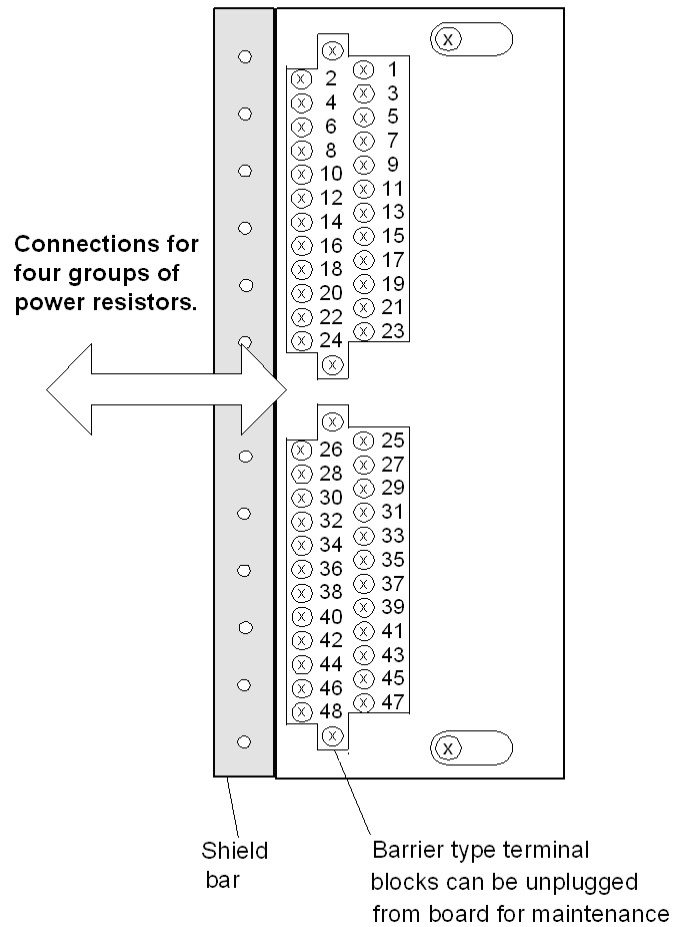
Functional Description

The Trip Servo Interface (TTSA) terminal board provides four sets of power resistors in a configuration to support bipolar currents in two-coil trip servos. All connections to the board are made through pluggable barrier terminal strips. The board is the functional equivalent of the 194B5725 Servo Module in a smaller physical design. Power ratings are adequate to withstand a high DC line of 145 V dc and zero coil impedance.

Mark VI and Mark VIe Systems

The TTSA function is independent of the control in use and is compatible with Mark V, Mark VI, and Mark VIe.

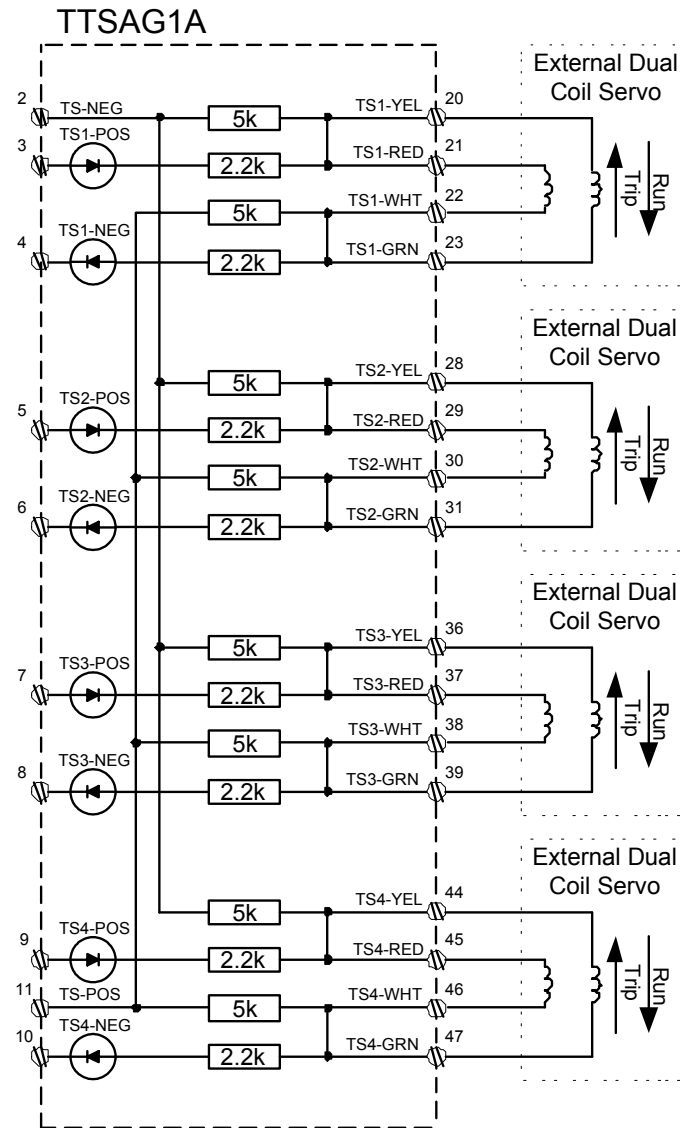
TTSA Terminal Board



Servo Interface Terminal board

Installation

Connect the wires for up to four trip servos to the terminal blocks to provide bipolar coil current, as shown in the following figure. Connect the barrier terminal strips to the appropriate tripping board and servo coils.



Mark VI Trip Servo Interface Board, TTSA

Operation

Fixed 125 V nominal dc power is applied to terminals 11 (positive) and 02 (negative). With no other power, a trip current is applied to the external solenoid coil pair with magnitude equal to $\frac{1}{2} V_{dc} / (10k + \text{parallel solenoid impedance})$. If a 1Ω servo coil is used and V_{dc} is 125 V, the current in each coil equals $\frac{1}{2} * 125 / (10,000 + 500) = 5.95 \text{ mA}$.

When running current is desired in the servo coils, positive dc is applied to the TS#-POS terminal and negative dc is applied to the TS#-NEG terminal. This causes a reverse current in the coil with magnitude equal to $[\frac{1}{2} V_{dc} / (4.4k + \text{parallel solenoid impedance})] \text{ trip current}$. For the previous example, this equals $[\frac{1}{2} * 125 / (4,400 + 500)] - 5.95 \text{ mA} = 6.8 \text{ mA}$.

Specifications

Item	Specification
Maximum applied V dc	145 V
Resistor tolerance	5%
Minimum servo coil impedance	0 Ω

Diagnostics

No diagnostic features are provided on this module.

Configuration

There are no jumpers or hardware settings on the board.

DTUR Simplex Pulse Rate Input

Functional Description

The Simplex Pulse Rate Input (DTUR) terminal board is a compact pulse-rate terminal board designed for DIN-rail mounting. The board accepts four passive pulse-rate transducers (magnetic pickups) for speed and flow measurement. It connects to the VTUR processor board with a 37-pin cable and a 15-pin cable. These cables are identical to those used on the larger TTUR terminal board. VTUR only accommodates one DTUR board.

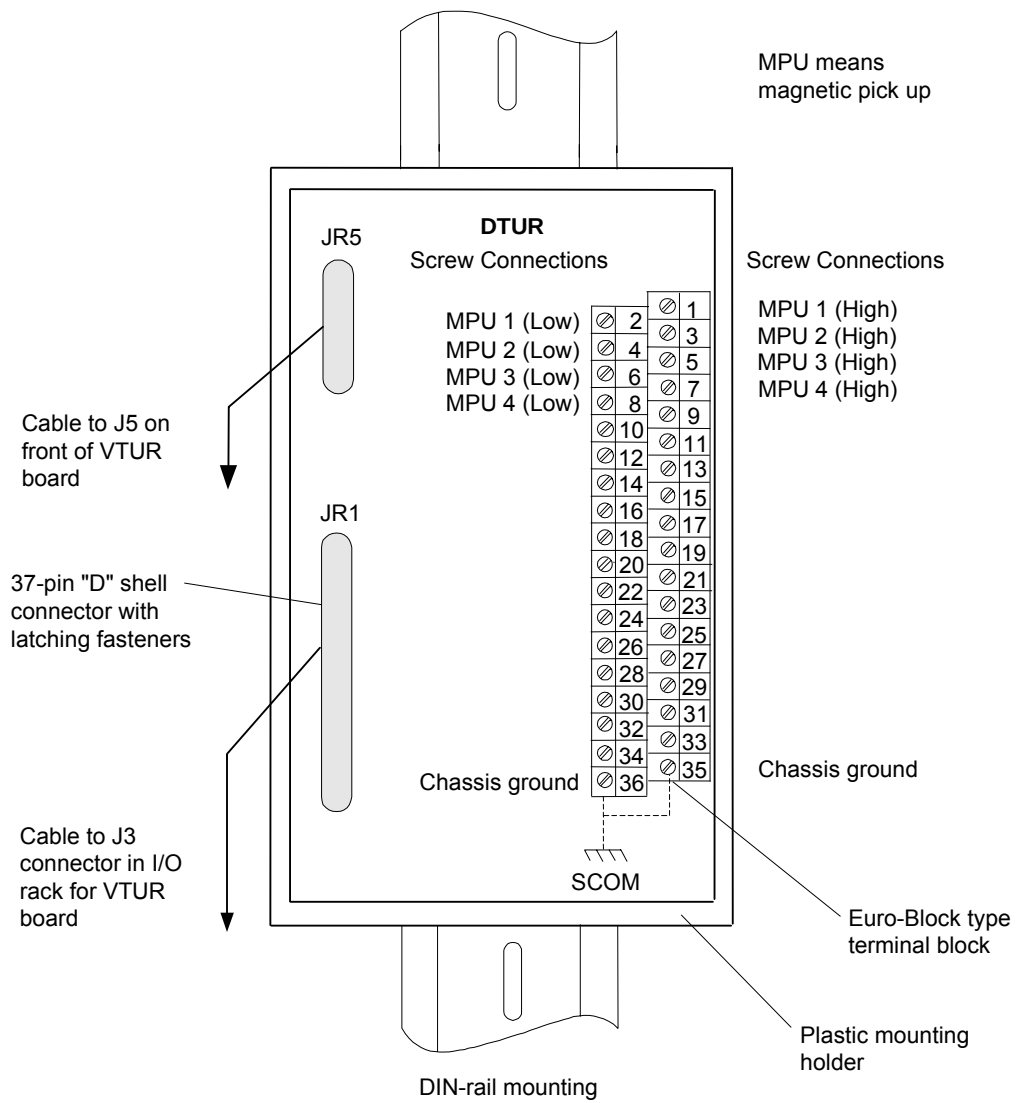
Note DTUR does not work with the Mark VIe system.

Note Only the simplex version is available.

Installation

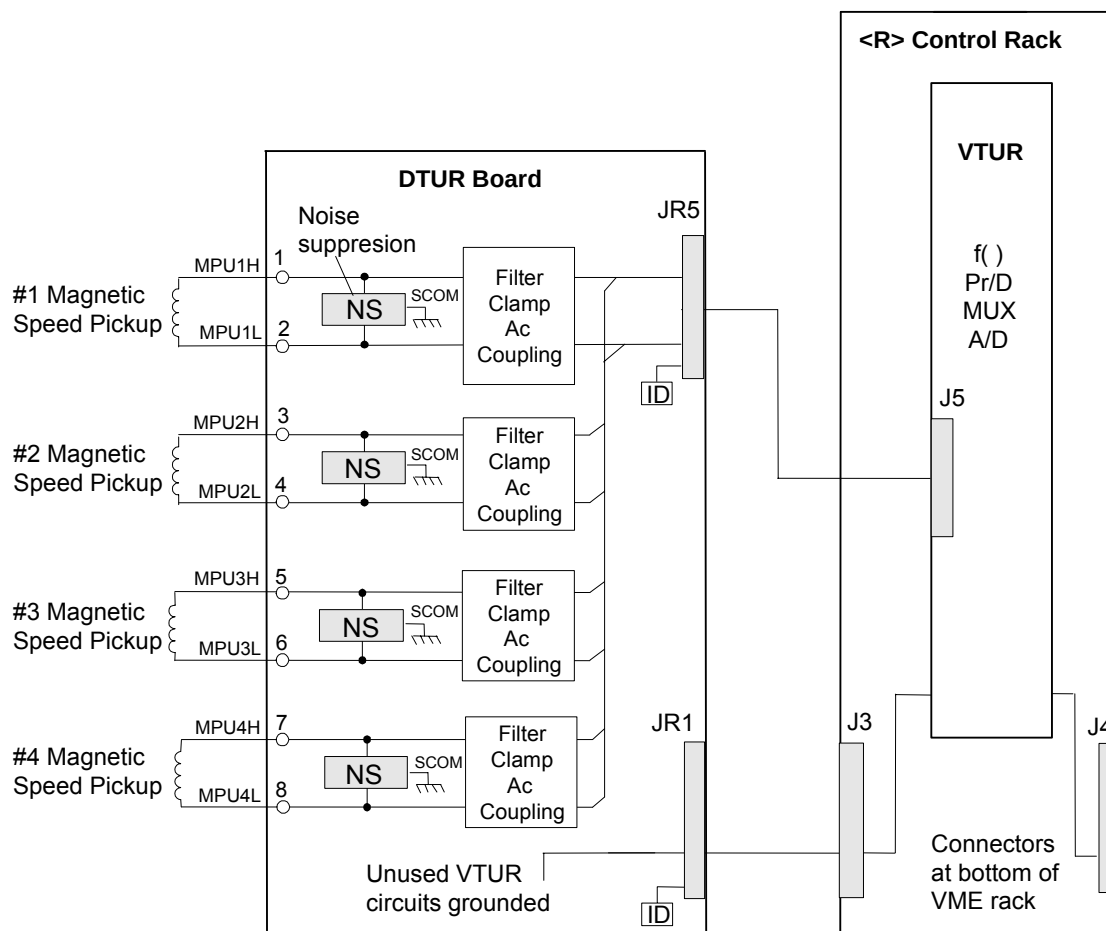
Mount the plastic holder on the DIN-rail and slide the DTUR board into place. DTUR boards can be stacked vertically on the DIN-rail to conserve cabinet space. Connect the wires for the magnetic pickups directly to the terminal block, which has 36 terminals. Typically #18 AWG shielded twisted pair wiring is used. Two screws, 35 and 36, are provided for the SCOM (ground) connection, which should be as short a distance as possible. Connect DTUR to VTUR using the JR1 and JR5 connectors.

Note Only the JR5 cable carries signals to VTUR.



Operation

DTUR accepts four magnetic pulse rate sensors and has onboard signal conditioning identical to that on the TTUR. The pulse frequency circuits are in the VTUR. DTUR does not accept generator and bus voltage signals, or shaft current and voltage signals, as with TTUR. Two on-board ID chips identify the connectors and terminal board to VTUR for system diagnostic purposes.



DTUR Board Circuits

Specifications

Item	Specification
Number of inputs	4 passive speed pickups. TRPG
MPU pulse rate range	2 Hz to 20 kHz
MPU pulse rate accuracy	0.05% of reading
MPU input circuit sensitivity	27 mV pk (detects 2 rpm speed)
Size	16.2 cm high x 8.6 cm wide (6.37 in. x 3.4 in.) with support holder
Technology	Surface mount
Temperature	Operating: -30 to 65°C (-22 to 149 °F)

Diagnostics

Terminal board connectors JR1 and JR5 have their own ID device that is interrogated by VTUR. The ID device is a read-only chip coded with the terminal board serial number, board type, revision number, and plug location. When the chip is read by VTUR and a mismatch is encountered, a hardware incompatibility fault is created.

Configuration

There are no jumpers or hardware settings on the board.

DTRT Simplex Primary Trip Relay Interface

Functional Description

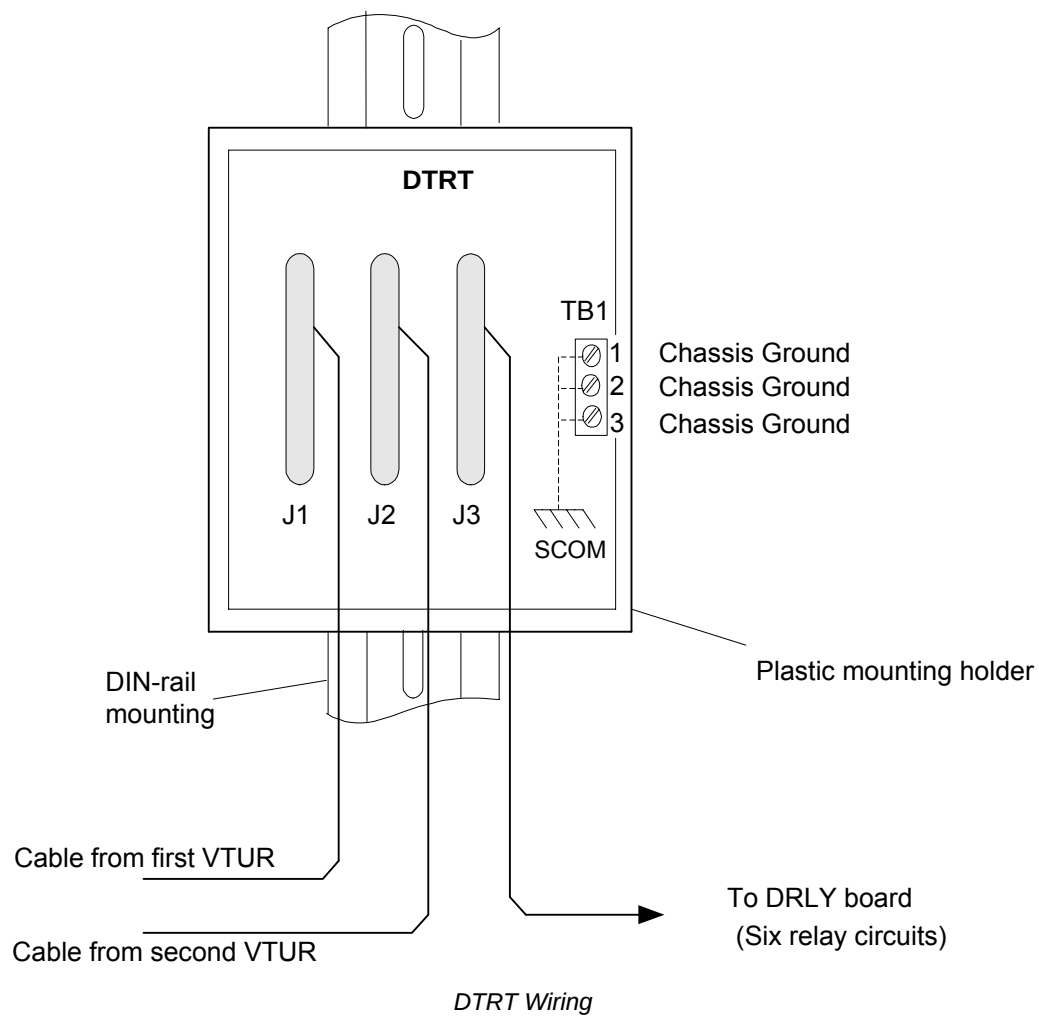
The Simplex Primary Trip Relay Interface (DTRT) terminal board is a DIN-rail mounted trip transition board that connects the VTUR with the DRLY board. DTRT allows three trip functions on the VTUR to interface with DRLY, instead of with the TRPG, TRPL, or TRPS board. Two VTUR boards can connect to the DTRT to control a total of six relays on DRLY.

Note Only the simplex version of this board is available.

Installation

Note DTRT does not have a shield terminal strip.

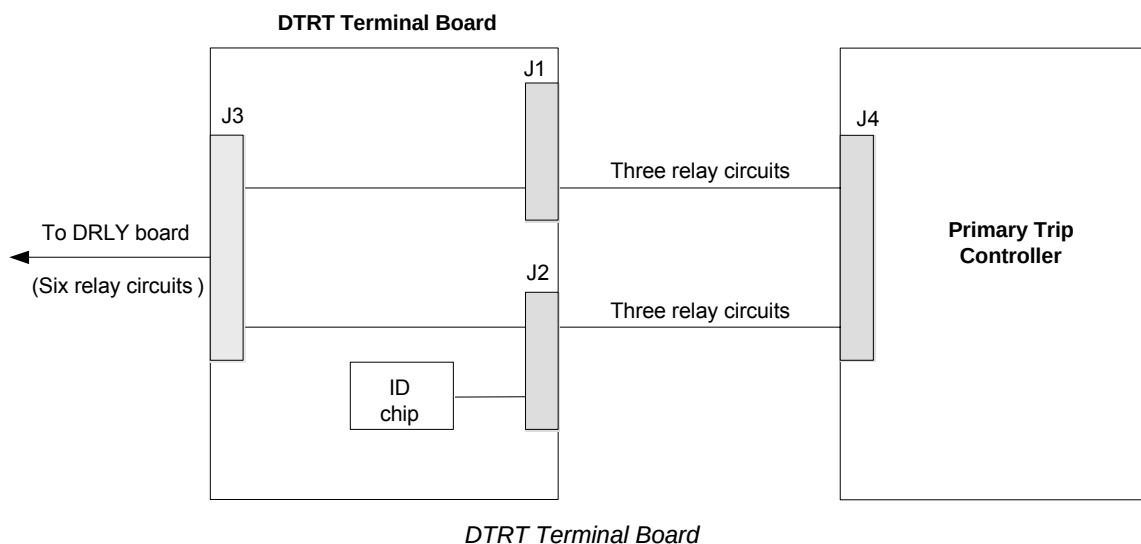
Mount the plastic holder on the DIN-rail and slide the DTRT board into place. The three cables connecting VTUR and DRLY plug into the DC-37 connectors. Connect DTRT to the first VTUR using the J1 connector. Connect DTRT to the second VTUR using the J2 connector. Connect DTRT to DRLY using the J3 connector. Three screws are provided on TB1 for the SCOM (ground) connection, which should be as short a distance as possible.



Operation

DTRT must be used in applications where a trip is required that is faster than VTUR, the controller, and TRPG can provide. DTRT cannot be eliminated if the application requires only one VTUR. A high density Euro-Block type terminal block is permanently mounted to the board with three screw connections for the ground connection (SCOM). The first three DRLY circuits are driven by the first VTUR and the second three DRLY circuits are driven by the second VTUR, as shown in the following figure.

DTRT transfers board identification from the ID chip on DRLY to VTUR for diagnostic purposes. DTRT has its own ID chip connected to J2.



Specifications

Item	Specification
Number of Inputs	Two DC-37 pin connectors for cables from VTUR, J4. 3 trip relays per cable
Number of Outputs	One DC-37 pin connector for cable to DRLY. Total of 6 trip relays

Diagnostics

Diagnostic tests are made on components on the terminal board as follows:

- Each terminal board connector has its own ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, revision number, and the J connector location. When the chip is read by the I/O processor and a mismatch is encountered, a hardware incompatibility fault is created.
- DTRT also transfers ID information from DRLY to VTUR through J1.

Configuration

There are no jumpers or hardware settings on the board.

DRLY Simplex Relay Output

Functional Description

The Simplex Relay Output (DRLY) terminal board is a compact relay output terminal board designed for wall mounting (not DIN-rail mounting). The board has 12 form-C dry contact output relays and connects to the VCCC, VCRC, or VTUR processor board with a single cable. The 37-pin cable connector is identical to those used on the larger TRLY terminal board. Two DRLY boards can be connected to VCCC, VCRC, or VTUR for a total of 24 contact outputs. Only a simplex version of this board is available.

There are two versions of the DRLY terminal board:

- H1A has higher powered relay contacts than H1B.
- H1B is suitable for use in UL listing for Class I, Division 2 Hazardous (classified) locations.

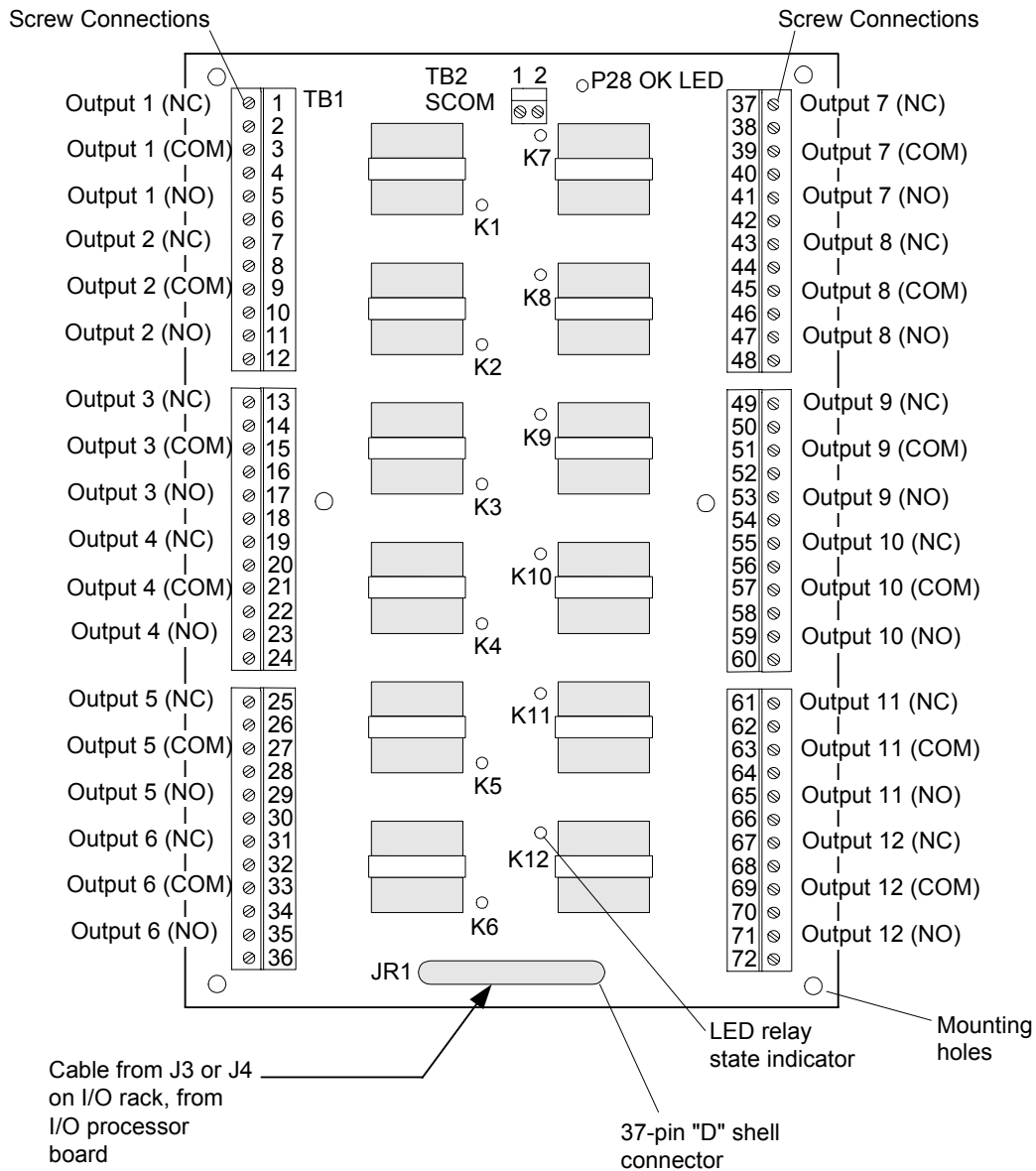
Note DRLY does not work with the PDOA I/O Pack.

Installation

Note DRLY does not have a shield terminal strip.

Mount the DRLY board by fastening screws to wall through the four mounting holes in the corners of metal support plate. Connect the wires for the 12 relay outputs directly to the odd-numbered screws on the terminal blocks. The high-density Euro-Block type terminal blocks plug into the numbered receptacles on the board. The two screws on TB2 are provided for the SCOM (chassis ground) connection, which should be as short a distance as possible.

Note SCOM, TB2, must be connected to chassis ground.

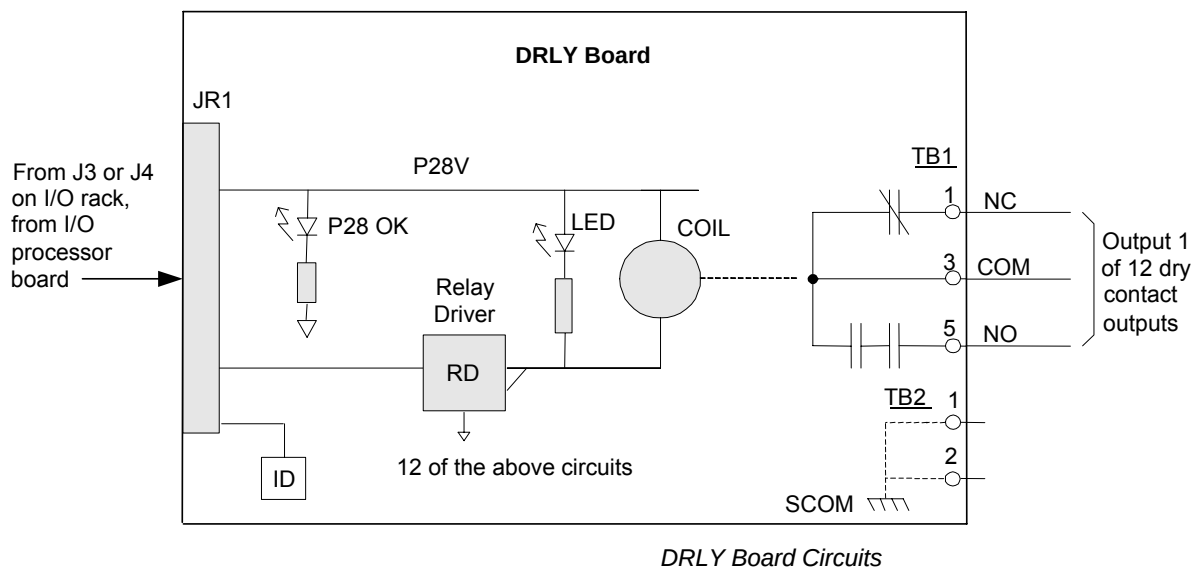


DRLY Wiring and Cabling

Operation

DRLY does not include solenoid source power. There is one set of dry contacts per relay, with two NO contacts in series. Unlike TRLY, there is no on-board suppression, and no relay state monitoring. The I/O board (VCCC, VCRC, or VTUR) provides the 28 V dc power for the relay coils, which is indicated with a green LED. DRLY has a yellow LED for each relay that indicates voltage across the coil. With an unconnected control cable, the relays default to a de-energized state.

Note Three relays on DRLY can be controlled by VTUR using the DTRT transition board. Six relays can be controlled if two DTURs are used.



DRLYH1A Specifications

Item	Specification
Number of relay outputs and type	12 relays, nominal 24 V dc coil. Two-pole double throw with Form C contacts containing two NO and 2 NC contacts
Relay contact rating	Resistive: Inductive: 28 V dc: 10 A 28 V dc: 2 A, L/R = 7 ms, without suppression 120 V ac: 10 A 120 V ac: 2 A, PF= 0.4, 10 A inrush, no suppression Motor load 1/3 Hp. 240 V ac: 3 A 240 V ac: 2 A, PF= 0.4, 10 A inrush, no suppression Motor load 1/2 Hp. 125 V dc: 0.5 A 125 V dc: 0.2 A, L/R = 7 ms without suppression 125 V dc: 0.65 A, L/R = 150 ms, MOV suppression by others (with two contacts in series on the same relay)
Suppression	External suppression will be supplied by customer
Relay response time	Operate: 15 ms typical Release: 10 ms typical
Fault detection in I/O board	The state of the P28 V dc is monitored using a green LED at the top of the board. Voltage across each relay coil is indicated with a yellow LED. There is no relay state monitoring in the VCCC or VCRC
Physical	
Size	21.59 cm long x 20.57 cm wide (8.5 in x 8.1 in wide)
Temperature	0 to 60°C (32 to 140 °F)

DRLYH1B Specifications

Item	Specification
Number of relay outputs	12 relays, nominal 24 V dc coil
Relay type	Two-pole double throw with Form C contacts containing two NO and 2 NC contacts. UL listed, CSA certified, sealed to UL 1604
Relay contact rating (resistive load)	28 V dc: 2 A Max operating voltage: 250 V rms, 220 V dc 125 V dc: 0.5 A Max operating current: 2 A dc, 1 A rms 120 V ac: 1 A Max switching capacity: 125 VA, 60 W 240 V ac: 0.5 A
Suppression	External suppression will be supplied by customer
Relay response time	Operate: 3 ms typical Release: 2 ms typical
Fault detection in I/O board	The state of the P28 V dc is monitored using a green LED at the top of the board Voltage across each relay coil is indicated with a yellow LED There is no relay state monitoring in the I/O board
Agency requirements	UL listed Class I, Division. 2 applications, CSA, and CE, also approvals listed in table above for TRLYH1A
Physical	
Size	21.59 cm long x 20.57 cm wide, (8.5 in x 8.1 in)
Temperature	0 to 75°C (32 to 167 °F)

Diagnostics

The board contains the following diagnostics; there is no relay state monitoring.

- The terminal board connector has an ID device that is interrogated by the I/O board. The connector ID is coded into a read-only chip containing the board serial number, board type, and revision number. When this chip is read by VCCC/VCRC or VTUR and a mismatch is encountered, a hardware incompatibility fault is created.
- The voltage across each relay coil is indicated with a yellow LED.
- The 28 V supply to the board is indicated with a green LED.

Configuration

There are no jumpers or hardware settings on the board.

VVIB Vibration Monitor Board

VVIB Vibration Monitor

Functional Description

The Vibration Monitor (VVIB) board processes vibration probe signals from the TVIB or DVIB terminal board. Up to 14 probes connect directly to the terminal board. Two TVIB can be cabled to the VVIB processor board. VVIB digitizes the various vibration signals, and sends them over the VME bus to the controller. The Mark* VI system uses Bently Nevada* probes for shaft vibration monitoring. The following vibration probes are compatible:

- Proximity
- Velocity
- Acceleration
- Seismic
- Phase

Note If desired, a Bently Nevada 3500 monitoring system can be connected to the terminal board.

Vibration probes are normally used for four protective functions in turbine applications as follows:

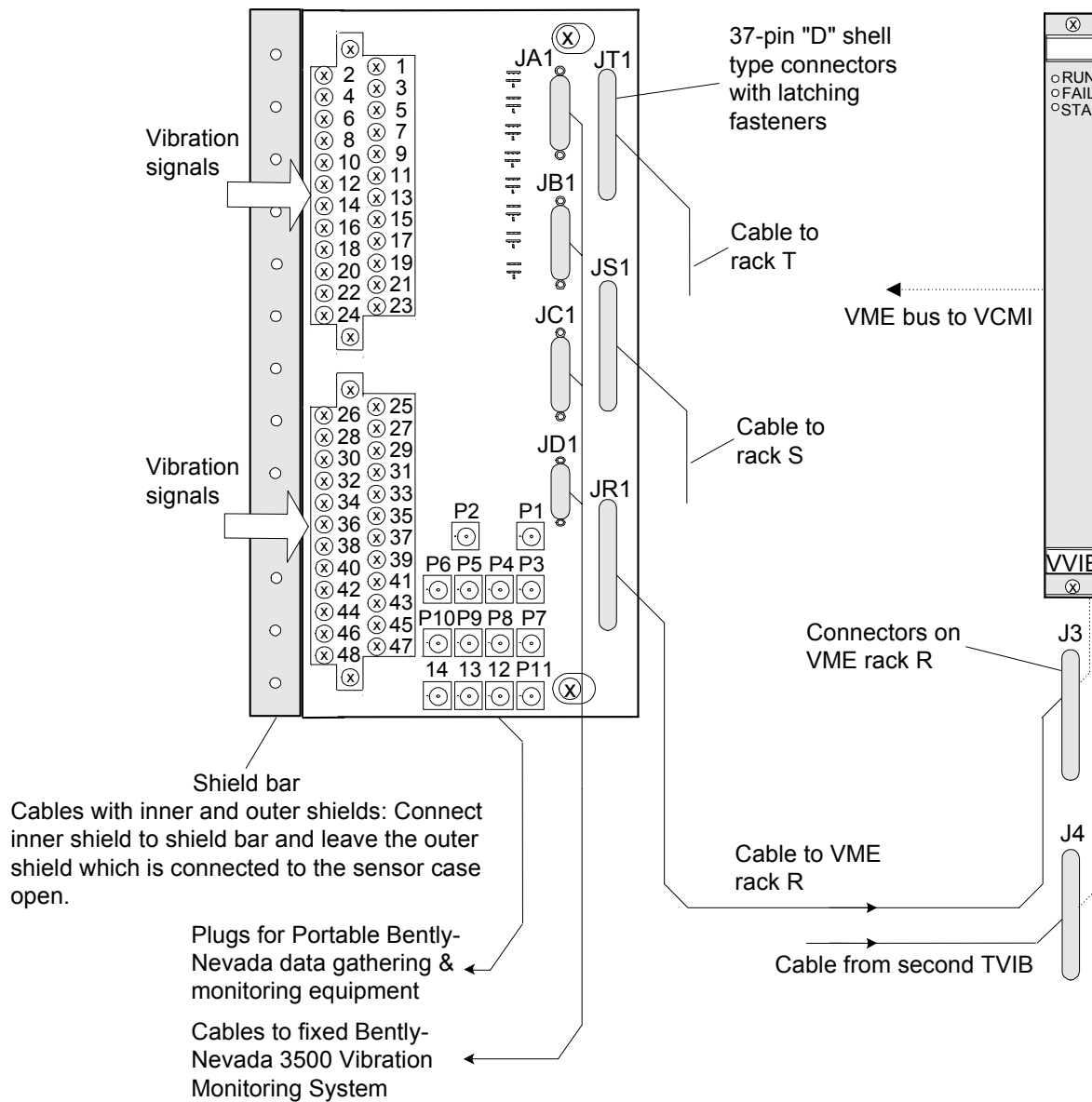
Vibration: Proximity probes monitor the peak-to-peak radial displacement of the shaft (the shaft motion in the journal bearing) in two radial directions. This system uses non-contacting probes and Proximity[®], and detects alarms, trips, and faults.

Rotor Axial Position: A probe is mounted in a bracket assembly off the thrust bearing casing to observe the motion of the thrust collar on the turbine rotor. This system uses non-contacting probes and Proximity, and detects thrust bearing wear alarms, trips, and faults.

Differential Expansion: This application uses non-contacting probe(s) and Proximity(s) and detects alarms, trips, and faults for excessive expansion differential between the rotor and the turbine casing.

Rotor Eccentricity: A probe is mounted adjacent to the shaft to continuously sense the surface and update the turbine control. The calculation of eccentricity is made once per revolution while the turbine is on turning gear. Alarm and fault indications are provided.

There are two types of TVIB terminal boards, H1A and H2A. The H2A type board has BNC connectors allowing portable vibration data gathering equipment to be plugged in for predictive maintenance purposes. Both types have connectors so that Bently Nevada vibration monitoring equipment can be permanently cabled to the terminal board to measure and analyze turbine vibration.



Vibration Processor Board, Terminal Board, and Cabling

Installation

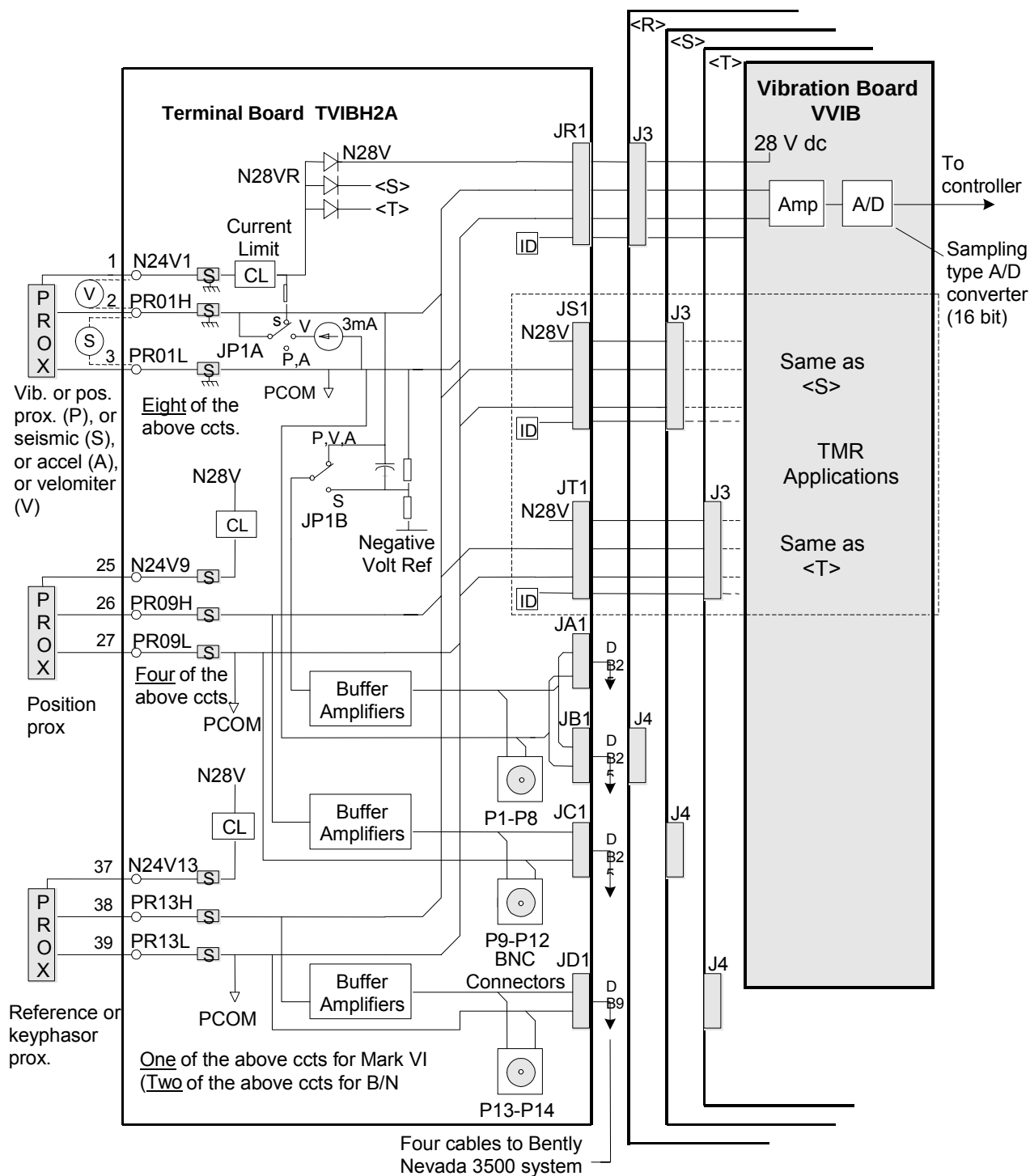
➤ To install the V-type board

- 1 Power down the VME processor rack
- 2 Slide in the board and push the top and bottom levers in with your hands to seat its edge connectors
- 3 Tighten the captive screws at the top and bottom of the front panel

Note Cable connections to the terminal boards are made at the J3 and J4 connectors on the lower portion of the VME rack. These are latching type connectors to secure the cables. Power up the VME rack and check the diagnostic lights at the top of the front panel. For details, refer to the section on diagnostics in this document.

Operation

The terminal board supports Proximitors, Seismic, Accelerometer, and Velomitor[®] probes of the type supplied by Bently Nevada. Power for the vibration probes comes from the VVIB boards, in either simplex or TMR mode. The probe signals return to VVIB where they are A/D converted and sent over the VME bus to the controller.



VVIB Processor, Vibration Probes, and Bently Nevada Interface, TMR system

VVIB supplies -28 V dc to the terminal board for Proximitors power. In TMR systems, a diode high-select circuit selects the highest -28 V dc bus for redundancy. Regulators provide individual excitation sources, -23 to -26 V dc, short circuit protected.

Probe inputs are sampled at high speeds up to 4600 samples per second over discrete time periods. The maximum and minimum values are accumulated, the difference is taken (max-min) for vibration, and the results are filtered. The resulting peak-to-peak voltage is scaled to yield engineering units (EU) (peak-to-peak) displacement for Proximitors inputs, EU (pk) for velocity inputs from accelerometers, integrated outputs, seismics, and Velomiters.

Vibration Monitoring Firmware

The Vibration Monitoring on the VVIB is partitioned in the following manner:

Channels 1 – 3:

Channels 1 through 3 can be used for position information from Proximitors, wideband vibration information from Proximitors, accelerometers with integrated outputs, Velomiters, and Seismics. 1X and 2X information can be derived from Proximitors viewing axial vibration information when a Keyphasor[®] probe is used. Tracking filters are normally used in LM applications with accelerometers.

Gapx_Vibx Vibration Filtering section runs the low-pass filter for the gap calculation, the wideband vibration filter, and the maximum / minimum detect for the peak-to-peak calculation at a 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The Gap Scaling and Limit Check runs at the frame rate. This function converts the gap value from volts to the desired EU. The system limit check provides two detection limits and Boolean outputs for the status. The Vpp, Filter and Limit Check block runs every 160 ms. The peak-to-peak calculation is based on the V_{fmax} and V_{fmin} values of the Gapx_Vibx Wideband Vibration Filtering section. The wideband peak-to-peak signal is filtered and then scaled to EU.

Note Vibx is expressed in EU (pk) for the configuration parameter, VibTypes: accelerometers with integrated outputs, seismics, and Velomiters. Vibx is expressed in EU(pk – pk) for Proximitors.

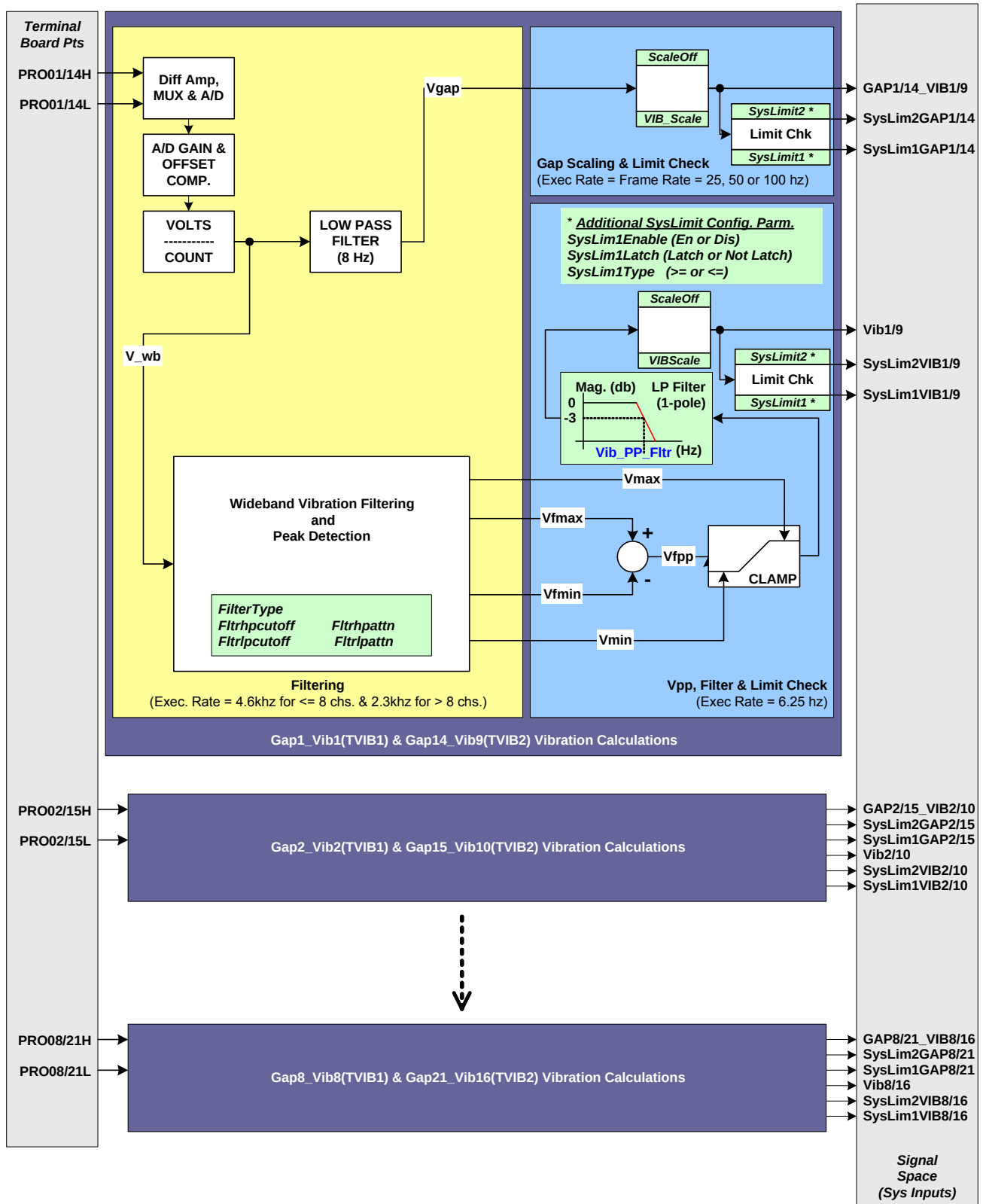
The re-scaled wideband signal is the input for the limit check function. The limit check provides the Booleans, SysLim1VIBx, and SysLim2VIBx for the limit check status.

Three tracking filters are provided to calculate the peak vibration for the LM applications when accelerometers are used. The tracking filters provide the vibration that occurs at the rotor speeds defined by the System outputs, LM_RPM_A, LM_RPM_B, and/or LM_RPM_C. LMVib1A is the vibration detected on channel 1 based on the rotor speed, LM_RPM_A. LMVib1B is the vibration detected on channel 1 based on rotor speed, LM_RPM_B. LMVib1C is based on LM_RPM_C.

The 1X and 2X filters provide the peak-to-peak vibration vector relative to the Keyphasor input from channel 13. VIB1X1 is the peak-to-peak magnitude of the vibration from channel 1 relative to the rpm based on the Keyphasor input. Vib1xPH1 is the phase angle in degrees of the vibration vector from channel 1 relative to the Keyphasor input. VIB2X1 is the peak-to-peak magnitude of the vibration from channel 1 relative to twice the Keyphasor rpm. Vib2xPH1 is the phase angle in degrees of the 2X vibration vector from channel 1.

Channels 4 – 8:

Channels 4 through 8 can be used for position information from Proximitors, wideband vibration information from Proximitors, Velomitors, and Seismics. 1X and 2X information can be derived from Proximitors viewing axial vibration information when a Keyphasor probe is used. Channels 4 through 8 are identical to channels 1 through 3 with the exception of the Tracking filters. Channels 4-8 do not include the Tracking filters.



Channels 9 – 12:

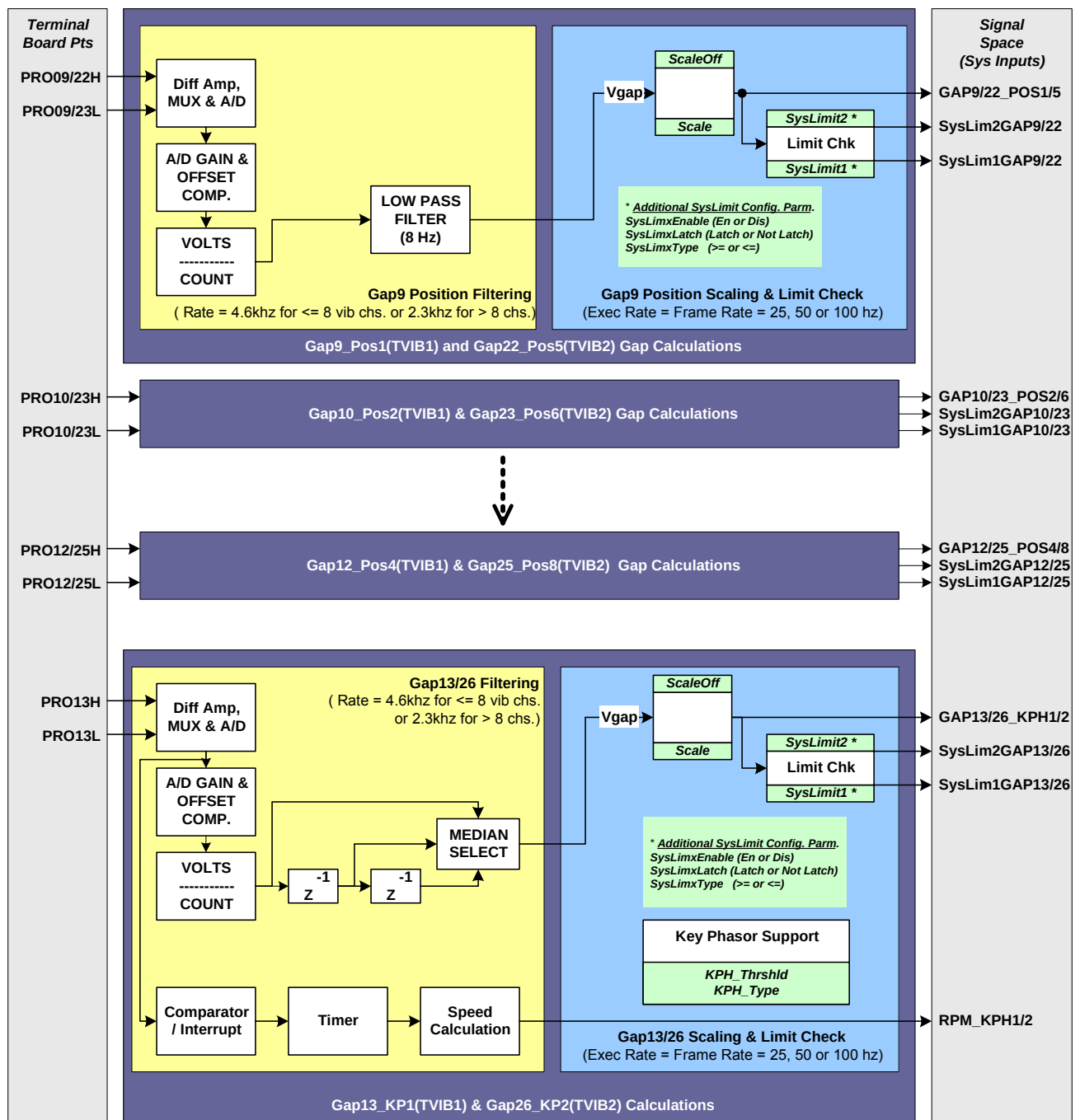
Channels 9 – 12 are used for position information only. The Gapx_Pos_Filtering runs at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. This section provides an 8 Hz low pass filter for the gap calculation. Gapx_Pos Scaling and Limit Check runs every frame. This function rescales the gap value from volts to EU based on the configuration. The System Limit Check can be used set a Boolean at minimum and/or maximum limit values configured by the user.

Channel 13:

Channel 13 supports position feedback and Keyphasor feedback. The Key_Phase Filtering is executed 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The Filtering function performs a median select filter for the gap signal.

A hardware comparator circuit with a software controlled hysteresis limit is used to detect the leading edge of the slot or pedestal gap transition. The Keyphasor timing pulse is fed into an FPGA with counters that determine the time between Keyphasor pulses and the firmware uses this information to calculate the rotor speed in rpm. At very low speeds the hardware Keyphasor comparator is not usable and the runtime application code determines speed by counting pulses detected through the system input, GAP13_KPH1.

The Gap13 KP Scaling and Limit Check runs every frame. The gap scaling and System Limit Check performs the same way it does for channels 1 through 12.



Wideband Vibration Filtering

The Wideband_Vibration Filtering function is executed at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The vibration input for this function comes from the FPGA that controls the A/D and multiplier circuit. The gap or position filter is a 2-pole low pass filter with a cutoff frequency set at 8 Hz. The output of the gap filter is expressed in volts and provides the input the Gap Scaling and Limit Check function.

The wideband vibration information can be shaped or conditioned based on the configuration parameter, FilterType. FilterTypes equal to Low-pass, Band-pass or High-pass are used for the Seismic and Velomitor sensor types. FilterType = None is used by all the other sensor types. The Low-Pass filter can be configured for 2, 4, 6 or 8 pole attenuation behavior through the parameter, Filtrlpattn. The 3 db cutoff frequency, Filtrlocutoff is also adjustable. The High-pass filter can also be configured for 2, 4, 6 and 8 pole to sharpen the attenuation characteristics of the filter through the parameter, Filtrhpattn. The cutoff frequency, Filtrhpcutoff is adjustable in configuration.

The wideband filtered vibration output, Vfout goes through a minimum/maximum peak detect function. The capture window for the minimum/maximum detect is 160 milliseconds wide for Keyphasor based speeds greater than 12 rpm. The objective is to capture at least 2 cycles of vibration information to get an accurate peak-to-peak calculation.

The wideband unfiltered vibration output, goes through a second minimum/maximum peak detect function. The outputs, Vmax and Vmin, are used to clamp the filtered vibration output peak-to-peaks.

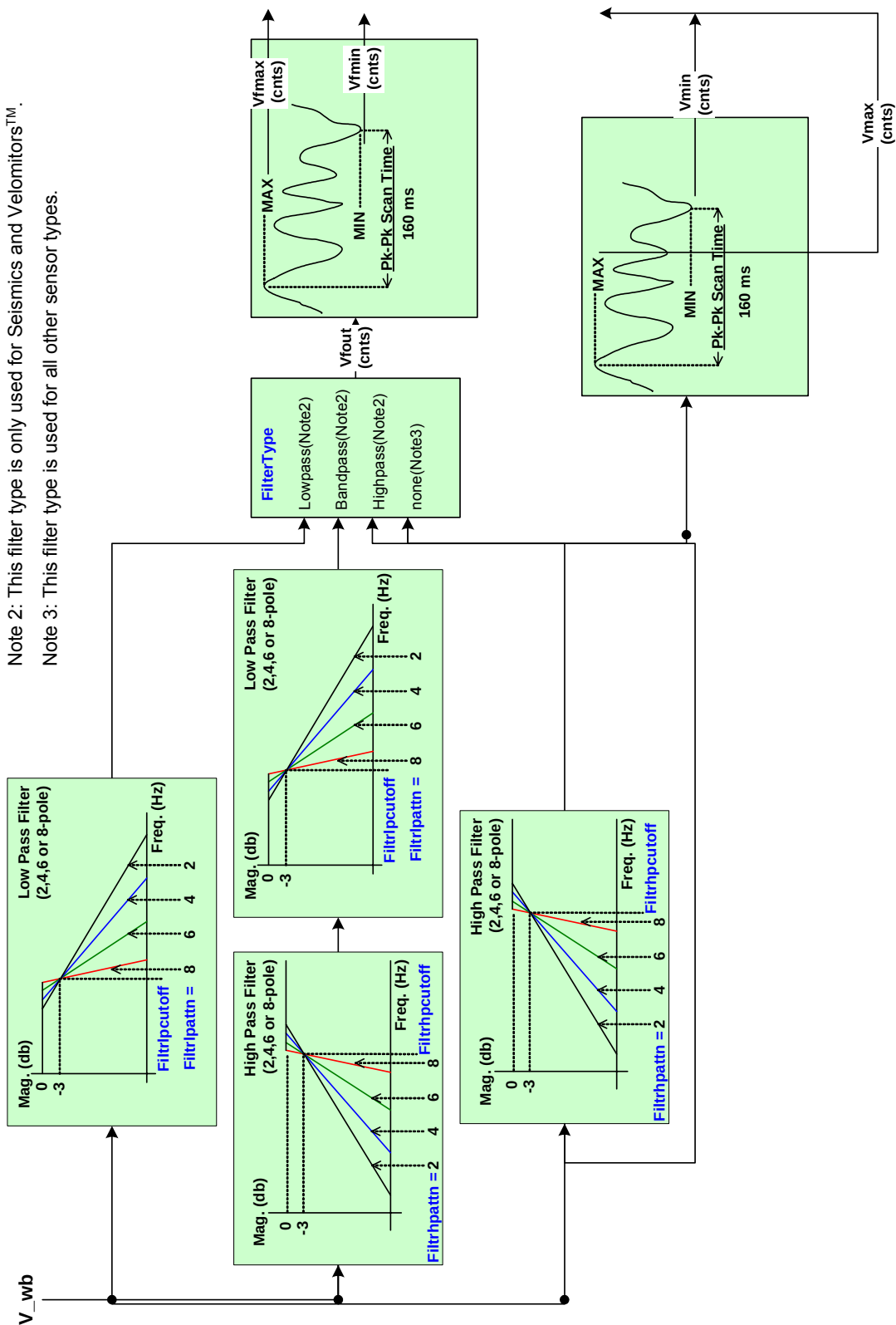
Wideband Vibration Filtering and Peak Detection

Exec. Rate = 4600 / 2300 Hz

Note 1: Text in **BLUE** are PVIB configuration parameters.

Note 2: This filter type is only used for Seismics and Velometers™.

Note 3: This filter type is used for all other sensor types.



Vpp Filter and Limit Check

The Vpp, Filter and Limit Check operates on channels 1 through 8 for TVIB1 and channels 14 through 21 for TVIB2. The execution rate for the function is 6.25 Hz. The Vpp, Filter, and Limit Check inputs are the following:

- Vfmax – filtered maximum peak vibration
- Vfmin – filtered minimum peak vibration
- Vmin – unfiltered min peak vibration
- Vmax – unfiltered max peak vibration

The system inputs or Vpp, Filter, and Limit Check outputs are:

VIBx - the wideband vibration in EU where the units for EU are in peak for the configuration parameter, VibType = Seismic, Velomitor or Accelerometer and the EU units are peak-to-peak for VibType = Proximitior

SysLim1VIBx – the System Limit #1 Boolean (Boolean is True if VIBx is in the limit 1)

SysLim2VIBx – the System Limit #2 Boolean (Boolean is True if VIBx is in the limit 2)

The system output used is the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The filtered peak-to-peak wideband vibration signal, Vfpp = Vfmax – Vfmin. Vfpp is then clamped based on the unfiltered peak-to-peak wideband value. The clamp prevents outputs from the Infinite Impulse Response (IIR-based) filter designs used for the high-pass and low-pass filters to exceed the original input values. The clamped wideband vibration signal, Vpp passes through a single-pole low-pass filter with an adjustable cutoff frequency, VIB_PP_Fltr.

The Vpp, Filter, and Limit Check scaling block converts the clamped and filtered wideband peak-to-peak vibration from volts to EU or Volts peak (Vp) depending on the configuration parameter VibType.

- VibType – determines the A/D conversion value, AD_CONV in units of volts / counts and the default value for the sensor offset and the final EU units being expressed in peak or peak-to-peak.
- VIBScale – gain factor expressed in volts peak / EU (peak) irregardless to the VibType setting.
- ScaleOffset – offset value in EU (peak).

The Vpp, Filter and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

- SysLimxEnabl – the System Limit (x=1 or 2) Enable is set True to select the use of the block.
- SysLimxType – the System Limit (x=1 or 2) Type selects whether the limit check does a “>=” check or a “<=” check.
- SysLimitx – System Limit (x=1 or 2) is the limit value used in the “>=” or “<=” check.
- SysLimxLatch – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched the flag will remain True even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxVIBy where x is the System Limit block number (1 or 2) and y is the VVIB channel input number (1 – 8 for TVIB1 and 14 – 21 for TVIB2).

Gap Scaling and Limit Check

The Gap Scaling and Limit Check operates on channels 1 through 8 for TVIB1 and channels 14 through 21 for TVIB2. The execution rate for the function is 25, 50, or 100 Hz. The rate of execution is based on the frame rate selected for IONet. The system inputs or Gap Scaling and Limit Check outputs are:

Gapx_VIBx – the position or gap value in EU for Proximitors and bias voltage in Vdc for accelerometers with integrated outputs, seismics, and Velomiters

SysLim1GAPx – the System Limit #1 Boolean; (Boolean is True if GAPx_VIBx is in the limit 1)

SysLim2GAPx – the System Limit #2 Boolean. (Boolean is True if GAP_VIBx is in the limit 2)

The system output used is the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The Gap Scaling and Limit Check scaling block converts the 8 Hz filtered output gap signal from volts to EU or Volts peak (Vp) depending on the configuration parameter VibType. The scaling is determined by the following configuration parameters:

- VIB_Scale – gain factor expressed in volts peak / EU (peak) irregardless to the VibType setting.
- ScaleOffset – offset value in EU (peak)

The Gap Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

- SysLimxEnabl – the System Limit (x=1 or 2) Enable is set True to select the use of the block.
- SysLimxType – the System Limit (x=1 or 2) Type selects whether the limit check does a “>=” check or a “<=” check.
- SysLimitx – System Limit (x=1 or 2) is the limit value used in the “>=” or “<=” check.
- SysLimxLatch – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched the flag will remain True even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAPy where x is the System Limit block number (1 or 2) and y is the VVIB channel input number (1 – 8 for TVIB1 and 14 – 21 for TVIB2).

Gapx_POSy Gap Calculations

The Gapx_POSy Gap Calculations is comprised of the Gapx Position Filtering and the Gapx_Pos Scaling and Limit Check where x is the VVIB channel number 9 through 12 for TVIB1 and 22 through 25 for TVIB2 and y is the position number 1 – 4 for TVIB1 and 5 – 8 for TVIB2. The Gapx_POSy Gap Calculation's outputs are:

Gapx_POSy – the position or gap value in EU for Proximitys

SysLim1GAPx – the System Limit #1 Boolean (Boolean is True if GAPx_POSy is in the limit 1)

SysLim2GAPx – the System Limit #2 Boolean (Boolean is True if GAP_POSy is in the limit 2)

The system output used is the System Limit Reset Boolean. If Reset is True, a latched System Limit Boolean is cleared.

The Gapx_Position Filtering is executed at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The position input for this function comes from an FPGA that controls the multiplexed A/Ds. The A/D value is compensated for A/D gain and offset errors and converted to volts. A median select filter is then applied.

The Gapx_Position Scaling and Limit Check scaling block converts the filtered gap signal from volts to EU or Volts peak (Vp) depending on the configuration parameter VibType. The configuration parameters are:

- Scale – gain factor expressed in volts peak / EU (peak)
- ScaleOffset – offset value in EU (peak)

The Gapx_Position Scaling and Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

- SysLimxEnabl – the System Limit (x=1 or 2) Enable is set True to select the use of the block.
- SysLimxType – the System Limit (x=1 or 2) Type selects whether the limit check does a “>=” check or a “<=” check.
- SysLimitx – System Limit (x=1 or 2) is the limit value used in the “>=” or “<=” check.
- SysLimxLatch – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched the flag will remain True even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAPy where x is the System Limit block number (1 or 2) and y is the VVIB channel input number (9 – 12 for TVIB1 and 22 – 25 for TVIB2).

Gap13/26_KPH1/2 Calculations

The Gap13/26_KPH1/2 Calculations is comprised of the Gap13/26 Filtering and the Gap13/26_KP Scaling and Limit Check. The Gap13/26_KPH1/2 Calculation system inputs are:

GAP13_KPH1 – the position or gap value in EU for the Keyphasor Proximitors for TVIB1

GAP26_KPH2 – the position or gap value in EU for the Keyphasor Proximitors for TVIB2

SysLim1GAP13 – the System Limit #1 Boolean for TVIB1 (Boolean is True if GAP13_KPH1 is in the limit 1)

SysLim2GAP13 – the System Limit #2 Boolean for TVIB1 (Boolean is True if GAP13_KPH1 is in the limit 2)

SysLim1GAP26 – the System Limit #1 Boolean for TVIB2 (Boolean is True if GAP26_KPH2 is in the limit 1)

SysLim2GAP26 – the System Limit #2 Boolean for TVIB2 (Boolean is True if GAP26_KPH2 is in the limit 2)

The Gap13_KPH1 system outputs are:

SysLimReset – the System Limit Reset Boolean (If Reset is True, a latched System Limit Boolean is cleared)

LM_RPMx – rotor shaft speed in rpm from different stages of the turbine (x = A, B or C)

The Gap 13/26 Filtering is executed at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The input for this function comes from a multiplexed A/D controlled by an FPGA. The Gap 13/26 Filtering uses the median select function to calculate the filtered gap. The median select filter uses the present value (n), the previous (n-1), and the value 2 samples back (n-2) to perform a median select on. The output is expressed in volts and passes to the Gap13/26 Scaling and Limit Check.

The Gap13/26 Scaling and Limit Check scaling block converts the filtered gap signal from volts to EU. The Gap13/26 runs at the frame rate of either 25, 50 or 100 Hz. The gap conversion is based on the following configuration parameters:

- Scale – gain factor expressed in volts peak / EU (peak)
- ScaleOffset – offset value in EU (peak)

The Gap13/26 Scaling & Limit Check provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

- SysLimxEnabl – the System Limit (x=1 or 2) Enable is set True to select the use of the block.
- SysLimxType – the System Limit (x=1 or 2) Type selects whether the limit check does a “>=” check or a “<=” check.
- SysLimx – System Limit (x=1 or 2) is the limit value used in the “>=” or “<=” check.
- SysLimxLatch – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched the flag will remain True even if the limit value is no longer exceeded.

The system input or System Limit Boolean status flag is SysLimxGAP13 for TVIB1 and SysLimxGAP26 for TVIB2 where x is the System Limit block number (1 or 2).

1X and 2X Calculations based on Keyphasor Input

The 1X and 2X Calculations based on a Keyphasor input provides a peak-to-peak vibration component (magnitude and phase) at both the Keyphasor frequency and twice the frequency. The calculations are comprised of two sections:

- Modulator and Filter
- Magnitude and Phase Calculation

The system inputs from the 1X & 2X calculations are:

- Vib1Xy – the peak-to-peak magnitude of the vibration phasor that is rotating at the Keyphasor frequency
- Vib1xPHy – the phase angle between the Keyphasor input and the ViB1Xy vibration phasor
- Vib2Xy – the peak-to-peak magnitude of the vibration phasor that is rotating at the twice the Keyphasor frequency
- Vib1xPHy – the phase angle between the Keyphasor input and the Vib2Xy vibration phasor, and where y is the VVIB channel number, 1 through 8 for TVIB1 and 14 through 21 for TVIB2

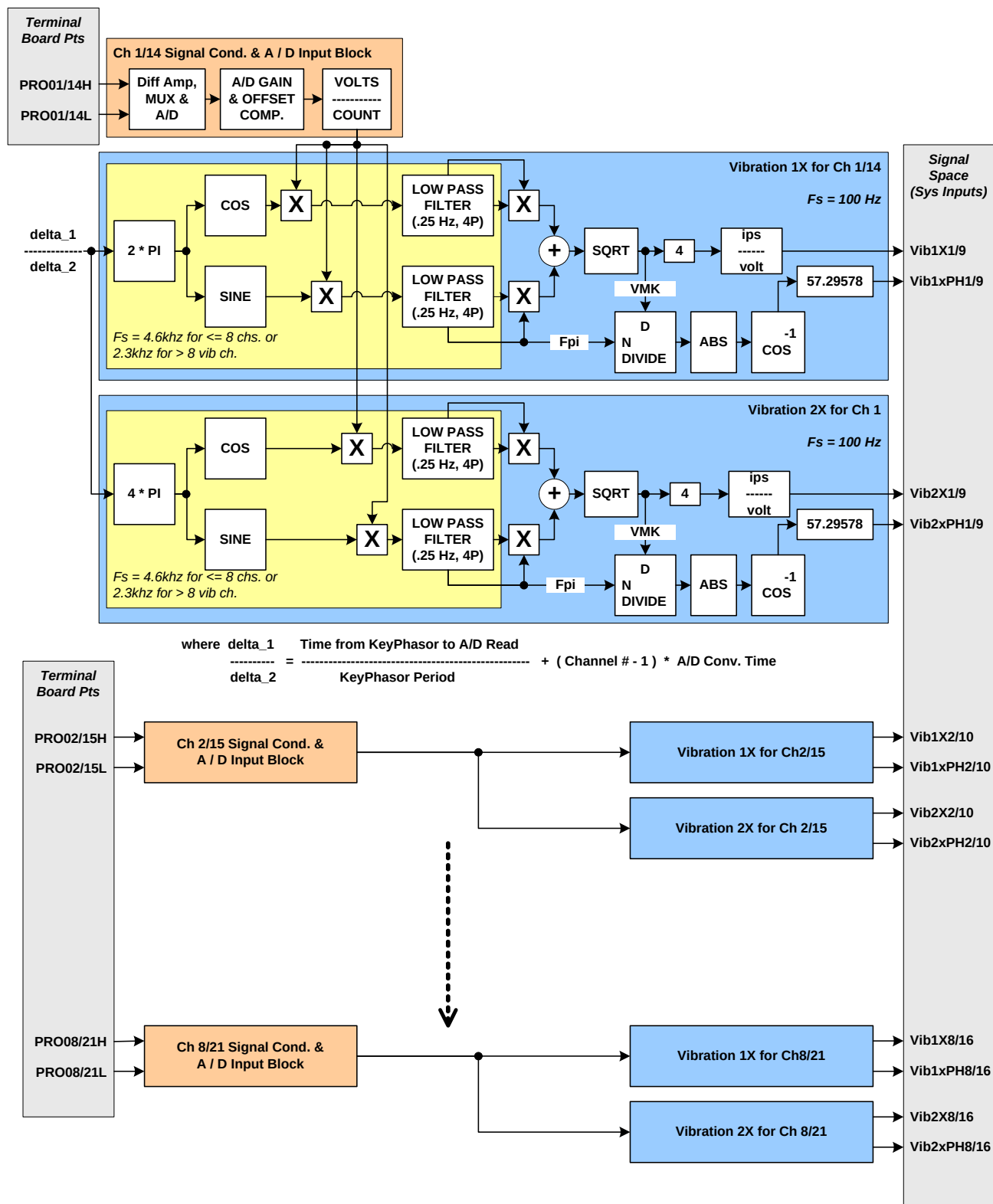
The Modulator and Filter for both the 1X and 2X calculations are executed at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels. The 1X modulator has two inputs: delta_1/delta_2 and the vibration channel input. The delta_1/delta_2 is the point in the key_phasor cycle where the vibration channel input was sampled. The range for delta_1/delta_2 is from 0 to 1. Delta_1/delta_2 is converted to radians and is the index into a cosine and sine lookup table. The result from the cosine and sine lookup table is modulated with the vibration channel input. The modulated signal is filtered through a 4-pole low pass filter with a cutoff frequency of 0.25 Hz. The filter output provides the dc value of the de-modulated components: the real and imaginary phasors of the vibration component that is rotating at 1X speed.

The Vibration 1X function uses the real and imaginary vibration components based on the Keyphasor frequency as the inputs to the RMS calculator. The square root of the sum of the squares of the real and imaginary vibration components times the scaling block results in the peak-to-peak magnitude of the 1X vibration phasor, Vib1Xy rotating at the Keyphasor frequency. The phase, Vib1xPHy, is the arccosine of the absolute value of Fpi / (VMK).

The Vibration 2X function is the same calculation except the input delta_1/delta_2 is multiplied by 4 * PI instead of 2 * PI. The results are a peak-to-peak magnitude of the 2X vibration phasor, Vib2Xy, rotating at twice the Keyphasor frequency and a phase of Vib2xPHy.

The scaling block converts the VMK * 4 signal to EU. The scaling is based the following configuration parameters:

- Scale – gain factor expressed in volts peak / EU (peak)
- ScaleOffset – offset value in EU (peak)



Tracking Filters based on LM_RPM_A/B and C

The Tracking Filters based on LM_RPM_A/B and C provide the peak vibration component (magnitude only) at the frequencies: LM_RPM_A, LM_RPM_B, and LM_RPM_C. The Tracking filters require both Modulation & filter stage executing at 4.6 kHz rate and 2.3 kHz rate if input channels 14 through 21 are configured as vibration channels and the Magnitude calculation.

The system inputs from the Tracking filters are:

- LMVibxA – the peak magnitude of the vibration component rotating at LM_RPM_A speed
- LMVibxB – the peak magnitude of the vibration component rotating at LM_RPM_B speed
- LMVibxC – the peak magnitude of the vibration component rotating at LM_RPM_C speed
- SysLim1ACCx – the System Limit Boolean status of Limit1 where x = 1 through 9
- SysLim2ACCx – the System Limit Boolean status of Limit2 where x = 1 through 9

The Modulator and Low-pass filter for the LMVibxA, LMVibxB, and LMVibxC tracking filters are executed at 4.6 kHz rate. The low-pass filter is identical for all tracking filters. The filter is a 5-pole low-pass filter with a cutoff frequency equal to 2.5 Hz. The LMVibxA filter inputs are the modulated signals $\cos(2\pi/60F_s * LM\_RPM\_A) * \text{Vibration Input}$ and $\sin(2\pi/60F_s * LM\_RPM\_A) * \text{Vibration Input}$. The filtered output of the modulated vibration input with the sine is the de-modulated imaginary component of the channel vibration based on the rotor shaft speed, LM_RPM_A and the filtered output of the modulated vibration input with the cosine is the de-modulated real component of the channel vibration based on the rotor shaft speed, LM_RPM_A.

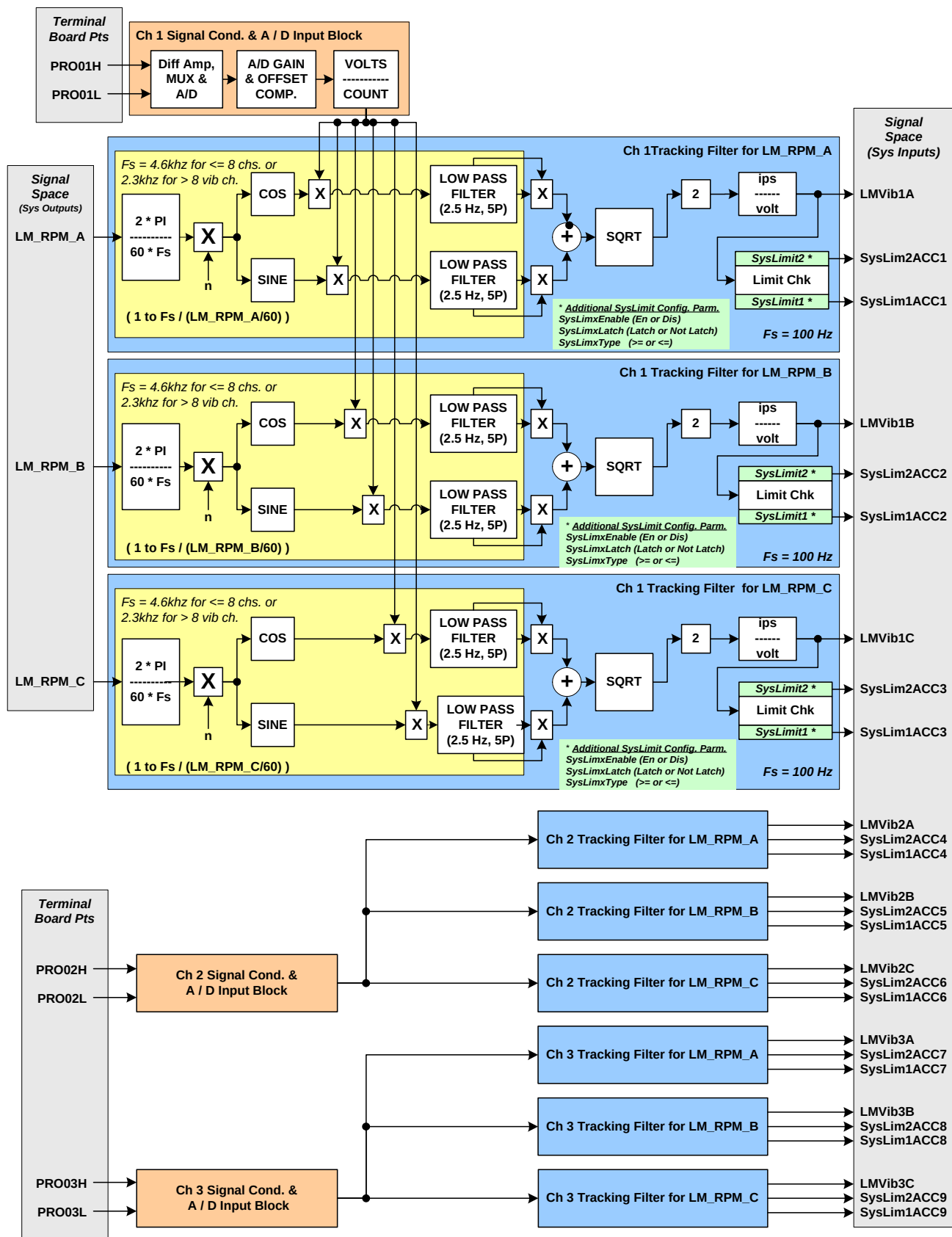
The LMVibxB and LMVibxC tracking filters perform the same task as the LMVibxA filter, except the de-modulated real and imaginary components of the vibration input are based on the rotor speeds: LM_RPM_B and LM_RPM_C.

The scaling block converts the VMx where x = A, B, or C magnitude to EU. The scaling is based on the following configuration parameters:

- Scale – gain factor expressed in volts peak / EU (peak)
- ScaleOffset – offset value in EU (peak)

The Tracking Filter provides two System Limit blocks. The following configuration parameters control the behavior of the System Limit block:

- SysLimxEnabl – the System Limit (x=1 or 2) Enable is set True to select the use of the block.
- SysLimxType – the System Limit (x=1 or 2) Type selects whether the limit check does a “>=” check or a “<=” check.
- SysLimitx – System Limit (x=1 or 2) is the limit value used in the “>=” or “<=” check.
- SysLimxLatch – System Limit (x=1 or 2) Latch determines whether the Boolean status flag is latched or unlatched. If the Boolean status flag is latched the flag will remain True even if the limit value is no longer exceeded.



Specifications

Item	Specification			
Number of Channels	TVIB: 13 probes: 8 vibration, 4 position, 1 Keyphasor VVIB: 26 probes with two TVIB boards			
Vibration	Measurement	Range	Accuracy	Frequency
Proximity	Displacement	0 to 4.5 V pp	±0 .030 V pp	5 to 200 Hz
	Displacement	0 to 4.5 V pp	±0 .150 V pp	200 to 500 Hz
Seismic	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]	5 to 200 Hz
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]	200 to 500 Hz
Velomitor	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]	5 to 200 Hz
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]	200 to 500 Hz
Accelerometer	Velocity (track filter)	0 to 2.25 V p	±0.015 Vp	10 to 233 Hz
Position	Position	-.5 to -20 V dc	±0.2 V dc	Air gap (average)
Phase	Degrees	0 to 360 degrees	±2 degrees	Up to 14,000 rpm
(1X vibration component with respect to key slot)				
Probe power	-24 V dc from the -28 V dc bus; each probe supply is current limited 12 mA load per transducer			
Probe signal sampling	16-bit A/D converter with 14-bit resolution on the VVIB Sampling rate is 4,600 samples per second in fast scan mode (4,000 to 17,500 rpm) Sampling rate is 2,586 samples per second for nine or more probes (less than 4,000 rpm) All inputs are simultaneously sampled in time windows of 160 ms			
Rated RPM	If greater than 4,000 rpm, can use eight vibration channels, (others can be prox/position) If less than 4,000 rpm, can use 16 vibration channels, and other probes			
Buffered outputs	Amplitude accuracy is 0.1% for signal to Bently Nevada 3500 vibration analysis system			

Diagnostics

Diagnostics perform a high/low (hardware) limit check on the input signal and a high/low system (software) limit check. The software limit check is adjustable in the field.

A probe fault, alarm, or trip condition occurs if either of an X or Y probe pair exceeds its limits. In addition, the application software prevents a vibration trip (the ac component) if a probe fault is detected based on the dc component.

Position inputs for thrust wear protection, differential expansion, and eccentricity are monitored similar to the vibration inputs except only the dc component is used for a position indication. A 16-bit sampling type A/D converter is used with 14-bit resolution and overall circuit accuracy of 1% of full scale.

Vibration Monitoring and Analysis

Note The Mark VI system provides vibration protection and displays the basic vibration parameters.

Each input is actively isolated and the signals made available through four plugs for direct cabling to a Bently Nevada 3500 monitor. This configuration provides the maximum reliability by having a direct interface from the Proximity sensors to the turbine control for trip protection and still retaining the real-time data access to the Bently Nevada system for static and dynamic vibration monitoring.

Note The Mark VI system displays the total vibration, the 1X vibration component, and the 1X vibration phase angle, but it is not intended as a vibration analysis system.

Fourteen BNC connectors on TVIB provide buffered signals available to portable data gathering equipment for predictive maintenance purposes. Buffered outputs have unity gain, 10 k Ω internal impedance, and can drive loads up to 1500 Ω configuration.

Configuration

Parameter	Description	Choices
Configuration		
System limits	Enable system limits	Enable, disable
Vib_PP_Fltr	First order filter time constant (sec)	0.01 to 2
LMVib1A	Vib, 1X component, for LM_RPM_A, input #1 - board point	Point edit (input FLOAT)
SysLim1Enable	Enable system limit 1 fault check	Enable, disable
SysLim1Latch	Latch system limit 1 fault	Latch, not latch
SysLim1Type	system limit 1 check type	>= or <=
SysLimit1	System Limit 1 - Vibration in mils (Prox) or Inch/sec (seismic, accel)	-100 to +100
SysLim2Enable	Enable system limit 2 (same configuration as above)	Enable, disable
TMR_DiffLimt	Difference limit for voted TMR inputs in volts or mils	-100 to +100
LMVib1B	Vib, 1X component, for LM_RPM_B, #1 - board point	Point edit (input FLOAT)
LMVib1C	Vib, 1X component, for LM_RPM_C, #1 - board point	Point edit (input FLOAT)
LMVib2A	Vib, 1X component, for LM_RPM_A, #2 - board point	Point edit (input FLOAT)
LMVib2B	Vib, 1X component, for LM_RPM_B, #2 - board point	Point edit (input FLOAT)
LMVib2C	Vib, 1X component, for LM_RPM_C, #2 - board point	Point edit (input FLOAT)
LMVib3A	Vib, 1X component, for LM_RPM_A, #3 - board point	Point edit (input FLOAT)
LMVib3B	Vib, 1X component, for LM_RPM_B, #3 - board point	Point edit (input FLOAT)
LMVib3C	Vib, 1X component, for LM_RPM_C, #3 - board point	Point edit (input FLOAT)
J3:IS200TVIBH1A	Vibration terminal board, first of two	Connected, not connected
GAP1_VIB1	Average air gap (for Prox) or dc volts (for others) - board point	Point edit (input FLOAT)
VIB_Type	Type of vibration probe	Unused, PosProx, VibProx, VibProx-KPH1, VibProx-KPH2, VibLMACcel, VibVelomitor, KeyPhasor
VIB_Scale	Volts/mil or volts/ips	0 to 2
ScaleOff	Scale offset for prox position only, in mils	0 to 90
SysLim1Enable	Enable system limit 1	Enable, disable
SysLim1Latch	Latch the alarm	Latch, not latch
SysLim1Type	System limit 1 check type	>= or <=
SysLimit1	System limit 1 – GAP in negative volts (for vel) or positive mils (prox)	-100 to +100
SysLim2Enabl	Enable system limit 2 (same configuration as above)	Enable, disable
TMR_DiffLimt	Difference limit for voted TMR inputs in volts or mils	-100 to +100

Parameter	Description	Choices
Vib1	Vibration, displacement (pk-pk) or velocity (pk) - board point	Point edit (input FLOAT)
SysLim1Enable	System limits configured as above	Enable, disable
GAP2_VIB2	Second vibration probe of 8 - board point	Point edit (input FLOAT)
Vib2	Vibration, displacement (pk-pk) or velocity (pk) - board point	Point edit (input FLOAT)
GAP9_POS1	First position probe of 4 - board point	Point edit (input FLOAT)
GAP13_KPH1	KeyPhasor probe air gap - board point	Point edit (input FLOAT)
J4:IS200TVIBH1A	Second vibration terminal board	Connected, not connected
GAP14_VIB9	First Vibration Probe of 8 - board point	Point edit (input FLOAT)
Vib9	Vibration, displacement (pk-pk) or velocity (pk) - board point	Point edit (input FLOAT)
GAP22_POS5	First position probe of 4 - board point	Point edit (input FLOAT)
GAP26_KPH2	KeyPhasor probe air gap - board point	Point edit (input FLOAT)

Board Points Signals	Description - Point Edit (Enter Signal Connection)	Direction	Type
L3DIAG_VVIB1	Board diagnostic	Input	BIT
L3DIAG_VVIB2	Board diagnostic	Input	BIT
L3DIAG_VVIB3	Board diagnostic	Input	BIT
SysLim1GAP1	Gap signal limit	Input	BIT
:	:	Input	BIT
SysLim1GAP26	Gap signal limit	Input	BIT
SysLim2GAP1	Gap signal limit	Input	BIT
:	:	Input	BIT
SysLim2GAP26	Gap signal limit	Input	BIT
SysLim1VIB1	Vibration signal limit	Input	BIT
:	:	Input	BIT
SysLim1VIB16	Vibration signal limit	Input	BIT
SysLim1ACC1	Acceleration signal limit	Input	BIT
:	:	Input	BIT
SysLim1ACC9	Acceleration signal limit	Input	BIT
SysLim2VIB1	Vibration signal limit	Input	BIT
:	:	Input	BIT
SysLim2VIB16	Vibration signal limit	Input	BIT
SysLim2ACC1	Acceleration signal limit	Input	BIT
:	:	Input	BIT
SysLim2ACC9	Acceleration signal limit	Input	BIT
RPM_KPH1	Speed RPM, of KP #1	Input	FLOAT
RPM_KPH2	Speed RPM, of KP #2	Input	FLOAT
Vib1X1	Vibration, 1X component only, displacement	Input	FLOAT
:	:	Input	FLOAT
Vib1X16	Vibration, 1X component only, displacement	Input	FLOAT
Vib1XPH1	Angle of 1X component to KP	Input	FLOAT
:	:	Input	FLOAT
Vib1XPH16	Angle of 1X component to KP	Input	FLOAT
LM_RPM_A	-----	Output	FLOAT
LM_RPM_B	-----	Output	FLOAT
LM_RPM_C	-----	Output	FLOAT

Alarms

Fault	Fault Description	Possible Cause
2	Flash Memory CRC Failure	Board firmware programming error (board will not go online)
3	CRC failure override is Active	Board firmware programming error (board is allowed to go online)
16	System Limit Checking is Disabled	System checking was disabled by configuration.
17	Board ID Failure	Failed ID chip on the VME I/O board
18	J3 ID Failure	Failed ID chip on connector J3, or cable problem
19	J4 ID Failure	Failed ID chip on connector J4, or cable problem
20	J5 ID Failure	Failed ID chip on connector J5, or cable problem
21	J6 ID Failure	Failed ID chip on connector J6, or cable problem
22	J3A ID Failure	Failed ID chip on connector J3A, or cable problem
23	J4A ID Failure	Failed ID chip on connector J4A, or cable problem
24	Firmware/Hardware Incompatibility	Invalid terminal board connected to VME I/O board.
30	ConfigCompatCode mismatch; Firmware: #; Tre: # The configuration compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
31	IOCompatCode mismatch; Firmware: #; Tre: # The I/O compatibility code that the firmware is expecting is different than what is in the tre file for this board	A tre file has been installed that is incompatible with the firmware on the I/O board. Either the tre file or firmware must change. Contact the factory.
32	VVIB A/D Converter 1 Calibration Outside of Spec. VVIB monitors the Calibration Levels on the 2 A/D. If any one of the calibration voltages is not within 1% of its expected value, this alarm is set	The hardware failed (if so replace the board) or there is a voltage supply problem
33	VVIB A/D Converter 2 Calibration Outside of Spec. VVIB monitors the Calibration Levels on the 2 A/D. If any one of the calibration voltages is not within 1% of its expected value, this alarm is set	The hardware failed (if so replace the board) or there is a voltage supply problem
34	TVIB J3 Analog Input (channel #) Out of Limits	Possible open circuit, customer cable short or sensor failure
35	TVIB J4 Analog Input (channel #) Out of Limits	Possible open circuit, customer cable short or sensor failure
65-77/ 81-93	TVIB/DVIB J3/J4 Analog Input # out of limits. VVIB monitors the Signal Levels from the 2 A/D. If any one of the voltages is above the max value, this diagnostic is set	The TVIB/DVIB board(s) may not exist but the sensor is specified as used, or the sensor may be bad, or the wire fell off, or the device is miswired.
128- 287	Logic Signal # Voting mismatch. The identified signal from this board disagrees with the voted value	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.
288- 404	Input Signal # Voting mismatch, Local #, Voted #. The specified input signal varies from the voted value of the signal by more than the TMR Diff Limit	A problem with the input. This could be the device, the wire to the terminal board, the terminal board, or the cable.

TVIB Vibration Input

Functional Description

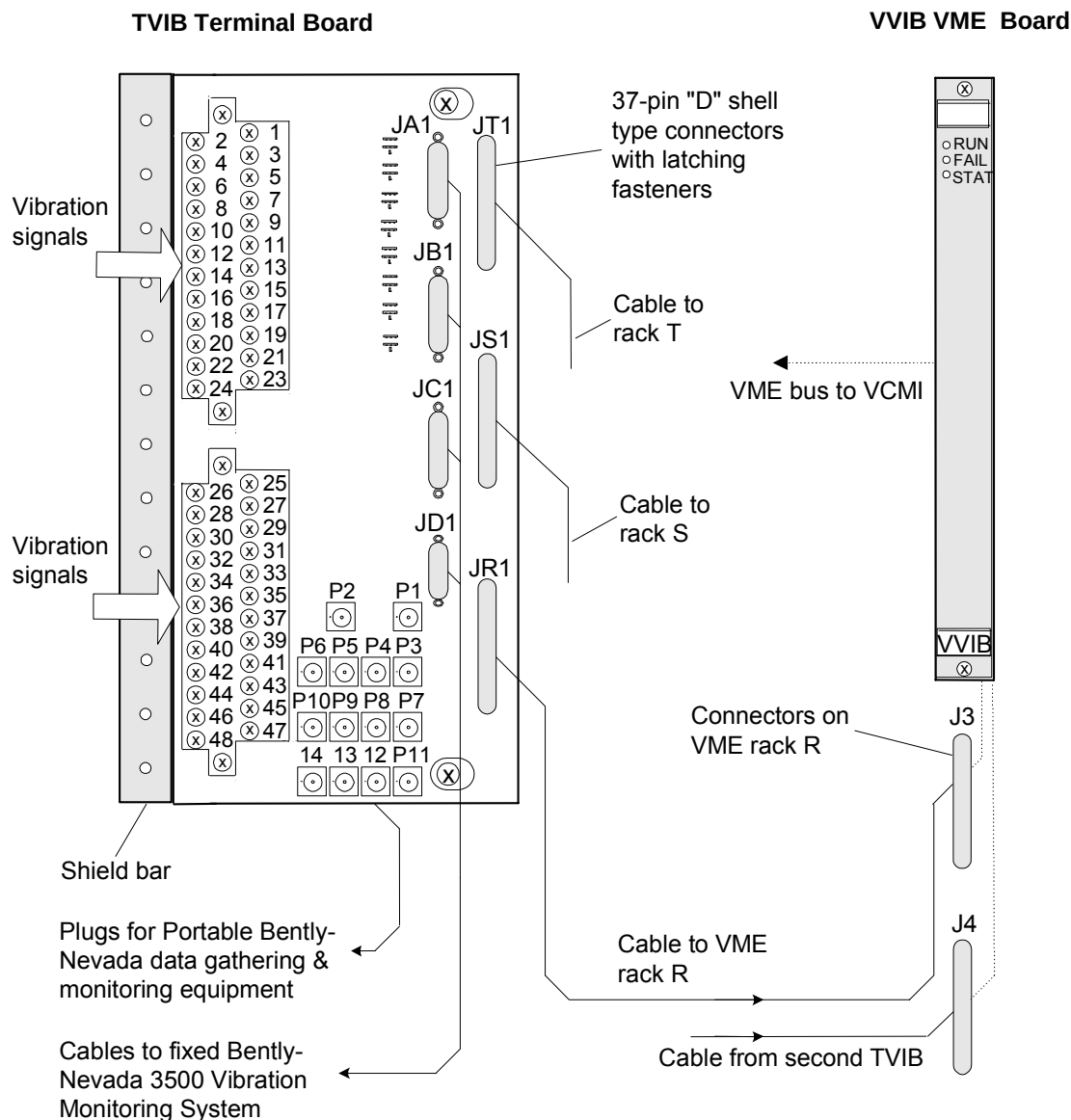
The Vibration Input (TVIB) terminal board accepts up to 14 vibration probes, two of which can be cabled directly to the VVIB board. VVIB processes and digitizes the displacement and velocity signals, which are then sent over the VME bus to the controller. The Mark* VI system uses Bently Nevada probes for shaft vibration monitoring. The following vibration probes are compatible with TVIB:

- Proximity
- Velocity
- Acceleration
- Seismic
- Phase

There are two types of TVIB terminal boards, H1A and H2A. The H2A type board has BNC connectors allowing portable vibration data gathering equipment to be plugged in for predictive maintenance purposes. Both types have connectors so that Bently Nevada vibration monitoring equipment can be permanently cabled to the terminal board to measure and analyze turbine vibration.

In the Mark VI system TVIB works with the VVIB processor and supports simplex and TMR applications. Two TVIBs connect to VVIB with two cables. In TMR systems, TVIB connects to three VVIB processors with three cables.

Note TVIBH does not support Mark VIe I/O packs.

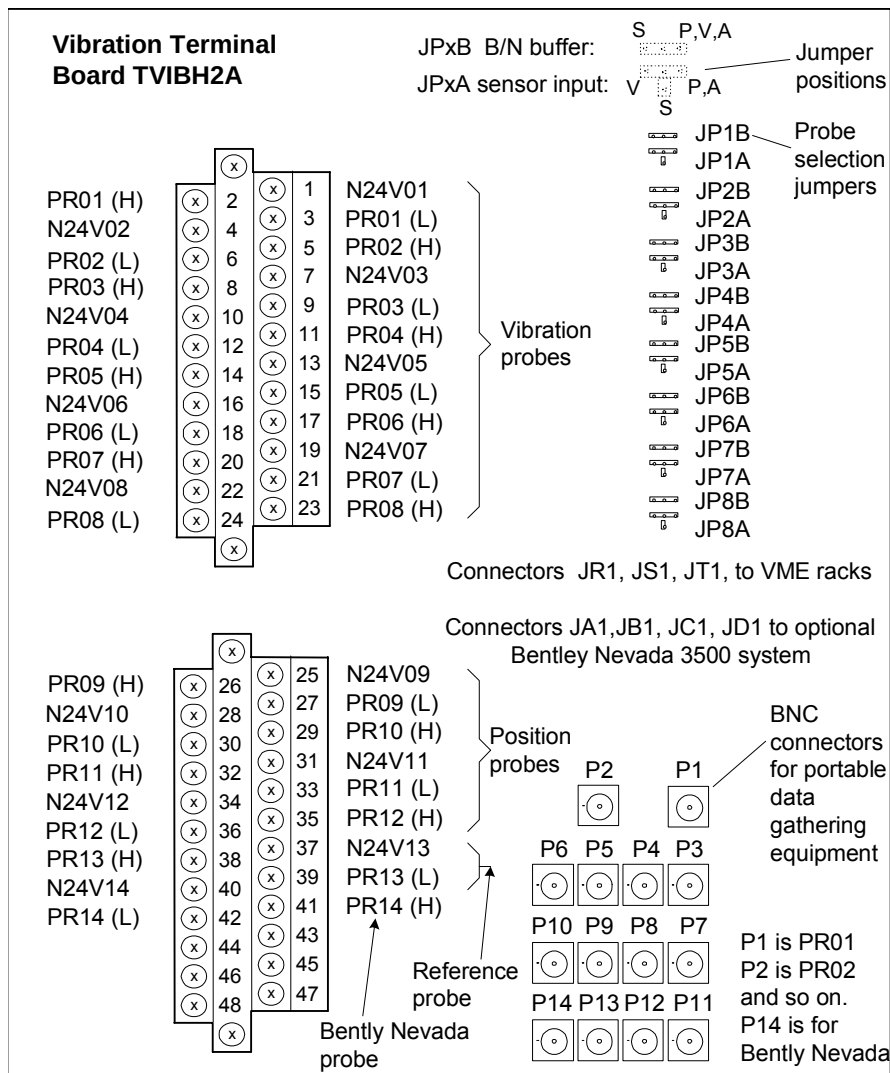


Vibration Terminal Board, Processor Board, and Cabling

Installation

Connect the wires for the 14 vibration probes to the two terminal blocks, three wires per probe. In simplex systems, connect the TVIB1 JR1 connector to VVIB J3 on the VME rack and the TVIB JR1 connector to VVIB J4. In TMR systems, connect the VVIB JR1, JS1, and JT1 connectors to the R, S, and T VVIBs. Use jumpers JP1 through JP8 to select the probe type for the first eight probes. Optionally, connect TVIB to a Bently Nevada system using connectors JA1, JB1, JC1, and JD1.

Note Permanent cable connections to BNCs P1 through P14 are not made.



		Connector Pin Assignments				Px, BNC
Ckt	Sensor	Conn	Comm	Sign	Shld	Connector
01	Vib 1	JA1	2	3	4	P1
02	Vib 2	JA1	6	7	8	P2
03	Vib 3	JA1	10	11	12	P3
04	Vib 4	JA1	24	23	22	P4
05	Vib 5	JB1	2	3	4	P5
06	Vib 6	JB1	6	7	8	P6
07	Vib 7	JB1	10	11	12	P7
08	Vib 8	JB1	24	23	22	P8
09	Pos 1	JC1	2	3	4	P9
10	Pos 2	JC1	6	7	8	P10
11	Pos 3	JC1	10	11	12	P11
12	Pos 4	JC1	24	23	22	P12
13	Ref probe	JD1	3	1	2	P13
14	B/N only	JD1	9	5	4	P14

Jumper JPxA:
S = Seismic
V = Velomitor
P = Proximitor
A = Accelerometer

Jumper JPxB:
S = Seismic
V = Velomitor
P = Proximitor
A = Accelerometer

Terminal Board TVIB Wiring

Operation

TVIB supports Proximitor[®], Seismic, Accelerometer, and Velomitor[®] probes supplied by Bentley Nevada. Power for the vibration probes comes from the VVIB boards in simplex or TMR mode. The probe signals return to VVIB where they are A/D converted and sent over the VME bus to the controller. Vibration, eccentricity, and axial position alarms and trip logic are generated in the controller.

Terminal Board TVIBH2A

Vib. or pos. prox. (P), or seismic (S), or accel (A), or velometer (V)

Eight of the above ccts.

Position prox

Reference or keyphasor prox.

One of the above ccts for Mark VI
(Two of the above ccts for B/N)

Vibration Board VVIB

28 V dc

Amp

A/D

To controller

Sampling type A/D converter (16 bit)

Same as <S>

TMR Applications

Same as <T>

Four cables to Bently Nevada 3500 system

GEH-6421M Mark VI Turbine Control System Guide Volume II

Specifications

Item	Specification		
Number of Channels	13 probes: 8 vibration, 4 position, 1 Keyphasor		
Probe Type	Measurement	Range	Accuracy
Proximity	Displacement	0 to 4.5 V pp	±0 .030 V pp
	5 to 200 Hz		
	Displacement	0 to 4.5 V pp	±0 .150 V pp
	200 to 500 Hz		
Seismic	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]
	5 to 200 Hz		
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]
	200 to 500 Hz		
Velomitor	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]
	5 to 200 Hz		
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]
	200 to 500 Hz		
Accelerometer	Velocity (track filter)	0 to 2.25 V p	±0 .015 Vp
	10 to 233 Hz		
Position	Position	-.5 to -20 V dc	±0.2 V dc
	Air gap (average)		
Phase	Degrees		
	0 to 360 degrees ±2 degrees		
	Up to 14,000 rpm		
	(1X vibration component with respect to key slot)		
Probe power	-24 V dc from the -28 V dc bus; each probe supply is current limited		
	12 mA load per transducer		
Rated RPM	If greater than 4,000 rpm, can use eight vibration channels, (others can be prox/position)		
	If less than 4,000 rpm, can use 16 vibration channels, and other probes		
Buffered outputs	Amplitude accuracy is 0.1% for signal to Bently Nevada* 3500 vibration analysis system		
Size	33.0 cm high x 17.8 cm wide (13 in. x 7 in.)		

Diagnostics

Diagnostic tests are performed on the terminal board components by VVIB as follows:

- Diagnostics perform a high/low (hardware) limit check on the probe input signals and a high/low system (software) limit check. These limits create faults.
- A probe fault, alarm, or trip condition will occur if either of an X or Y probe pair exceeds its limits.
- Position inputs for thrust wear protection, differential expansion, and eccentricity are monitored similar to the vibration inputs except only the dc component is used for a position indication. If a maximum limit is exceeded a fault is created.

Fourteen BNC connectors on TVIB provide buffered signals available to portable data gathering equipment for predictive maintenance purposes. Buffered outputs have unity gain, 10 Ω internal impedance, and can drive loads up to 1500 Ω .

Configuration

Jumpers JP1A through JP8A select the type of the first eight probes as follows:

- S = Seismic
- V = Velocity
- P = Proximity
- A = Accelerometer

Refer to the *Installation* section for more information.

DVIB Simplex Vibration Input

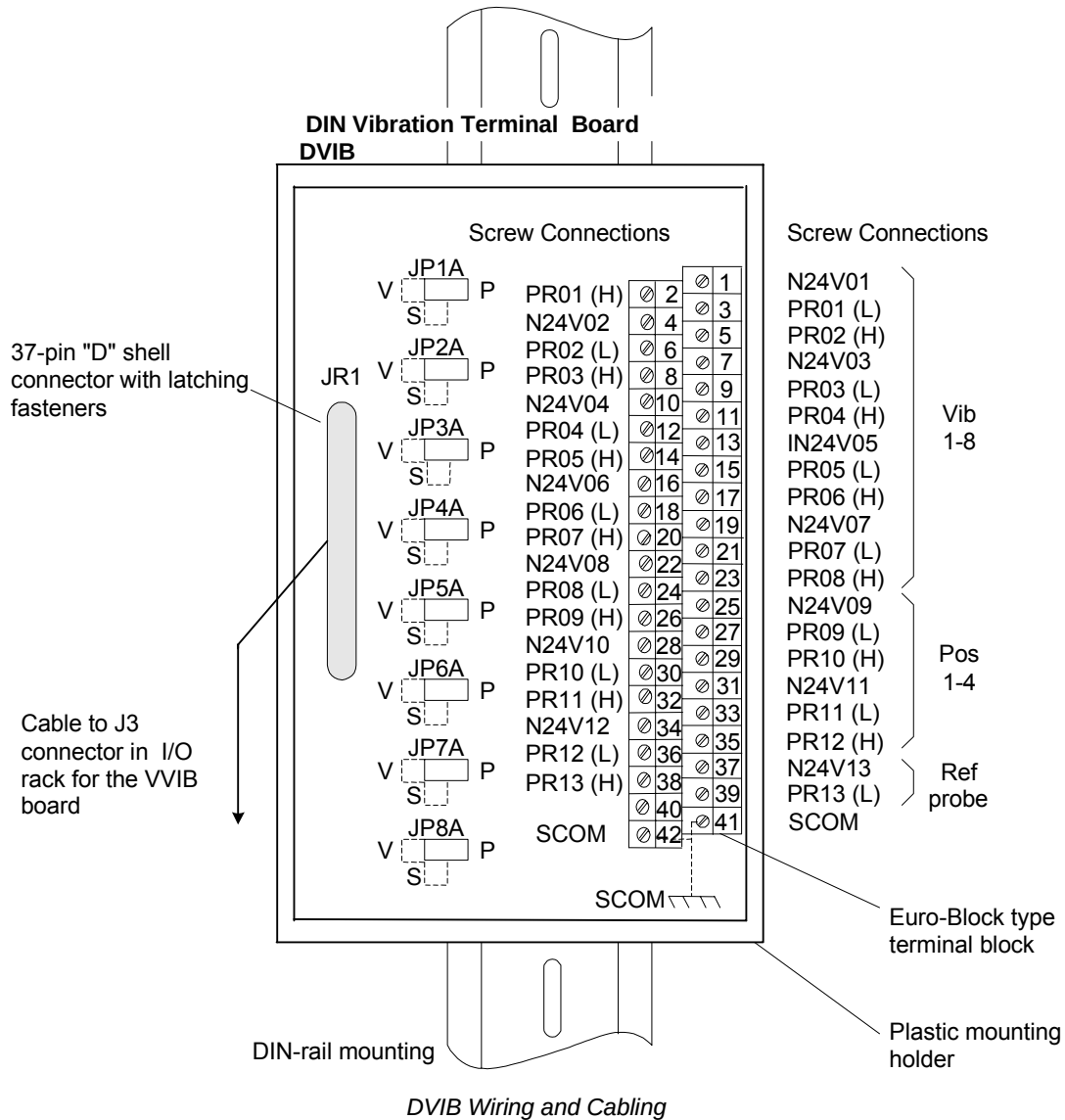
Functional Description

The Simplex Vibration Input (DVIB) terminal board is a compact vibration terminal board for DIN-rail mounting. It is designed to meet UL 1604 specification for operation in a 65°C Class 1, Division 2 environment. DVIB accepts 13 vibration probes, including 8 vibration inputs, 4 position inputs, and 1 Keyphasor input. It connects to the VVIB processor board with a 37-pin cable identical to those used on the larger TVIB terminal board. VVIB accommodates two DVIB boards.

Note Only a simplex version is available.

Installation

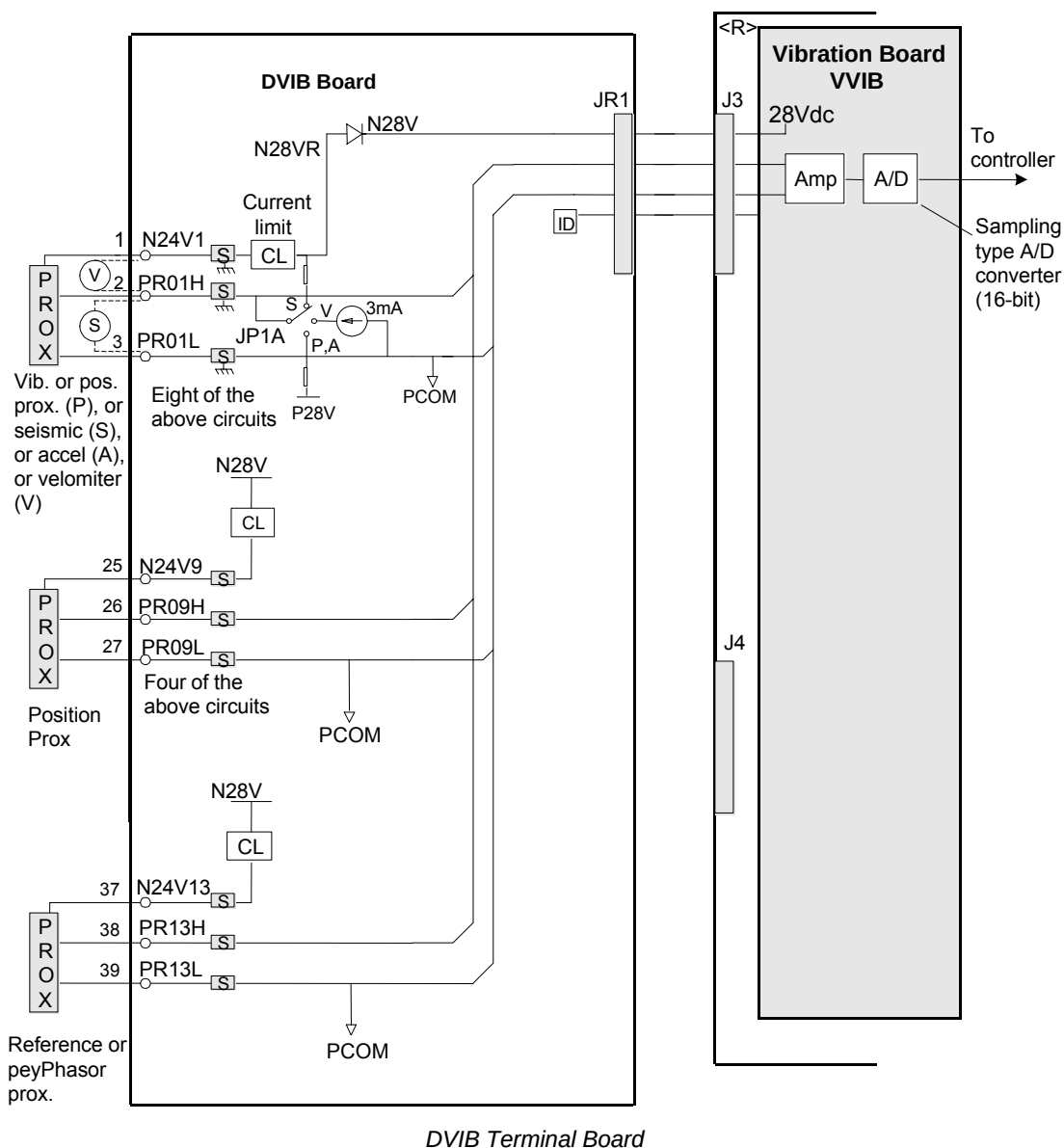
Mount the plastic holder on the DIN-rail and slide the DVIB board into place. Connect the wires for the vibration probes to the terminal block, which has 42 terminals. Typically #18 AWG shielded twisted triplet wiring is used. Two screws, 41 and 42, are provided for the SCOM (ground) connection, which should be as short distance as possible.



Operation

The eight vibration inputs on each DVIB can be applied as either Proximitor, accelerometer, seismic (velocity), or Velomitor[®] inputs. Jumpers on DVIB assign a specific vibration sensor type to each input point, with the seismic type assigned to point (S), the Velomitor type assigned to point (V), and the Proximitor and accelerometer types sharing point (P/A). The Proximitor reads a shaft keyway to generate a once per revolution Keyphasor input for phase angle reference.

On DVIB, the high frequency decoupling to ground on all signals is the same as on TVIB. An on-board ID chip identifies the board to VVIB for system diagnostic purposes.



Specifications

Item	Specification		
Number of Channels	13 probes: 8 vibration, 4 position, 1 Keyphasor		
Probe Type	Measurement	Range	Accuracy
Proximity	Displacement	0 to 4.5 V pp	±0 .030 V pp
	5 to 200 Hz		
	Displacement	0 to 4.5 V pp	±0 .150 V pp
	200 to 500 Hz		
Seismic	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]
		5 to 200 Hz	
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]
		200 to 500 Hz	
Velomitor	Velocity	0 to 2.25 V p	Max [2% reading, ±0.008 Vp]
		5 to 200 Hz	
	Velocity	0 to 2.25 V p	Max [5% reading, ±0.008 Vp]
		200 to 500 Hz	
Accelerometer	Velocity (track filter)	0 to 2.25 V p	±0 .015 Vp
	10 to 233 Hz		
Position	Position	-.5 to -20 V dc	±0.2 V dc
	Air gap (average)		
Phase	Degrees		
	0 to 360 degrees ±2 degrees		
	Up to 14,000 rpm		
	(1X vibration component with respect to key slot)		
Probe power	-24 V dc from the -28 V dc bus; each probe supply is current limited		
	12 mA load per transducer		
Rated RPM	If greater than 4,000 rpm, can use eight vibration channels, (others can be prox/position)		
	If less than 4,000 rpm, can use 16 vibration channels, and other probes		
Buffered outputs	Amplitude accuracy is 0.1% for signal to Bently Nevada* 3500 vibration analysis system		
Size	33.0 cm high x 17.8 cm wide (13 in. x 7 in.)		

Diagnostics

Diagnostic tests are performed on the terminal board components by VVIB as follows:

- Diagnostics perform a high/low (hardware) limit check on the probe input signals and a high/low system (software) limit check. These limits create faults.
- A probe fault, alarm, or trip condition occurs if either of an X or Y probe pair exceeds its limits.
- Position inputs for thrust wear protection, differential expansion, and eccentricity are monitored similar to the vibration inputs except only the dc component is used for a position indication. If a maximum limit is exceeded a fault is created.

Buffered signals for portable data gathering equipment or external vibration analysis equipment are not available as with the TVIB board.

Configuration

Jumpers JP1A through JP8A select the type of the first eight probes as follows:

- S = Seismic
- V = Velocity
- P = Proximity
- A = Accelerometer

Refer to the *Installation* section for more information.

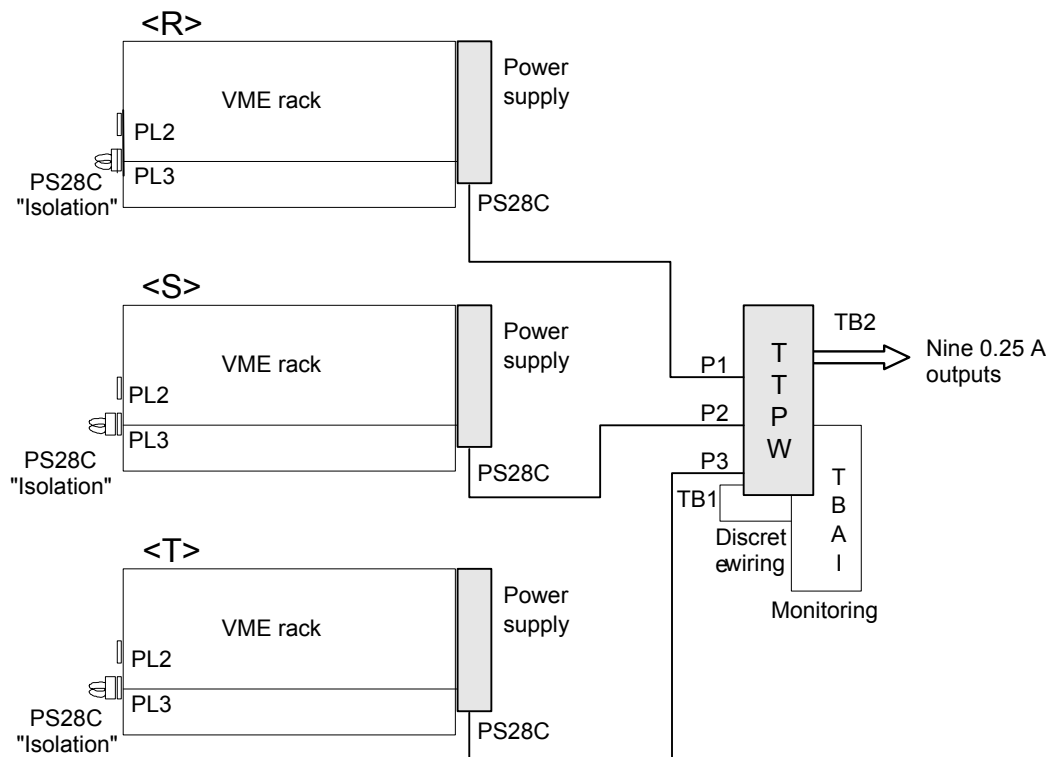
Notes

TTPW Power Conditioning Board

TTPW Power Conditioning

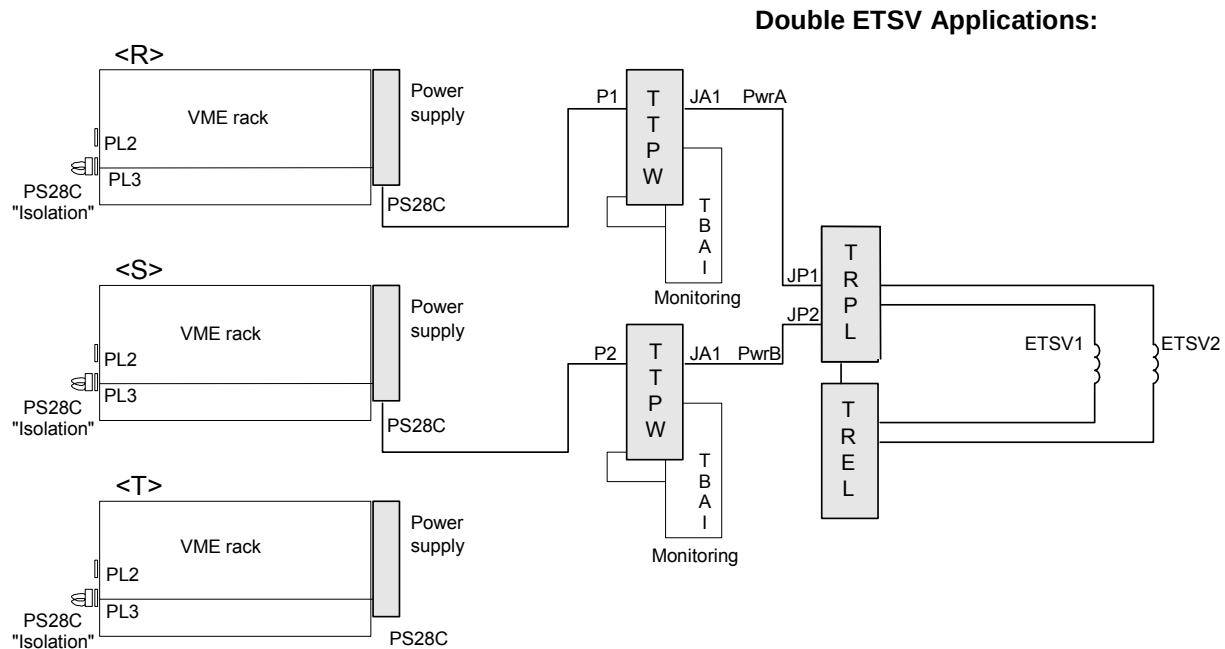
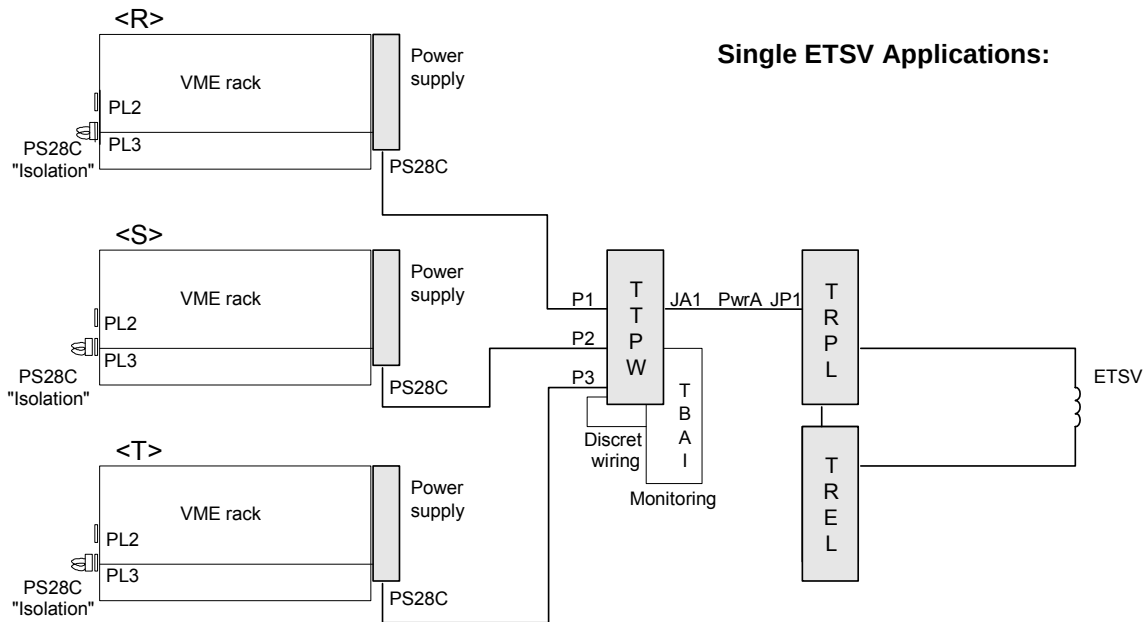
Functional Description

The Power Conditioning (TTPWH1A) terminal board power conditioning board provides branch circuit protection and distribution between one or more Mark* VI rack mounted +28 V dc power supplies and discrete wiring to peripheral devices. The H1A has three 2-pin inputs for +28 V dc from the Mark VI power supply. It provides diode OR selection between the three inputs to power the +28 V dc outputs. Outputs are rated 22 – 30 V dc, 0 – 0.25 A individually and capable of parallel operation. There is high frequency isolation between the inputs and the outputs and the voltage drop is less than +4 V dc when delivering rated current.



TTPWH1A Application Diagram

Large steam turbines use 24 V dc electrical trip solenoid valves (ETSV). Power for these valves is provided to the TRPL and TREL trip boards by a power transition board TTPW. Wiring from the rack power supplies, through TTPW, to the trip board is shown in the figure.

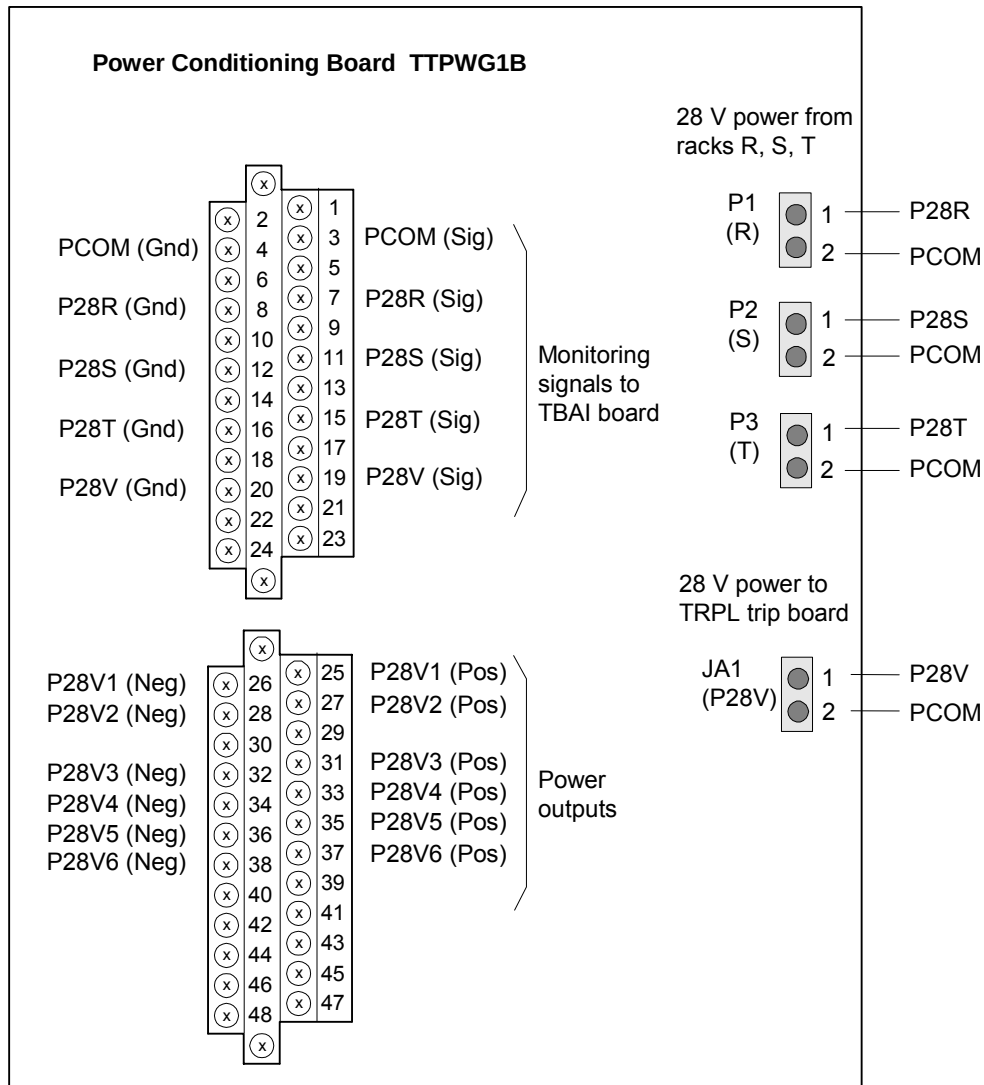


TTPWG1B Wiring to the ETSV

Installation

TTPWG1B

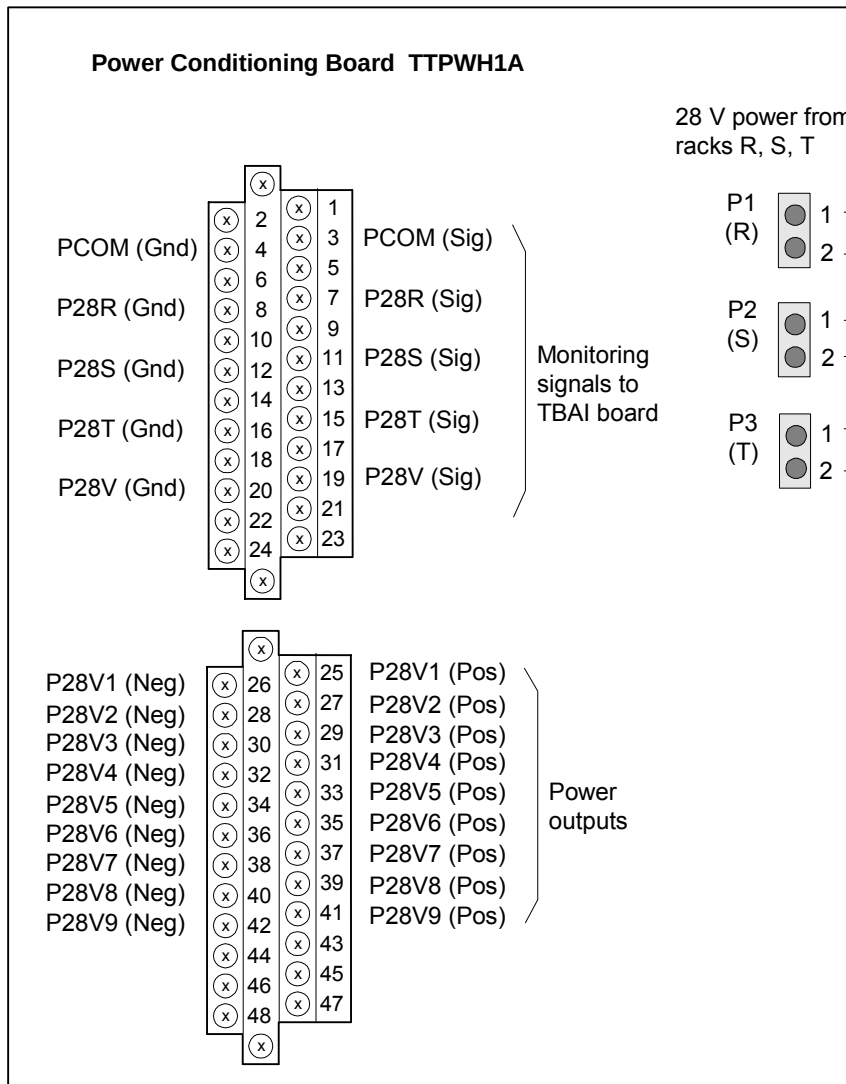
Three 28 V dc supplies are wired from I/O racks R, S, and T to plugs P1, P2, and P3. The primary 28 V dc output comes from plug JA1 and is wired to the trip board TRPL. The power monitoring signals are wired to the top terminal block (TB1) and go to an analog input board. The secondary voltage outputs are wired to the lower terminal block (TB2) as shown in the following figure.



TTPWG1B Board with Wiring and Cabling

TTPWH1A

Three 28 V dc supplies are wired from I/O racks R, S, and T to plugs P1, P2, and P3. The power monitoring signals are wired to the top terminal block (TB1) and go to an analog input board. The secondary voltage outputs are wired to the lower terminal block (TB2) as shown in the following figure.

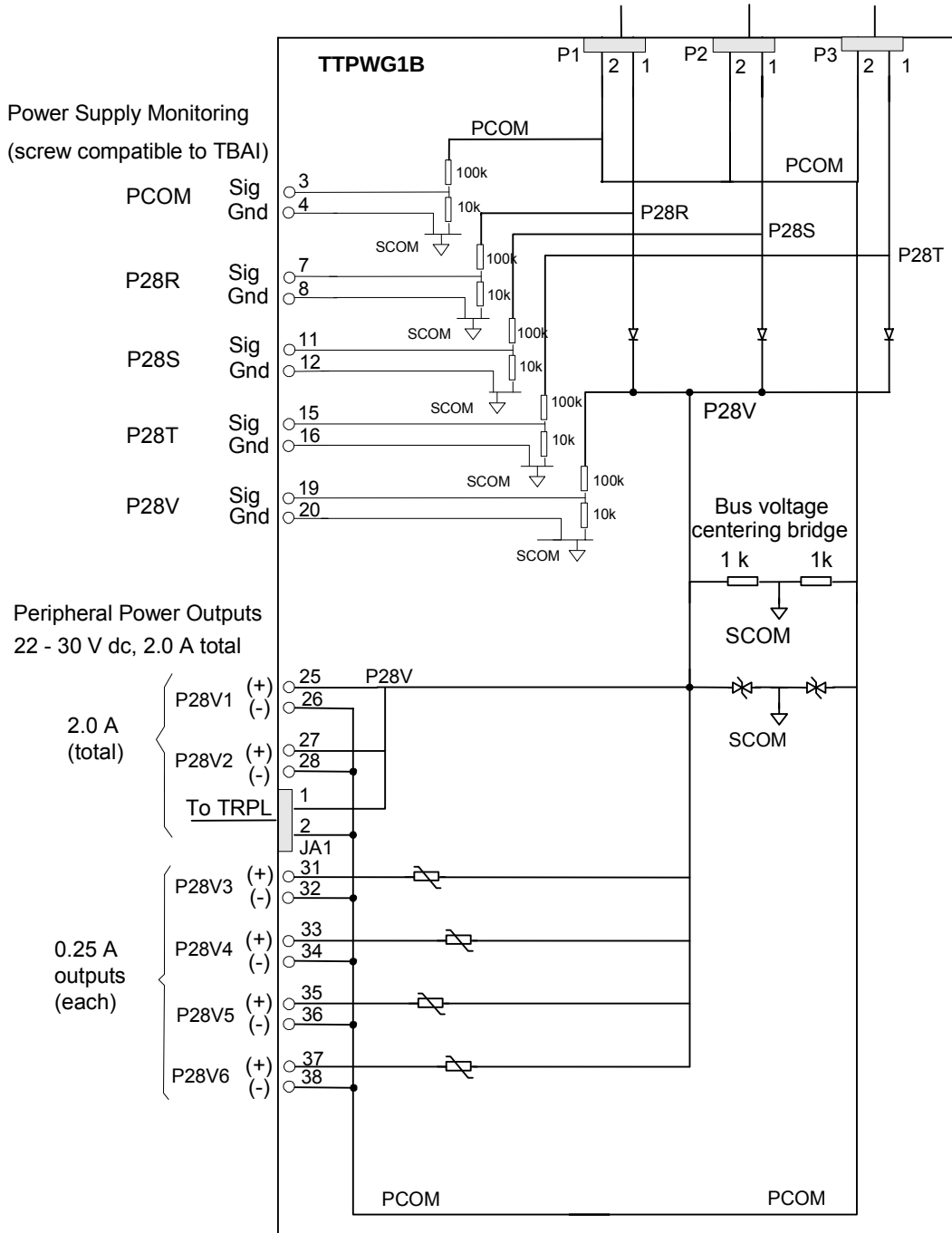


TTPWH1A Wiring and Cabling Diagram

Operation

TTPWG1B

The turbine ETSV is a 24 V dc device with a 24 watt, 20-22 ohm coil. Power is supplied from the three I/O rack supplies to TTPWG1B, where the three 28 V supplies are diode ORed to produce a single 28 V dc output. The primary output is 0 - 2 A (total), 22 - 30 V dc, and there are four secondary outputs of 0.25 A each.



TTPWG1B Board Diagram

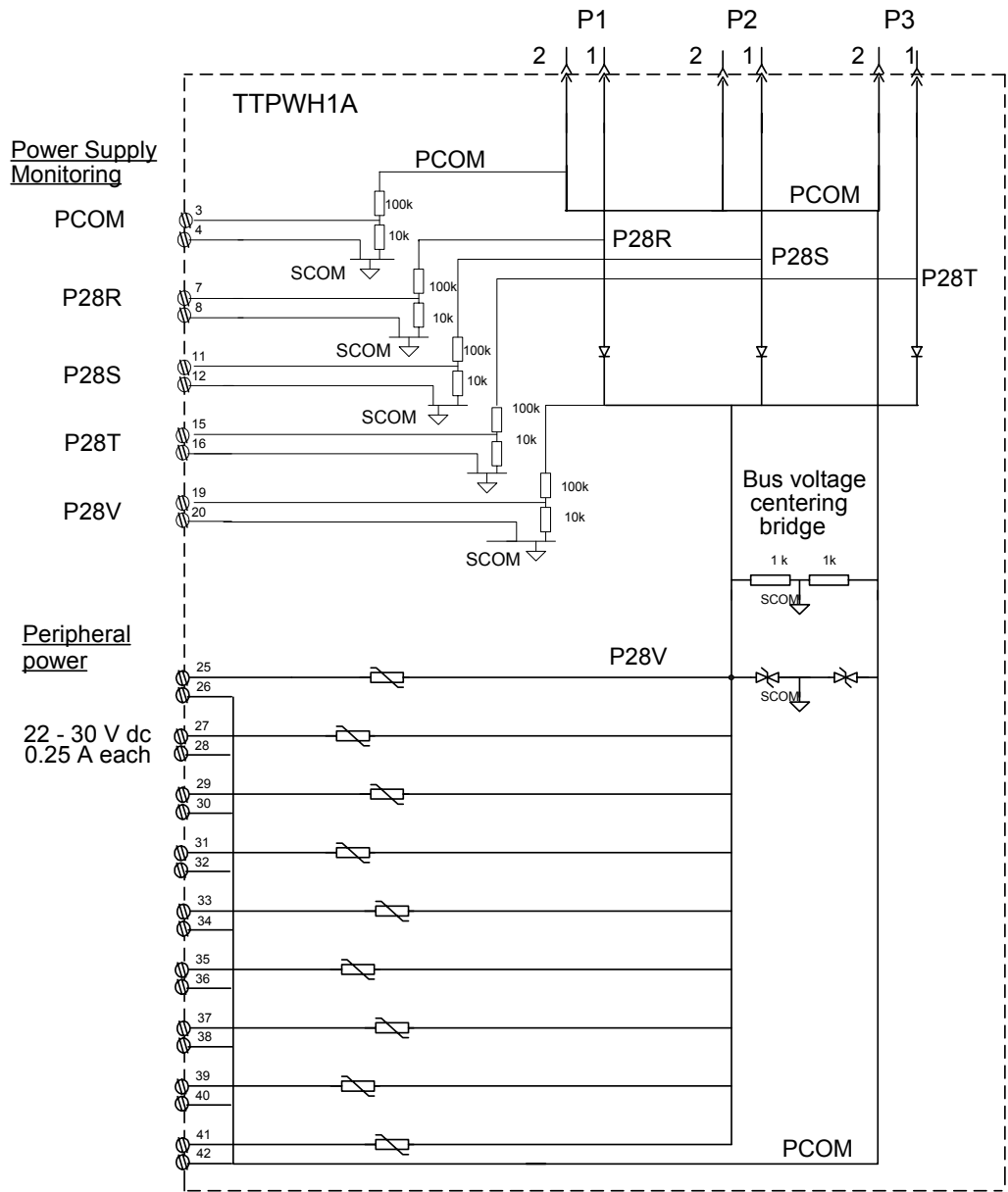
TTPWH1A

The TTPWH1A power conditioning board provides branch circuit protection and distribution between one or more Mark VI rack mounted +28 V dc power supplies and discrete wiring to peripheral devices. The H1A has three 2-pin inputs for +28 V dc from the Mark VI power supply. It provides diode or selection between the three inputs to power the +28 V dc outputs. Outputs are rated 22 – 30 V dc, 0 – 0.25 A individually and capable of parallel operation. There is high frequency isolation between the inputs and the outputs and the voltage drop is less than +4 V dc when delivering rated current.

Typical applications power the H1A from the P28C output of the VME rack power supply. When this is done, the isolation jumper on the rack is placed in the isolated position removing all connections between the P28C output and the rack. The TTPWH1A then provides a resistive bridge to ground to center the power circuit with respect to ground. Voltage feedback monitoring signals are provided using 0.1% resistors allowing monitoring of three input voltages, output voltage, and voltage between PCOM and SCOM.

Note The TTPWH1A internal signal paths are shown in the figure. Nine current limited 0.25 A outputs are provided and may be paralleled for higher current applications.

The +28 V dc power source should have an isolated common (return), especially if the load is external to the cabinet and is grounded. The rack power supplies are wired through TTPWH1A to the trip board.



TTPWH1A Board Diagram

Specifications

TTPWH1A Specification

Item	Description
Inputs	Three 28 V dc inputs from the VME rack power supplies
Outputs	Nine current limited outputs of 0.25 A, 22 – 30 V dc, 28 V dc nom.
Monitoring	Three 28 V dc inputs Output 28 V dc power PCOM voltage
Accuracy	Resistors in measuring circuits are 0.1%

Item	Description
Inputs	Three 28 V dc inputs from the VME rack power supplies
Outputs	Three outputs with total of 2.0 A, 22 – 30 V dc, 28 V dc nom. (to TRPL board) Four current limited outputs of 0.25 A, 22 – 30 V dc, 28 V dc nom
Monitoring	Three 28 V dc inputs Output 28 V dc power PCOM voltage
Accuracy	Resistors in measuring circuits are 0.1%

Diagnostics

The five monitored voltages are wired to an analog input terminal board, TBAI. The I/O processor board, VAIC, creates a fault if an input signal goes out of configured limits, either high or low.

Configuration

There are no switches or jumpers on the power conditioning boards. On the VME rack power supply, place the P28C isolation jumper in the isolated position.

Alarms

The alarms associated with this board depend on system use of the feedback signals.

VME Rack Power Supply

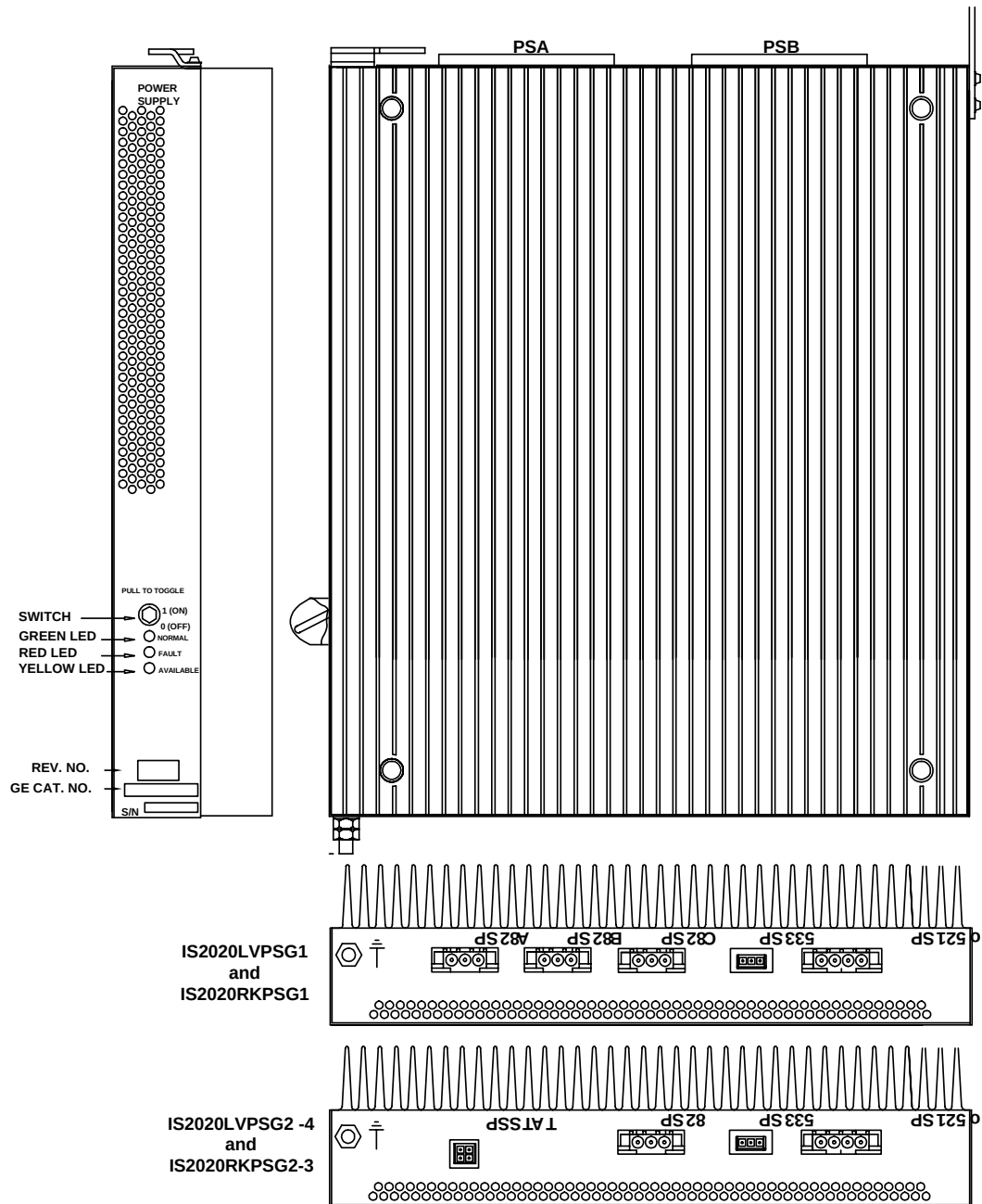
VME Rack Power Supply

Functional Description

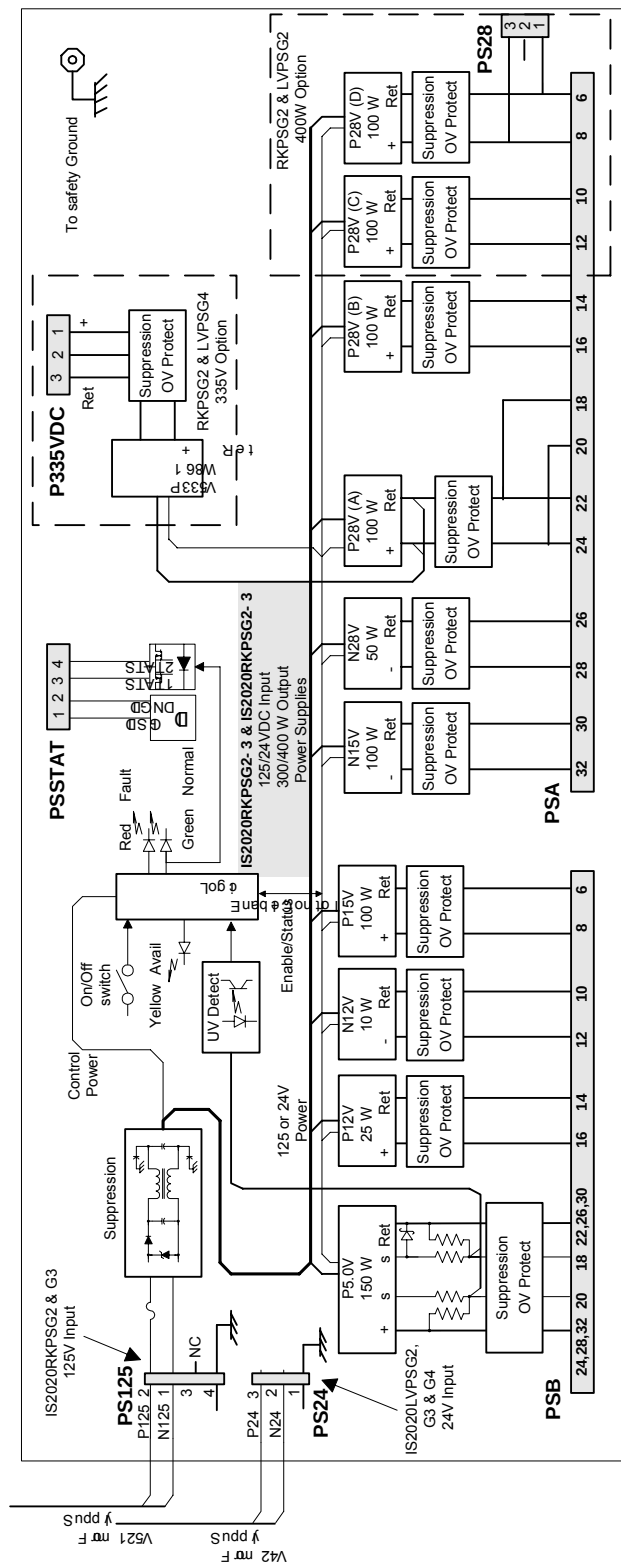
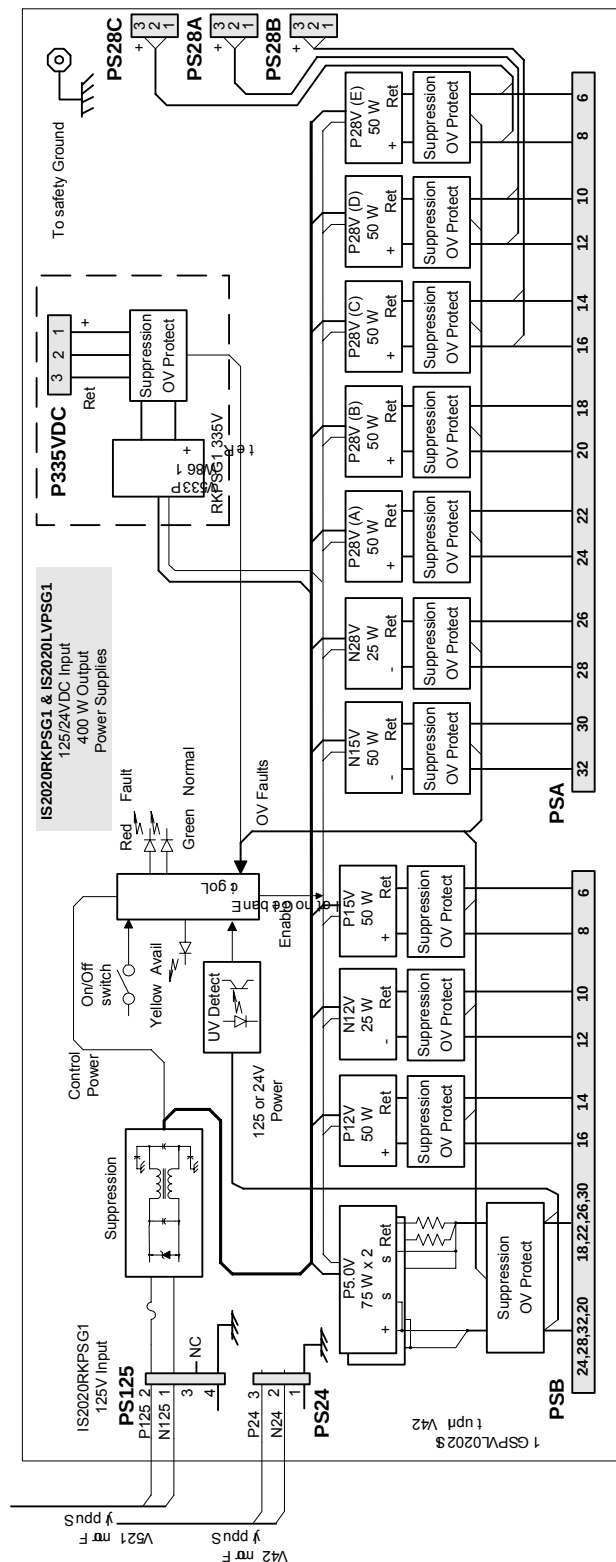
The Mark* VI VME rack power supply mounts on the side of the VME control and interface racks. It supplies +5, ± 12 , ± 15 , and ± 28 V dc to the VME backplane, and an optional 335 V dc output for powering flame detectors connected to TRPG.

Two supply input voltage selections are available. There is a 125 V dc input supply that is powered from a Power Distribution Module (PDM) and a low voltage version for 24 V dc operation.

Note A different power supply is used on the stand-alone control rack which only powers the Mark VI controller, VDSK, and VCMI.



VME Rack Power Supply types G1 and G2, Front, Side, and Bottom Views



Block Diagram of RKPS and LVPS versions of VME Power Supply

There are currently seven major variations of the VME rack power supply. These variations provide different power supply input and output requirements. The following table defines these variations.

IS2020 Part Number	Input Voltage	Output Rating	+28V PSA Outputs	+28V Remote Outputs	PS335 Output	Status ID Output	Support Redundant Operation
LVPSG1	24 V dc	400W	Qty. 5	Qty. 3	No	No	No
RKPSG1	125 V dc	400W	Qty. 5	Qty. 3	Yes	No	No
RKPSG2*	125 V dc	400W	Qty. 5	Qty. 1	Yes	Yes	Yes
RKPSG3*	125 V dc	400W	Qty. 5	Qty. 1	No	Yes	Yes
LVPSG2*	24 V dc	400W	Qty. 5	Qty. 1	No	Yes	Yes
LVPSG3*	24 V dc	300W	Qty. 3	None	No	Yes	Yes
LVPSG4*	24 V dc	300W	Qty. 3	None	Yes	Yes	Yes

* Newer design power supplies

With the exception of the number of remote 28 V outputs, the RKPSG2 and LVPSG2 are designed to be direct replacements for the RKPSG1 and LVPSG1 respectively. These two supplies have been replaced with the newer designs (marked with asterisk in the table above).

Installation

The power supply is mounted to the right-hand side of the VME rack on a sheet metal bracket. The dc input, 28 V dc output, and 335 V dc output connections are at the bottom. The newer design also has a status connector on the bottom. Two connectors, PSA and PSB, at the top of the assembly mate with a cable harness carrying power to the VME rack.

Each of the five 28 V dc power modules supplies a section of the VME rack. These sections are labeled A, B, C, D, E, and F. The P28C output or PS28 at the bottom of the power supply can be used to power an external peripheral device. To do this the jumper plug shown on the bracket to the left of the rack must be moved from the *Normal* position to the *Isolated* position below.

The fan is only used when the controller is mounted in the rack. It is powered from the top connector on the same bracket, located on the left side of the rack.



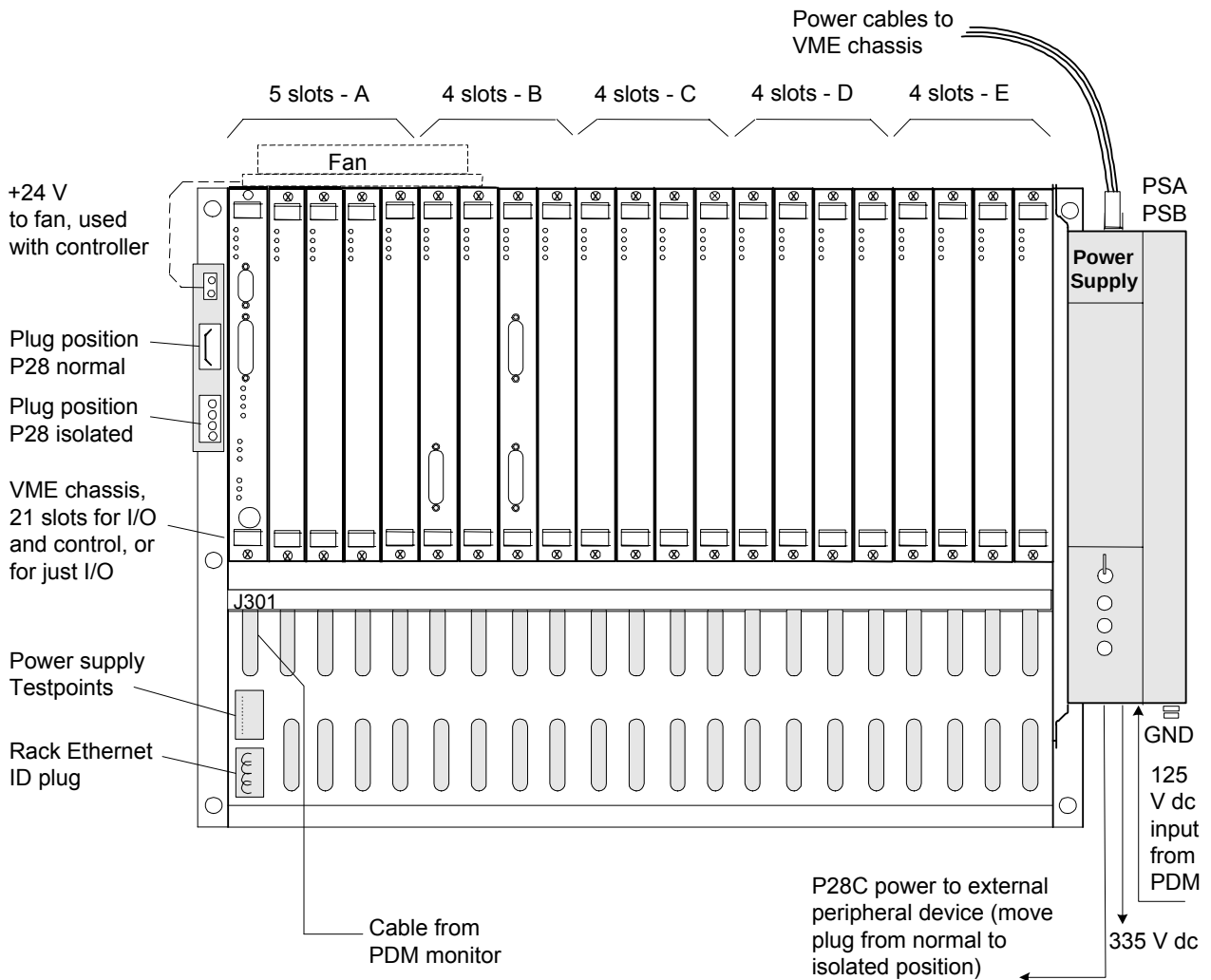
Warning

To prevent electric shock, turn off power to the RPSM to be replaced, then test to verify that no power exists on the module before touching it or any connected circuits.



Caution

To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.



Power Supply, VME Chassis, and Cabling to External Devices

➤ **To remove the power supply**

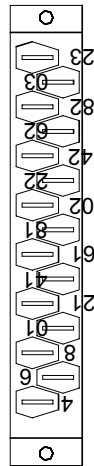
- 1** Loosen the PSA/PSB bracket captive fastener at the top front of the module.
- 2** Separate the PSA/PSB bracket assembly from the RPSM.
- 3** Disconnect the bottom connectors.
- 4** Loosen the two front sheet metal bracket captive fasteners.
- 5** Pull the sheet metal bracket/power module assembly forward, disconnect the four rear side connectors and then slide the assembly off of the control rack.
- 6** Remove the four mounting screws that hold the RPSM to the bracket and remove it.

Note Reinstall the screws and bracket on the control rack if a replacement module is not going to be installed.

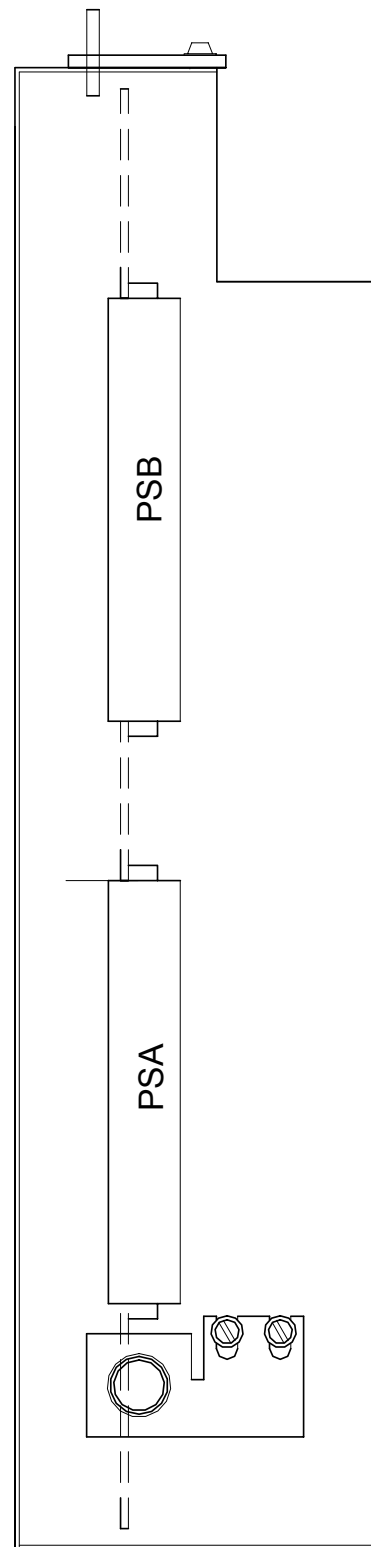
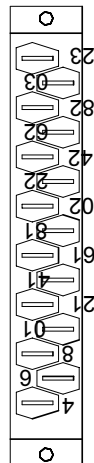
➤ **To install the power supply**

- 1** Locate the supply mounting sheet metal bracket and four mounting screws.
- 2** Position the module on the bracket with the front of the module at the captive fasteners, then install the four mounting screws and tighten.
- 3** Slide the module bracket assembly on to the control rack, connect the four rear side connectors and then push the assembly in to tighten the two front captive fasteners.
- 4** Slide the PSA/PSB assembly rear tab into the slot on the bracket located at the top rear of the RPSM.
- 5** Push the connector assemble into the mating connectors on the top of the RPSM.
- 6** Tighten the PSA/PSB bracket captive fastener.
- 7** Connect the power supply bottom connectors.

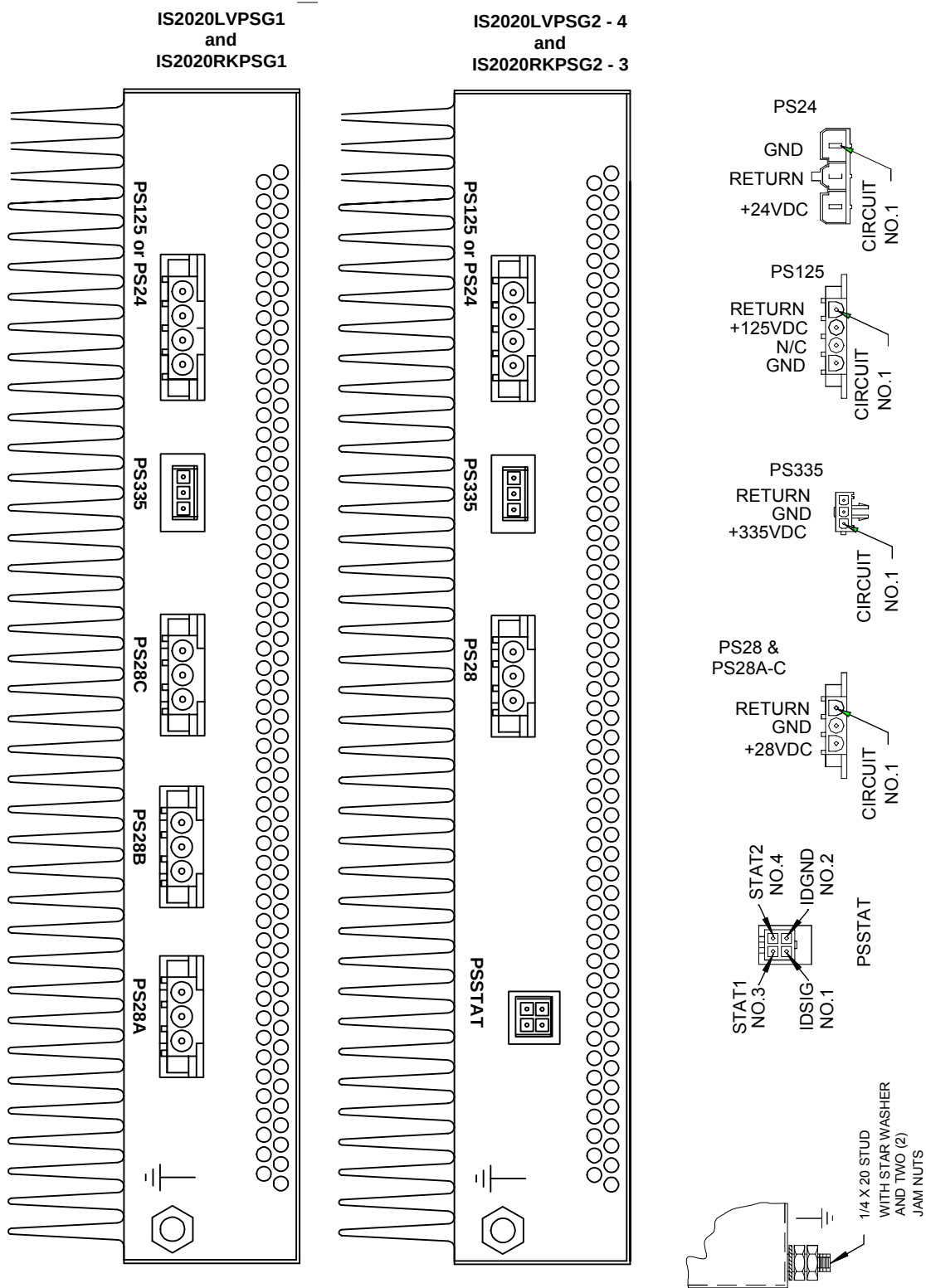
PIN32 5V
 PIN30 5V RET
 PIN28 5V
 PIN26 5V RET
 PIN24 5V
 PIN22 5V RET
 PIN20 5V
 PIN18 5V RET
 PIN16 +12V
 PIN14 RET
 PIN12 -12V
 PIN10 RET
 PIN8 +15V
 PIN6 RET
 PIN4 N/C
 PIN2 N/C



PIN32 -15V
 PIN30 RET
 PIN28 -28V
 PIN26 RET
 PIN24 28VA
 PIN22 RET
 PIN20 28VB
 PIN18 RET
 PIN16 28VC
 PIN14 RET
 PIN12 28VD
 PIN10 RET
 PIN8 28VE
 PIN6 RET
 PIN4 N/C
 PIN2 N/C



Power Supply, Top Connectors



Power Supply, Bottom Connectors

Operation

The VME Rack power supply has only one user control, the power switch, and three status LED indicators. The power switch provides front-panel control of the power supply output voltages and when toggled serves as a fault reset. The yellow, red and green LEDs indicate the status of the input power, fault presence, and normal operation.

Note Newer supply designs also have a status output that mimics the status of the green LED and an ID output that uniquely identifies the supply back to the system.

Power Switch

The front panel power switch is a locking type that must be pulled out to change position. This switch is a low voltage control to enable or disable the output voltages. If the red LED is ON indicating a fault condition the power switch can be toggled OFF and then back ON again to clear the fault. The fault will only be cleared if the condition that caused it no longer exists.

Yellow LED

When the power switch is OFF the yellow LED will indicate the status of the input power. If this LED is ON there is power present on the supply input connector. For the newer design, the yellow LED will only turn ON if the input voltage is above the input under-voltage fault threshold.

Red LED

This LED will only be ON if there is input power, the power switch is ON, and a fault has been detected.

Green LED/Status Output

If there is input power, the power switch is ON, and there are no detectable faults, the Green LED will be ON. The newer designs also have a status output that mimics the status of this LED. The status output is a NO solid-state relay contact that will be CLOSED when the green LED is ON.

Fault Conditions

There are three classes of power supply faults:

- Those that transiently shutdown an output
- Those that require some reset action to clear
- Permanent failures that require the replacement of the supply.

This section describes the first two fault classes and assumes the cause of the fault is external. For a detailed fault diagnostics, refer to the section, *Diagnostics and Troubleshooting*.

Note When the external condition causing the current limit condition is corrected, the output voltage will return to normal.

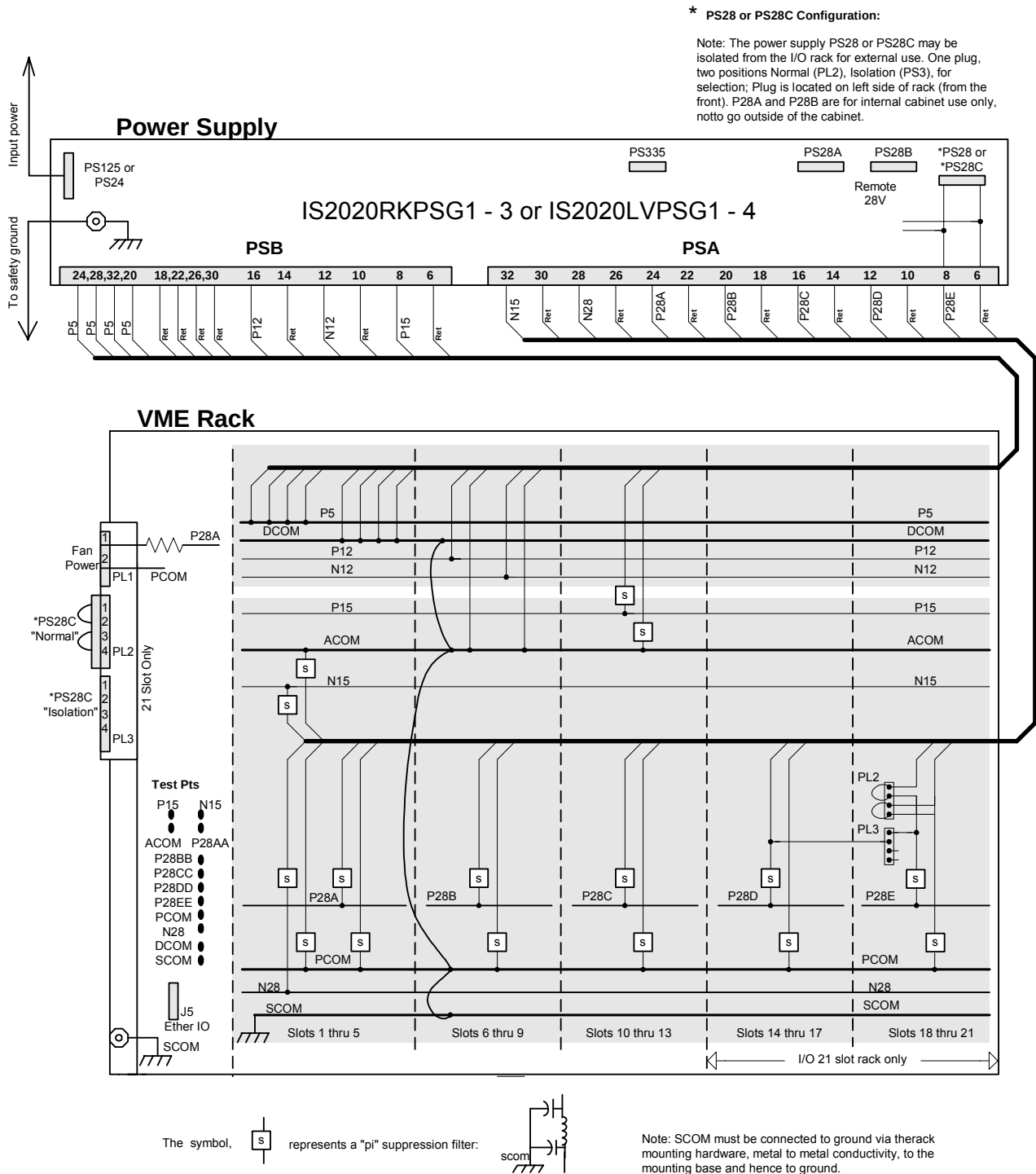
If an overcurrent condition exists on an output, the voltage on that output will fold back as required to maintain the constant current limit output. For every output other than the 5 V supply, this condition is not detectable at the supply and the green LED will remain ON. Detection of a low output voltage due to excessive output current has to be detected at the system level through the power supply voltage monitoring. The newer design also has an over temperature monitor of the output modules and a current limit detector on the optional 335V supply. These additional fault detectors may cause the red LED to come on when an output is in current limit but the red LED will also go out when the output voltage returns to normal.

The 5 V current limit is a special case due to the 5 V under-voltage detector. If the current limit causes the 5 V output voltage to fold back below the UV threshold, all of the other outputs will be disabled until the 5 V output voltage returns to a voltage above the UV threshold.

All of the other faults will shut down one or all of the outputs until the external cause of the fault condition is removed and the supply is reset. A reset can be initiated through the front panel power switch or by removing and reapplying input power to the supply. Output over-voltage faults on the newer design require the removal of input power for a minimum of one minute to reset the fault once the source of the fault has been removed. Below is a power supply fault summary.

- Input under-voltage (Latched)
- Input over-voltage (Newer Design Only)
- P5 output under-voltage
- Output over-voltage (Latched)
- Over temperature (Newer Design Only)

The following figure shows the power supply connections to the VME rack and the distribution of the power supply outputs.



VME I/O Rack Power Supply and Cables

Specifications

Item	Description				
Input voltage					
125 V input	70 V to 145 V dc floating supply	Up to 10 V pp ripple			
24 V input	18.5 V to 32 V dc floating supply	Up to 2 V pp ripple			
Input under-voltage	Under-voltage protection provided to prevent supply operation when the input voltage is below the minimum operating level.				
Input over-voltage*	Over-voltage protection provided to prevent supply operation when the input voltage is above the maximum operating level.				
Isolation	True isolation from input to output, 1500 V				
Output voltages	Output Voltage	Voltage Regulation		Capacity	Typical Over
For the RKPSG1 and LVPSG1 supplies	P5	+5 V dc	Less than $\pm 3\%$	150 W	120% $\pm 5\%$
	P15	+15 V dc	Less than $\pm 3\%$	50 W	120% $\pm 5\%$
	N15	-15 V dc	Less than $\pm 3\%$	50 W	120% $\pm 5\%$
	P12	+12 V dc	Less than $\pm 3\%$	50 W	120% $\pm 5\%$
	N12	-12 V dc	Less than $\pm 3\%$	25 W	120% $\pm 5\%$
	P28	+28 V dc	Less than $\pm 5\%$	50 W	120% $\pm 5\%$
	N28	-28 V dc	Less than $\pm 5\%$	25 W	120% $\pm 5\%$
	P335	+335 V dc	Less than $\pm 5\%$	1.68 W	110% to 120%
For the RKPSG2 -3 and LVPSG2 - 4 supplies* Note: P5 on these supplies has remote voltage sensing.	P5	+5 V dc	Less than $\pm 3\%$	150 W	130% $\pm 5\%$
	P15	+15.35 V dc	Less than $\pm 3\%$	100 W	120% $\pm 5\%$
	N15	-15.35 V dc	Less than $\pm 3\%$	100 W	120% $\pm 5\%$
	P12	+12.3 V dc	Less than $\pm 3\%$	25 W	120% $\pm 5\%$
	N12	-12.3 V dc	Less than $\pm 3\%$	10 W	120% $\pm 5\%$
	P28	+28 V dc	Less than $\pm 5\%$	100 W	120% $\pm 5\%$
	N28	-28 V dc	Less than $\pm 5\%$	50 W	120% $\pm 5\%$
	P335	+335 V dc	Less than $\pm 5\%$	1.68 W	110% to 120%
Power sequencing	The 5 V dc supply comes up first, then all the others				
Total Output	Maximum of 400 W				
Total output LVPSG3 & 4 only*	Maximum of 300 W				
Short circuit	Short circuit protection on all power supplies, with self-recovery. Note: A 5 V short circuit on the new design will cause a latched fault.				
Temperature	Ambient air convection cooling 0 to 60°C				
Indicating lights	Green: Normal	Status is OK			
	Red: Fault	Power is applied, but one or more outputs off due to a fault.			
	Yellow: Available	Power is applied, but switch is OFF			
Status output*	NO SSR contact .5 A @ 55 V dc - Closed when the green indicating light is on				
ID tag output*	Dallas DS2502 output. 2502 data = Week and year tested, unit number, part number and revision				

*Only pertain to the newer design power supplies

Diagnostics

Incoming and outgoing voltages and currents are monitored for control and protection purposes. If the red LED is ON, this is not a direct indication that the power supply has failed and has to be replaced. The LED ON could indicate that something is wrong in the system and the fault LED is latched on. The following is a description of the power supply parameters that are monitored and the conditions that can cause faults.

Input Under-voltage (below the minimum operating voltage)

The input voltage has to be above the under-voltage threshold or operation of the supply will be inhibited. For the newer design this is indicated by no LEDs ON. The red LED will come ON and remain on until the input voltage is above the under-voltage threshold and the power switch is toggled. If an under-voltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the input voltage is above the under-voltage threshold and the power switch is toggled.

Note If the supply power switch is turned on in this condition there will be no output voltages.

Input Over-voltage (newer design above maximum operating voltage)

If the supply power switch is turned on in this condition there, will be no output voltages and the red LED will come ON and remain on until the input voltage is below the over-voltage threshold and the power switch is toggled. If an over-voltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the input voltage is below the over voltage threshold and the power switch is toggled.

Note The input voltage has to be below the over-voltage threshold or operation of the supply will be inhibited and the yellow LED will be ON.

5 V Output Under-voltage (typically below 4.7 V)

The P5 output voltage has to be above the under-voltage threshold or operation of the supply will be inhibited, all supply outputs will be turned off, and the red LED will be ON. If an under-voltage fault occurs during normal operation, the outputs will be disabled and the red LED will come ON and remain ON until the output voltage is above the under-voltage threshold.

5 V Output Over-voltage (typically above 6 V)

The P5 output voltage has to be below the over-voltage threshold or operation of the supply will be inhibited. All supply outputs will be latched OFF and the red LED will be ON until the power switch is toggled. For the newer design, this fault must be reset by removing input power to the supply (wait for one minute and re-apply input power).

Output Over-voltage other than P5 (typically above 120%)

The output voltage has to be below the over-voltage threshold or operation of the supply output that is above the threshold will be inhibited (latched OFF) until the power switch is toggled. The red LED will be ON during this fault. For the newer design, this fault must be reset by removing input power to the supply (wait for one minute and re-apply input power).

Output Over-temperature (newer design typically above 100 degrees C)

The modules that supply the output voltage have to be operated below the over-temperature threshold. A specific supply output module operated above the threshold will be inhibited until the temperature is lowered below the threshold. The red LED will be ON during this fault. An over-temperature of the 5 V module will cause a 5 V under-voltage fault.

Troubleshooting

The supply has no field serviceable components. If a supply is found to be defective it must be replaced. The power supply cover should not be removed in the field.

There are only two indications of a problem on the power supply itself. A problem is indicated when there are no LEDs ON or the red LED is ON. Both conditions will be annunciated on the newer designs through the status output.

No LEDs ON is a good indication of an input voltage problem or a defective supply. If the red LED is ON, the cause could be any of the fault conditions listed above or a defective supply. Below is a list of troubleshooting hints.

Note Over-voltage faults on the newer design must be reset by removing input power to the supply, waiting for one minute, and re-applying input power.

No LEDs ON

Verify that the input connector and voltage to the supply are correct. If they are, then replace the supply. Use caution when powering on the replacement supply because the failure could have been caused by a problem in the system.

Red LED ON and system up

This condition indicates that the 5 V power is OK. Use the system diagnostics and or testpoints on the left bottom of the control rack or at the supply connectors to find the faulted outputs. Try and clear the fault with the input power or switch reset. If the green LED comes ON, the fault was a transient one and may come back. If the red LED is still ON, remove the connector supplying the faulted output and reset the supply. If the red LED is still ON, then a defective supply is the most probable cause. If the green LED comes ON, then the problem is most likely in the system.

Red LED ON and system down

This condition indicates that the 5 V power is not OK. In this case, all of the supply outputs should be off. Try and reset the fault with the input power. If the green LED comes on the fault was a transient one and may come back. If the red LED is still ON, remove the PSA/PSB output connector at the top of the supply and reset the supply. If the red LED is still ON, then a defective supply is the most probable cause. If the green LED comes ON, then the problem is most likely in the system.

Green LED ON and system up but one or more of the voltages out of specification

This condition indicates that the 5 V power is OK. Each supply output has a current limit and short circuit protection. This condition could be caused by a short or failed component in the system. Remove the connector supplying the failed output voltage. If the voltage returns to normal this is an indication of a system problem. If the voltage does not return to normal then the most probable cause is a defective supply.

Thermal over-temperature faults (new design only)

Even in the worst case ambient conditions, a thermal fault should not occur if the outputs are not overloaded. A sustained current limit on a supply output will be the most likely cause of a thermal fault.

Configuration

The P28C output or PS28 at the bottom of the power supply can be used to power an external peripheral device. To do this the jumper plug on the bracket to the left of the rack must be moved from the *Normal* position to the *Isolated* position below.

Alarms

Fault	Fault Description	Possible Cause
32	P5=####.## Volts is Outside of Limits. The P5 power supply is out of the specified operating limits	A VME rack backplane wiring problem and/or power supply problem
33	P15=####.## Volts is Outside of Limits. The P15 power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a back plane wiring or VME power supply problem
34	N15=####.## Volts is Outside of Limits. The N15 power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem
35	P12=####.## Volts is Outside of Limits. The P12 power supply is out of the specified operating limits	If "Remote I/O", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem
36	N12=####.## Volts is Outside of Limits. The N12 power supply is out of the specified operating limits	If "Remote I/O", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem
37	P28A=####.## Volts is Outside of Limits. The P28A power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem
38	P28B=####.## Volts is Outside of Limits. The P28B power supply is out of the specified operating limits	If "Remote Control", disable diagnostic and ignore; otherwise probably a VME backplane wiring and/or power supply problem
39	P28C=####.## Volts is Outside of Limits. The P28C power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem
40	P28D=####.## Volts is Outside of Limits. The P28D power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem
41	P28E=####.## Volts is Outside of Limits. The P28E power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem
42	N28=####.## Volts is Outside of Limits. The N28 power supply is out of the specified operating limits	If "Remote Control" disable diagnostic. Disable diagnostic if not used; otherwise probably a backplane wiring and/or power supply problem

Notes

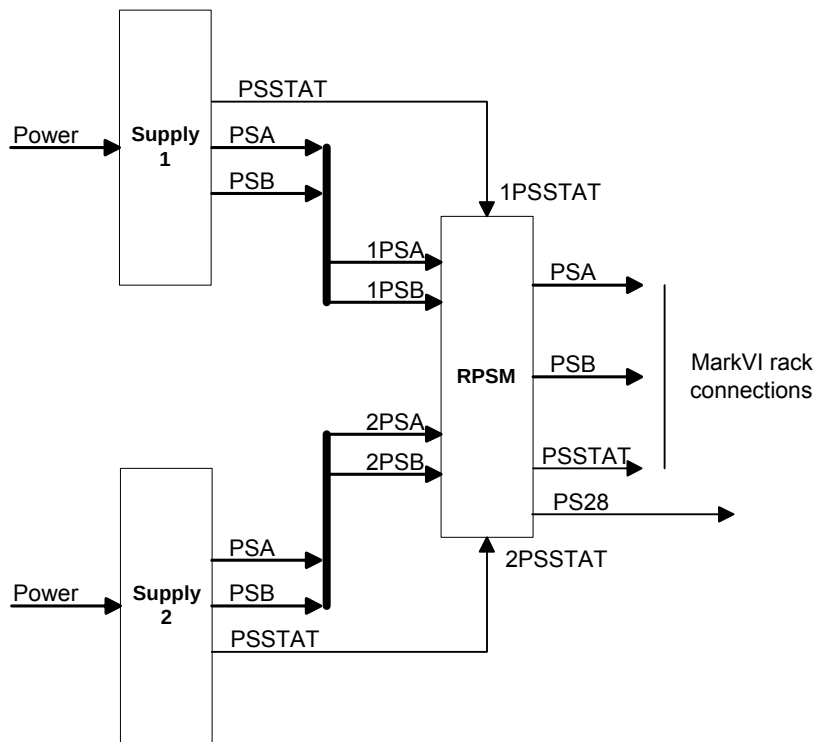
VME Redundant Power Supply

Redundant Power Supply

Functional Description

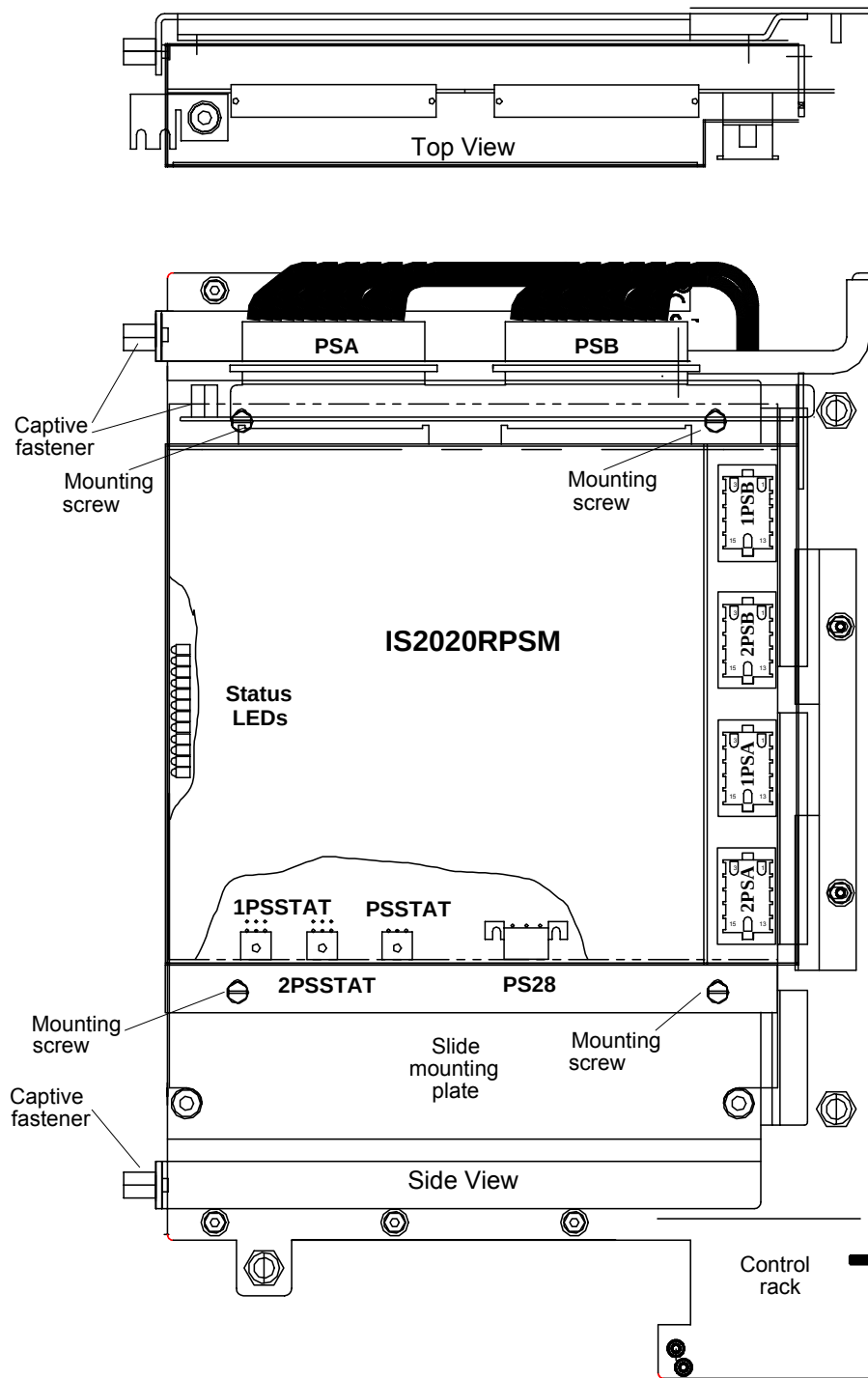
The redundant power supply module (RPSM) parallels two independent power supplies to provide ten output voltages with improved reliability. ORing diodes are used to OR the outputs of one supply with the outputs from the second redundant supply. Nine of the paralleling circuits have an additional current limit function. All output circuits have an LED status indicator.

The following figure shows the power and signal flow for two paralleled power supplies that provide power to a Mark* VI control rack. To provide redundancy, the outputs of each supply are passed into the RPSM, ORed and the redundant voltages are passed out the RPSM outputs. The RPSM module mounts on the side of the control rack in place of the power supply. The two power supplies that feed the RPSM are remotely mounted.



Power Supply and RPSM Signal Flow

Installation



RPSM Module and VME Chassis

The RPSM module is mounted to the right hand side of the VME rack on a sheet metal bracket. The status and 28 V dc output connections are at the bottom. Two connectors, PSA and PSB, at the top of the assembly connect with a cable harness carrying power to the VME rack. The four 15-pin connect-N-Lock connectors at the back side of the module are the primary power feeds from the remotely mounted power supplies.



Warning

To prevent electric shock, turn off power to the RPSM to be replaced, then test to verify that no power exists on the module before touching it or any connected circuits.



Caution

To prevent equipment damage, do not remove, insert, or adjust any connections while power is applied to the equipment.

The RPSM module is mounted to the right hand side of the VME rack on a sheet metal bracket. The status and 28 V dc output connections are at the bottom. Two connectors, PSA and PSB, at the top of the assembly connect with a cable harness carrying power to the VME rack. The four 15-pin connect-N-Lock connectors at the back side of the module are the primary power feeds from the remotely mounted power supplies.

➤ To remove the RPSM

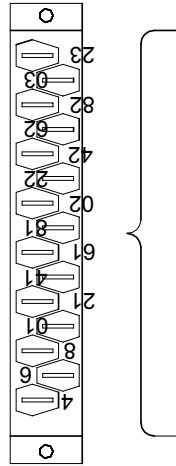
- 1 Loosen the PSA/PSB bracket captive fastener at the top front of the module.
- 2 Separate the PSA/PSB bracket assembly from the RPSM.
- 3 Disconnect the bottom connectors.
- 4 Loosen the two front sheet metal bracket captive fasteners.
- 5 Pull the sheet metal bracket/power module assembly forward, disconnect the four rear side connectors and then slide the assembly off of the control rack.
- 6 Remove the four mounting screws that hold the RPSM to the bracket and remove it.

Note Reinstall the screws and bracket on the control rack if a replacement module is not going to be installed.

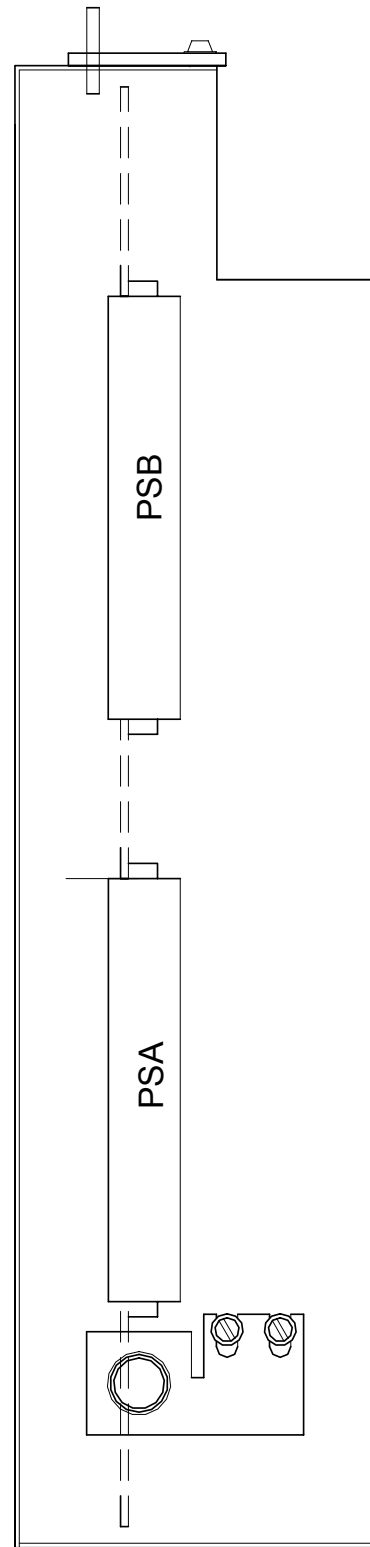
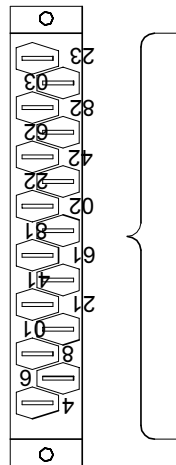
➤ To reinstall the RPSM

- 1 Locate the supply mounting sheet metal bracket and four mounting screws.
- 2 Position the module on the bracket with the front of the module at the captive fasteners, then install the four mounting screws and tighten.
- 3 Slide the module bracket assembly on to the control rack, connect the four rear side connectors and then push the assembly in to tighten the two front captive fasteners.
- 4 Slide the PSA/PSB assembly rear tab into the slot on the bracket located at the top rear of the RPSM.
- 5 Push the connector assembly into the mating connectors on the top of the RPSM.
- 6 Tighten the PSA/PSB bracket captive fastener.
- 7 Connect the power supply bottom connectors.

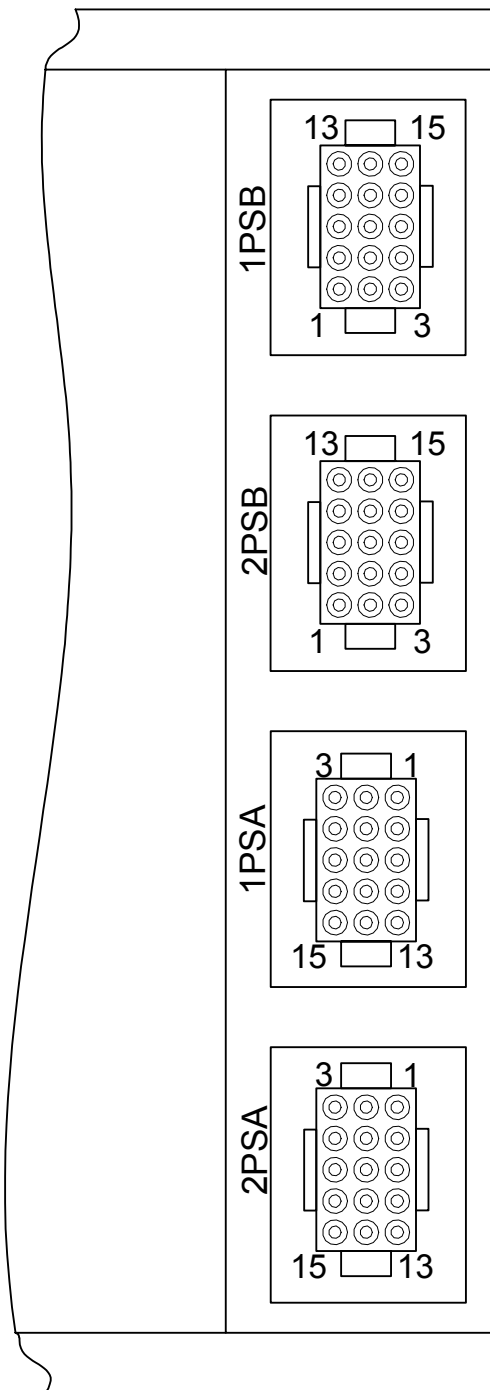
PIN32 5V
 PIN30 5V RET
 PIN28 5V
 PIN26 5V RET
 PIN24 5V
 PIN22 5V RET
 PIN20 5V
 PIN18 5V RET
 PIN16 +12V
 PIN14 RET
 PIN12 -12V
 PIN10 RET
 PIN8 +15V
 PIN6 RET
 PIN4 N/C
 PIN2 N/C



PIN32 -15V
 PIN30 RET
 PIN28 -28V
 PIN26 RET
 PIN24 28VA
 PIN22 RET
 PIN20 28VB
 PIN18 RET
 PIN16 28VC
 PIN14 RET
 PIN12 28VD
 PIN10 RET
 PIN8 28VE
 PIN6 RET
 PIN4 N/C
 PIN2 N/C



RPSM Top Connectors



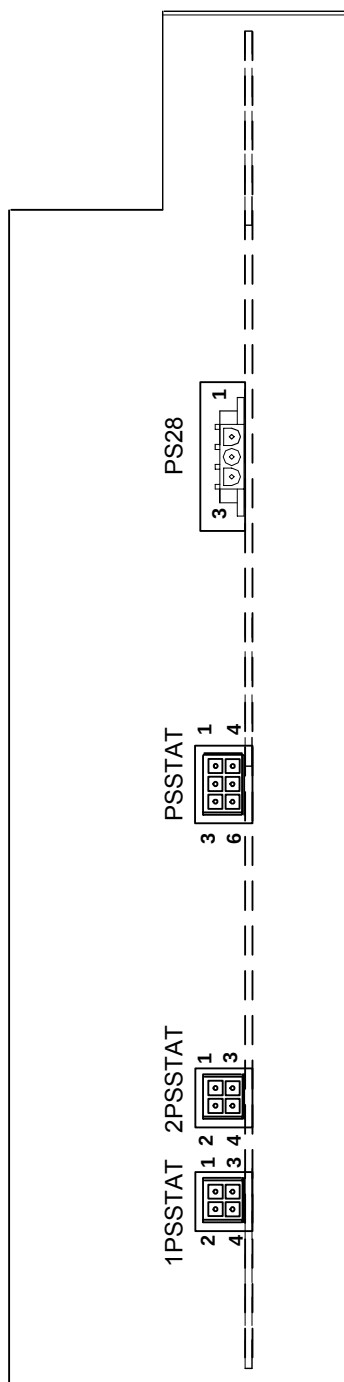
1 & 2PSB

Pin	
1	P5V1/2
2	P5V1/2
3	P5V1/2
4	P5RTN
5	P5RTN
6	P5RTN
7	NC
8	P5SENP
9	P5SENN
10	P15V1/2
11	N12
12	P12V1/2
13	P15RTN
14	N12RTN1/2
15	P12RTN

1 & 2PSA

Pin	
1	P28AB1/2
2	N28
3	N15
4	AB28RTN
5	N28RTN1/2
6	N15RTN1/2
7	NC
8	P28AB1/2
9	AB28RTN
10	P28E1/2
11	P28D1/2
12	P28C1/2
13	E28RTN
14	D28RTN
15	C28RTN

RPSM Back Side Connectors



RPSM Bottom Connectors

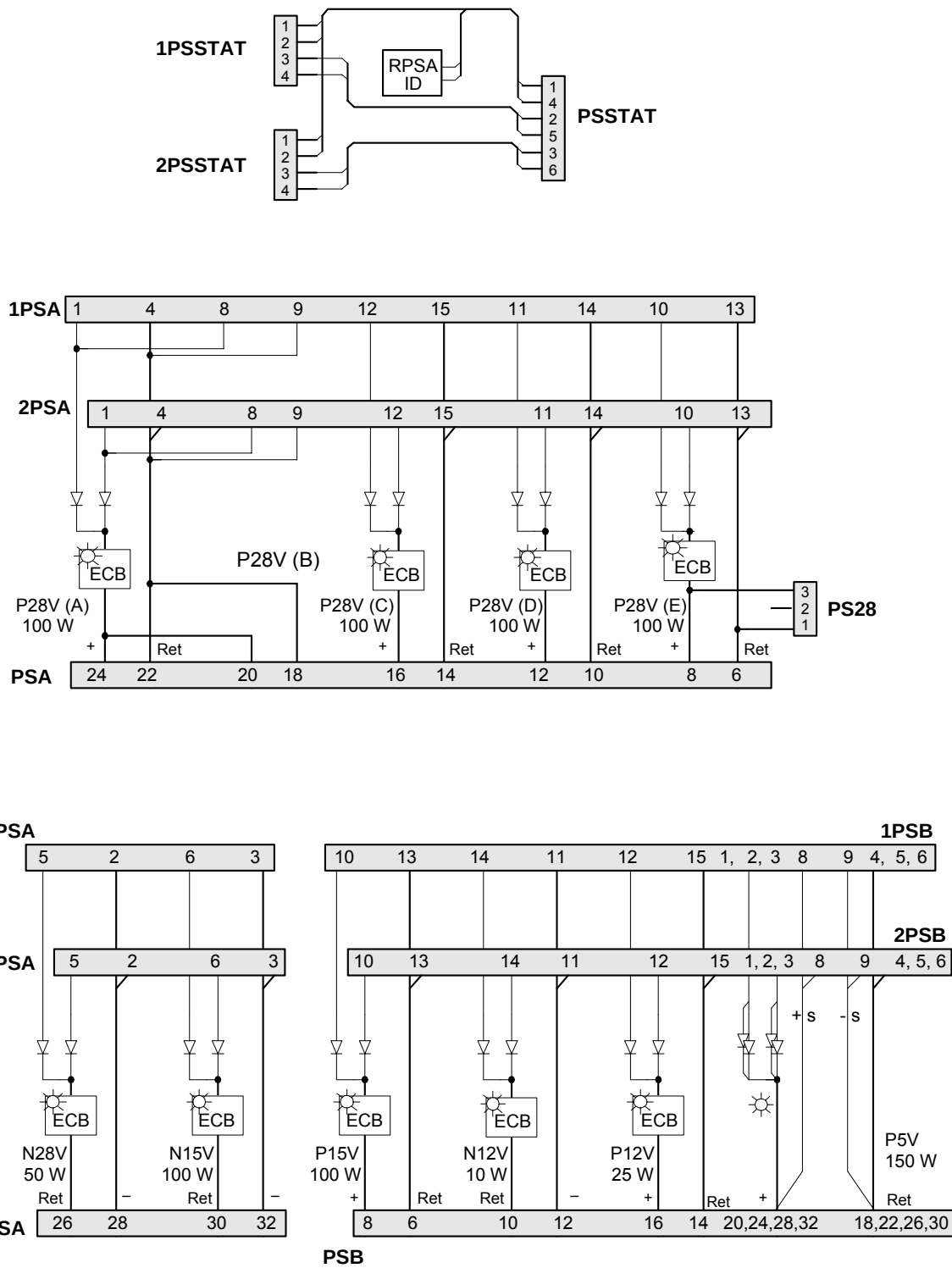
PS28	
Pin	
1	P28E
2	CHASS
3	E28RTN

PSSTAT	
Pin	
1	IDSIG
4	IDGND
2	1STAT1
5	1STAT2
3	2STAT1
6	2STAT2

2PSSTAT	
Pin	
1	IDSIG
2	IDGND
3	2STAT1
4	2STAT2

1PSSTAT	
Pin	
1	IDSIG
2	IDGND
3	1STAT1
4	1STAT2

Operation



RPSM Block Diagram

Output Voltage ORing

The ten outputs of two supplies are ORed together using low forward drop Schottky diodes. If an output of one of the supplies fails, the corresponding output on the other supply will pick up the full load through the diode. It is not intended that the two supplies equally share the load current, but if a short occurs on a RPSM output, it is possible to supply twice the normal short circuit current to the load. To prevent this, all of the outputs of the ORing diodes, with the exception of the 5 V, have an additional current limit circuit.

Note These circuits will hold the short circuit current to an acceptable level.

Refer to the *Specifications* section for expected RPSM output voltages accounting for the voltage losses introduced by passing the supply outputs through the ORing circuits. Due to the wiring impedance between the supply outputs and the RPSM, the supplies will tend to share the load. The sharing will reduce the diode and conductor losses so the expected losses for normal operations will be less than with one supply faulted.

Current Limit ECB

Nine of the outputs have electronic circuit breakers (ECBs) to limit the short circuit current. These circuit breakers are of the auto-reset type. Once the supplied output current exceeds the over-current threshold the output will be turned OFF and the reset timer started. Once the reset timer has expired the output will be turned back ON. If the over-current condition still exists, the output will be turned OFF and the reset timer started again. This cycle will continue until the short is removed. The output will then return to normal operation.

Note No current limiting is provided on the RPSM module for the 5 V output.

RPSM Electronic Circuit Breaker Limits

Parameter	Min.	Typical	Max.	Units
Reset Time		500		msec
±12 OC Threshold	2.78	3.3	3.89	Amps
±15 OC Threshold	8.30	10	11.70	Amps
±28 OC Threshold	4.15	5	5.85	Amps

Indicator LEDs

All the RPSM supply outputs have green status LEDs to indicate that power is being supplied to the load. The LEDs are located on the front panel of the module. For normal operations these LEDs will be ON solid. If the RPSM is not supplying the correct power to the load, one or more of these LEDs are OFF or flashing.

Note A flashing LED indicates that the output ECB is tripped

LED Definitions

LED	Description
P5	P5 output voltage indicator
P12	P12 output voltage indicator
N12	N12 output voltage indicator
P15	P15 output voltage indicator
N15	N15 output voltage indicator
N28	N28 output voltage indicator
P28AB	P28A/B output voltage indicator
P28C	P28C output voltage indicator
P28D	P28D output voltage indicator
P28E	P28E output voltage indicator

Specification

Item	Description
Output Voltage	Conditions Minimum Typical Maximum Units
+5 V	20 - 30 A 4.90 5.05 5.20 V dc
±12 V	0.1 - 1.6 A 11.64 12.0 12.72 V dc
±15 V	0.1 - 5.3 A 14.55 15.0 15.97 V dc
±28 V	0.2 - 3.2 A 26.6 28.0 29.4 V dc
Outputs	P28V (A), P28V (B), P28V (C), P28V (D), P28V (E), all with 100 W capability PS28 External 28 V output, from P28 (E) N28V 50 W N15V 100 W P15V 100 W N12V 10 W P12V 25 W P5V 150 W

Diagnostics

Below is a list of fault indications and the possible causes.

All RPSM green LEDs OFF - This is an indication of a problem back at the power supplies and not an RPSM failure.

One or more RPSM green LEDs OFF (but not all) - An RPSM LED OFF condition is an indication that there is no output voltage due to a short in the control rack or an RPSM failure.

5 V output problems - The 5 V output is unique from all of the other outputs. This RPSM output does not have current limit protection and has remote voltage sensing from the power supplies to the RPSM module. With a 5 V transient short or problem in the system, the most likely failure mode will be a 5 V output over-voltage fault back at the power supplies. Under high currents the losses will become high enough to cause the voltage at the power supplies to exceed the over-voltage threshold. Refer to the 5 V paragraph in GEI-100567 VME Power Supply for details. Any time the RPSM P5 green LED is on, the RPSM 5 V output voltage is above 4.55 V.

Redundant power supply replacement - As long as one of the power supplies is fully operational, the RPSM green LEDs will be ON and the correct power will be supplied to the system. When one of the power supplies fails, replacement can be postponed until it is convenient to do so. Before replacing the supply, refer to the troubleshooting guidelines outlined in GEI-100567 VME Power Supply to rule out a transient fault that can be reset such as an input power under-voltage. If the supply is found to be defective, follow removal and installation procedure outlined in the Power Supply section.

Parallel Status/ID

Each status connector from the power supplies has a status and ID signal. The ID signals from the two supplies are wired together along with the ID signal from the RPSM and passed out through the PSSTAT connector. The ID signal output is a single wire LAN line with three DALLAS 2502 ID ICs connected on it. The NO SSR contact status signals from the both supplies are passed through the RPSM and out the PSSTAT connector.

Power Supply 1 and 2 Status SSR NO Contacts

Parameter	Conditions	Min.	Max.	Units
V dc rating		55		V dc
V ac rating		55		V peak
Current rating		500		mA
ON resistance			1.0	Ohm
Isolation		1500		V dc

There are no field serviceable components in the RPSM module. If one or more of the green front panel LEDs are OFF, this is not a direct indication that the RPSM module has failed and has to be replaced. An LED OFF could indicate that something is wrong in the system and the fault is not due to the RPSM module.

Configuration

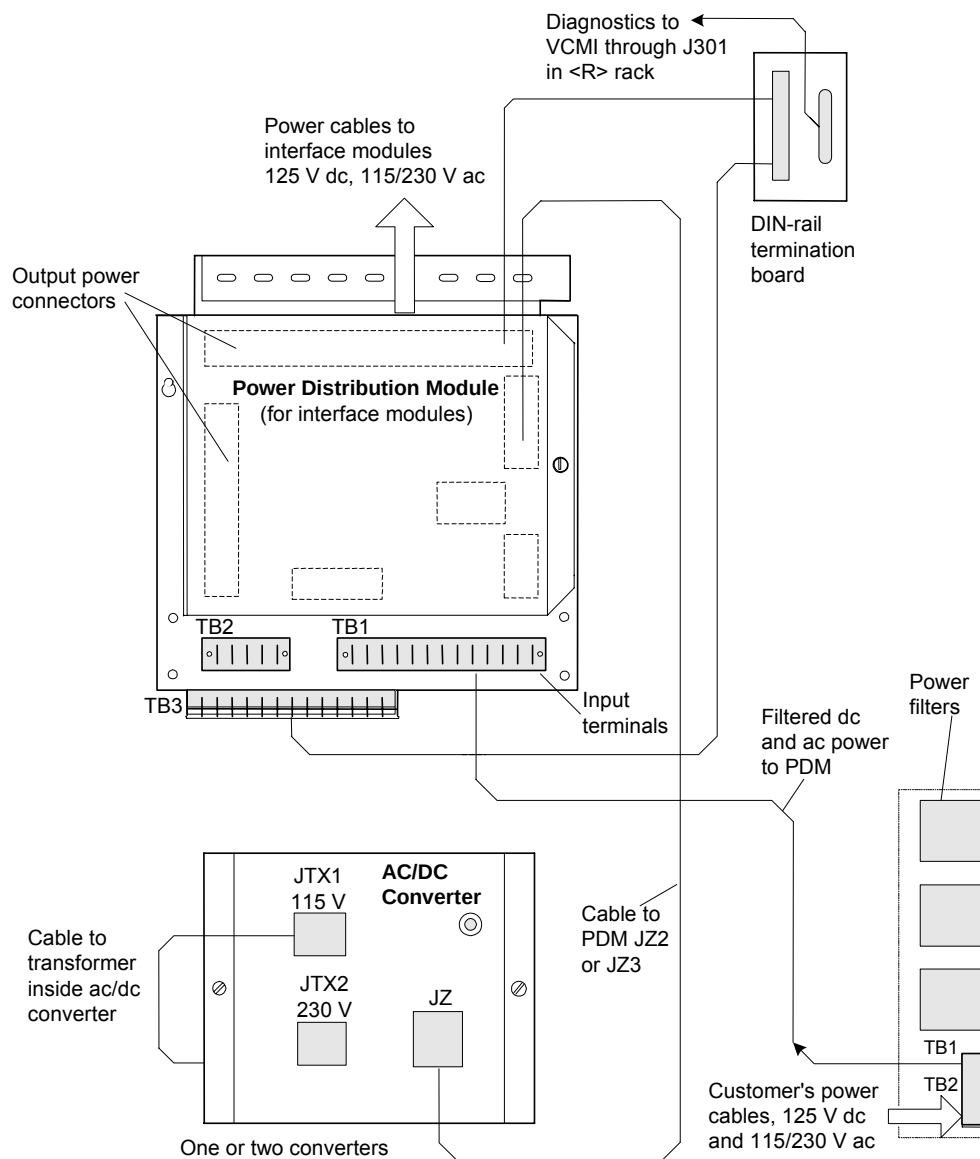
There are no jumpers or hardware settings on the board.

Power Distribution Modules

PDM Power Distribution Modules

Functional Description

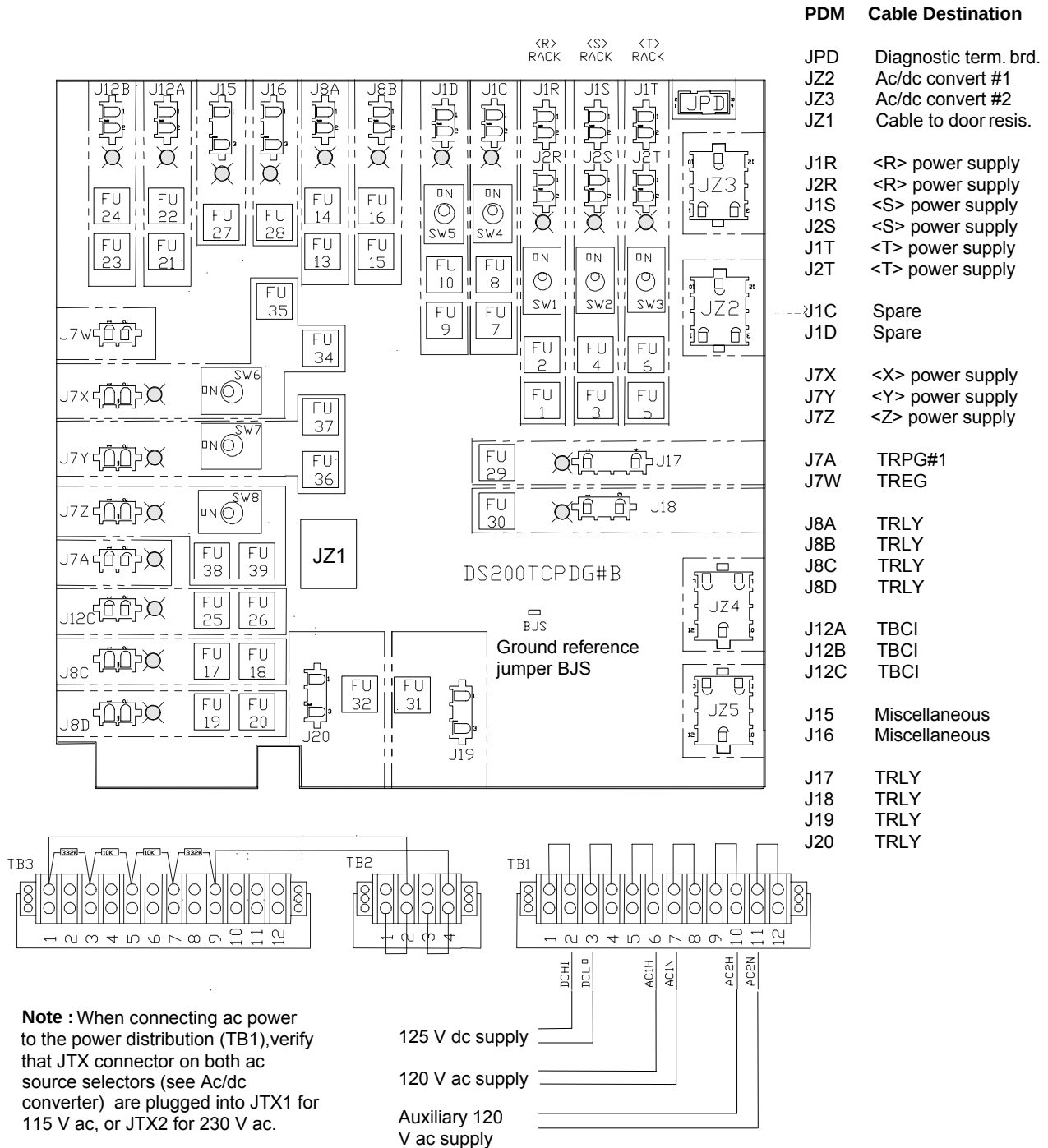
The Power Distribution Modules (PDM) provides 125 V dc and 115 V ac (or 230 V ac) to the Mark* VI system for all racks and terminal boards. There is a second version of the PDM for the control cabinet in those systems using remote I/O cabinets.



Power Distribution Module, Ac to Dc Converter, and Diagnostic Cabling

Installation

The cabling, wiring connections, and fuse locations for the PDM in the interface cabinet are shown in the figure.



Interface Cabinet PDM Circuit Board

Fuses in Interface and Control Cabinet PDM

Values of the fuses for the PDM interface cabinet are shown in the following table.

Interface Cabinet PDM Fuse Ratings

PDM Fuse* No.	J Connector	Current Rating	Voltage Rating	Vendor Catalog No.
FU1-FU6	J1R, S, T	15 A	125 V	Bussmann® GMA-15A
FU7-FU10	J1C, D	5 A	125 V	Bussmann GMA-5A
FU13-FU20	J8A, B, C, D	15 A	125 V	Bussmann GMA-15A
FU21-FU26**	J12A, B, C	1.5 A	125 V	Bussmann GMC-1.5A
FU27-FU28***	J15, 16	3.2 A	250 V	Bussmann MDL-3.2A
FU29	J17	15 A	250 V	Bussmann ABC-15A
FU30	J18	5 A	250 V	Bussmann ABC-5A
FU31-FU32	J19, 20	15 A	250 V	Bussmann ABC-15A
FU34-FU39	J7X, Y, Z	5 A	125 V	Bussmann GMA-5A

*All fuses are ferrule type 5 mm x 20 mm, except for FU27-FU32 which are 0.25" x 1.25".

**The short circuit rating for FU21-FU26 is 100 A

***The short circuit rating for FU27-FU28 is 70 A

The PDM in the control cabinet (IS2020CCPD) does not supply power to any terminal boards except the TRLY boards. Values for the fuses in the control cabinet PDM are similar to those in the I/O cabinet PDM, except the rating for fuses FU1-FU6 is 5 A instead of 15 A.

Operation

The customer's 125 V dc and 115/230 V ac power is brought into the PDM through power filters. The ac power is cabled out to one or two ac/dc converters which produce 125 V dc. This dc voltage is then cabled back into the PDM and diode coupled to the main dc power, forming a redundant power source. This power is distributed to the VME racks and terminal boards.

Either 115 V ac or 230 V ac can be handled by the ac/dc converters. The transformer cable must be plugged into either JTX1 for 115 V ac, or JTX2 for 230 V ac operation.

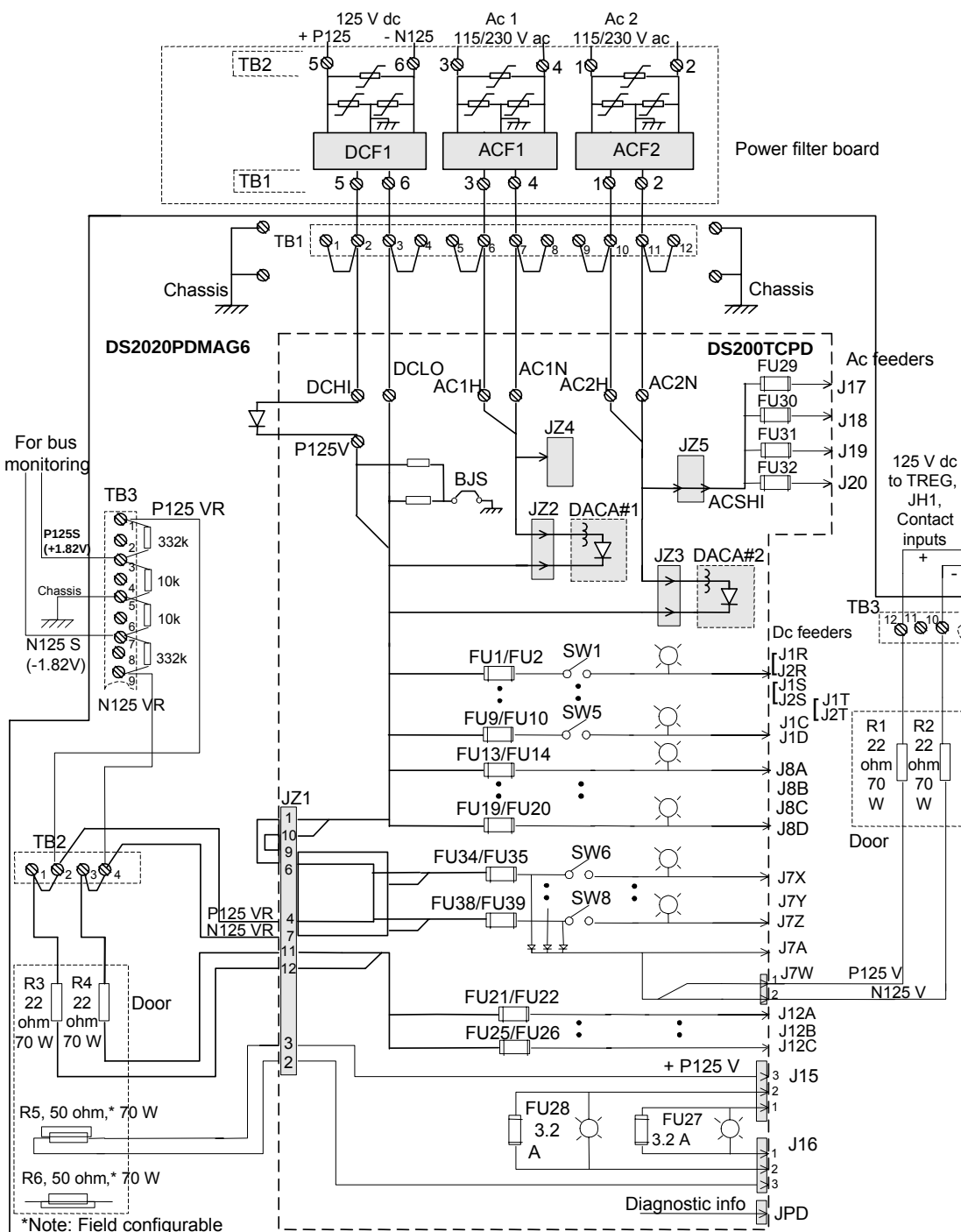
Diagnostic information is collected in the PDM and wired out to a DIN rail mounted terminal board. A cable then runs to the VCMI in rack <R> through J301.

Ac feeders, J17-20, are fused and cabled out to the relay terminal boards. 125 V dc feeders are fused and cabled to the interface (I/O) cabinets, protection modules, TRPG, TREG, and TRLY. To ensure a noise free supply to the boards, the PDM is supplied through a control power filter (CPF), which suppresses EMI noise. The CPF rack holds either two or three Corcom 30 A filter modules as shown in the following figure.

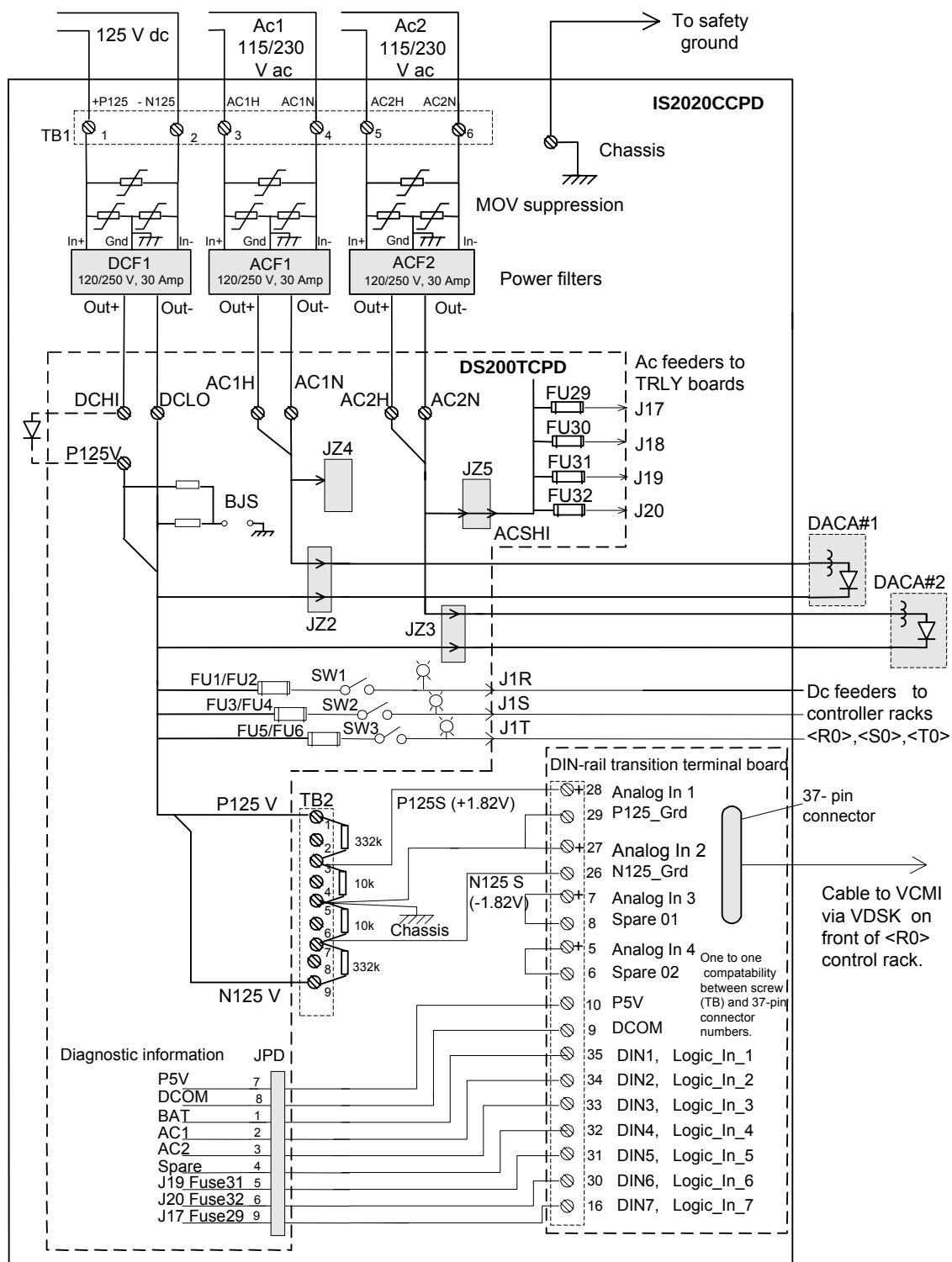
Power to the contact inputs first passes through resistors R3 and R4, through TB2, before being fused and cabled to the TBCI boards. Contact inputs operate with 125 V dc excitation.

Control Cabinet PDM

Power requirements for the control cabinet are less than for the interface cabinet. The PDM has the same layout but different fuse ratings, since only the control racks and relay output boards require power. For additional noise filtering for the controllers, Corcom power filters are included with the PDM.



Distribution Module for I/O Cabinet



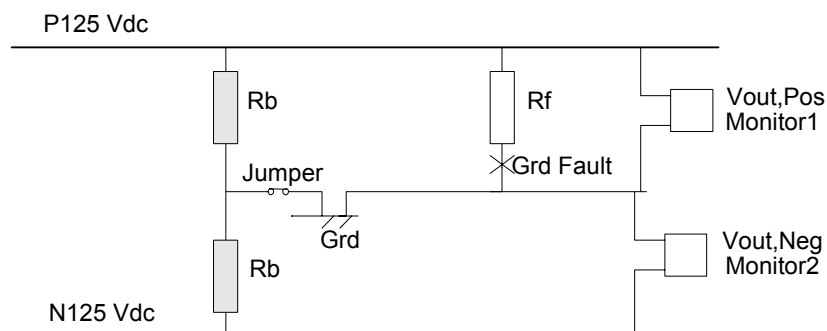
PDM for Controller Cabinet

Ground Fault Detection Sensitivity

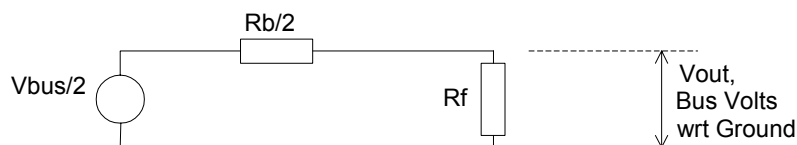
Note Ground fault detection is performed by the VCM I using signals from the PDM.

Ground fault detection on the floating 125 V dc power bus is based upon monitoring the voltage between the bus and the ground. The bus voltages with respect to ground are normally balanced (in magnitude), that is the positive bus to ground is equal to the negative bus to ground. The bus is forced to the balanced condition by the bridging resistors, Rb (refer to the figure). Bus leakage (or ground fault) from one side will cause the bus voltages with respect to ground to be unbalanced.

Power Distribution Module



Electrical Circuit Model



Ground Fault on Floating 125 Vdc Power Bus

There is a relationship between the bridge resistors, the fault resistance, the bus voltage, and the bus to ground voltage (Vout) as follows:

$$V_{out} = V_{bus} \cdot R_f / [2 \cdot (R_f + R_b/2)]$$

Therefore the threshold sensitivity to ground fault resistance is as follows:

$$R_f = V_{out} \cdot R_b / (V_{bus} - 2 \cdot V_{out}).$$

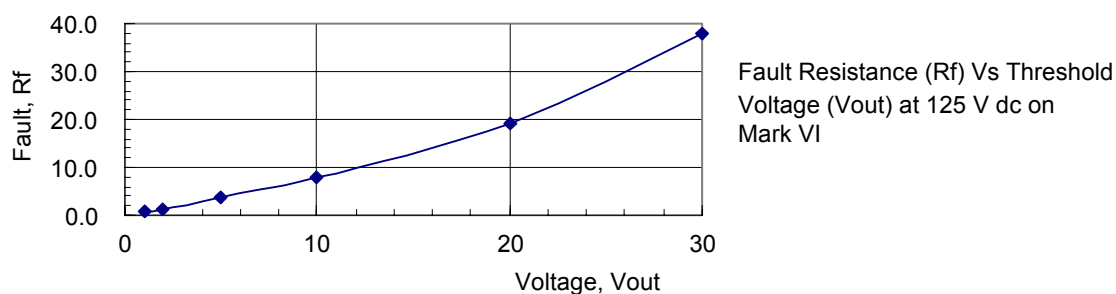
The ground fault threshold voltage is typically set at 30 V, that is $V_{out} = 30$ V. The bridging resistors are 82 K each. Therefore, from the formula above, the sensitivity of the control panel to ground faults, assuming it is on one side only, is as shown in the following table.

Note On Mark V systems, the bridging resistors are 33 K each so different Vout values result.

Sensitivity to Ground Faults

Vbus - Bus voltage	Vout - Measured Bus to ground voltage (threshold)	Rb (Kohms) - bridge resistors (balancing)	Rf (Kohms) -fault resistor	Control System
105	30	82	55	Mark VI
125	30	82	38	Mark VI
140	30	82	31	Mark VI
105	19	82	23	Mark VI
125	19	82	18	Mark VI
140	19	82	15	Mark VI
105	10	82	10	Mark VI
125	10	82	8	Mark VI
140	10	82	7	Mark VI
105	30	33	22	Mark V
125	30	33	15	Mark V
140	30	33	12	Mark V

The results for the case of 125 V dc bus voltage with various fault resistor values is shown in the following figure.



Threshold Voltage as Function of Fault Resistance

Results

On Mark VI, when the voltage threshold is configured to 30 V and the voltage bus is 125 V dc, the fault threshold is 38 Ω . When the voltage threshold is configured to 17 V and the voltage bus is 125 V dc, the fault threshold is 15 Ω .

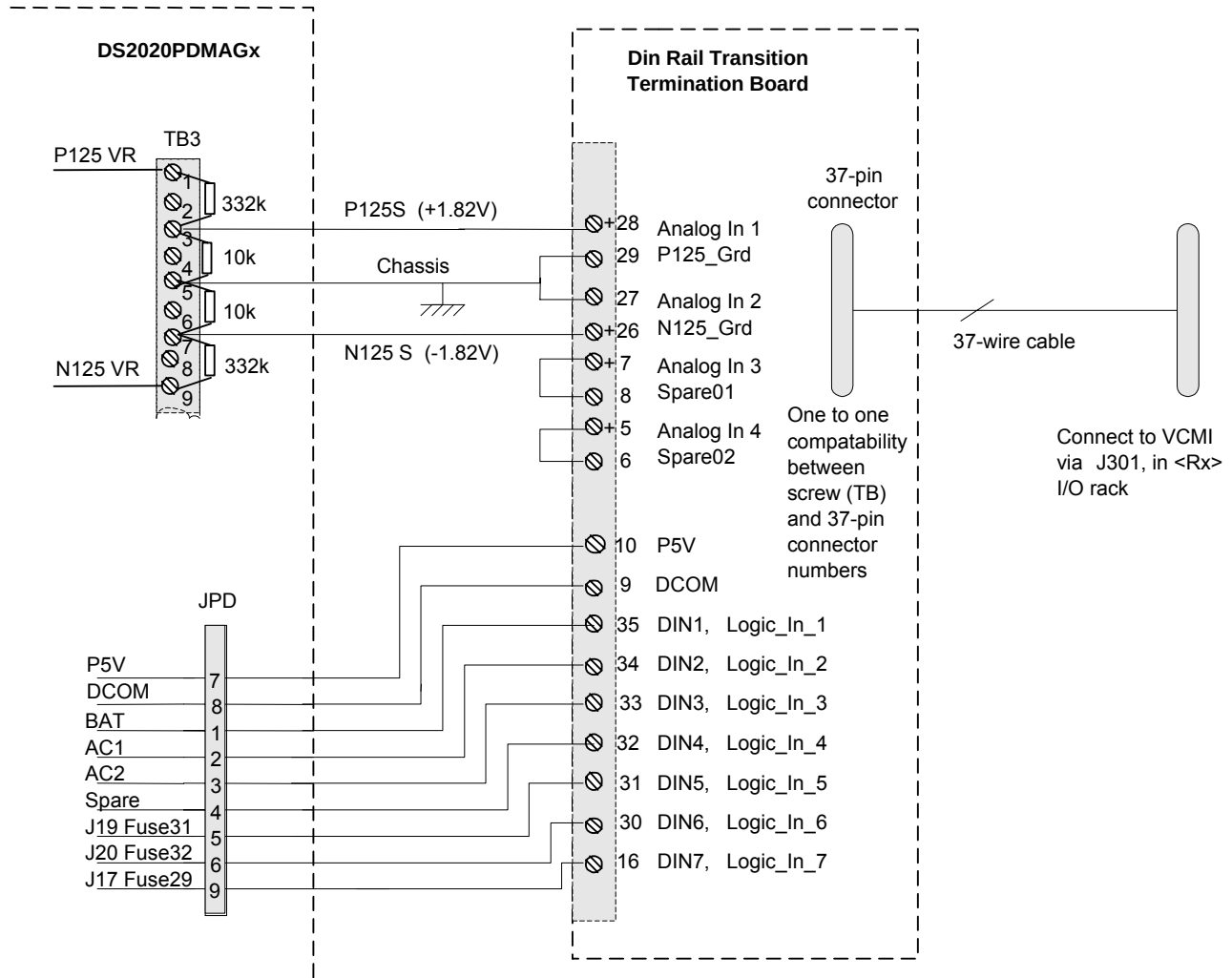
The sensitivity of the ground fault detection is configurable. Balanced bus leakage decreases the sensitivity of the detector.

Specifications

Item	Specification
Number of input sources	One 125 Volt battery One or two 115/230 V ac sources
Control Power filters	Dc: One Corcom 30 A filter modules - 120/250 V, 30 A Ac: One or two Corcom 30 A filter modules - 120/250 V, 30 A
AC to DC converters	One or two DACA converters – 115 or 230 V ac
Redundancy	The two or three dc sources are diode coupled to form a redundant power source for the I/O racks
Outputs	Two TMR I/O racks, six total Three VPRO protection modules One TRPG and one TREG board Four AC feeders to TRLY boards Four DC feeders to TRLY boards Three TBCI boards Two spare, two miscellaneous outputs

Diagnostics

As shown in the following figure, the 125 V dc is reduced by a resistance divider network to signal level for monitoring. Other items monitored include the battery voltage, two ac sources, and fuses in the feeders to the relay output boards. In the interface cabinet this diagnostic data is monitored by the VCM I. In the control cabinet it is cabled to the VDSK board and then to the VCM I.



PDM Diagnostic Monitoring

Configuration

Switches

The PDM for the I/O cabinets has a number of jumpers and switches as follows. Refer to the circuit diagrams for location and function.

Switch	Indicator	Output	Cable Destination
SW1	Yes	J1R, J2R	<R> Power Supply, 125 V dc
SW2	Yes	J1S, J2S	<S> Power Supply, 125 V dc
SW3	Yes	J1T, J2T	<T> Power Supply, 125 V dc
SW4	Yes	J1C	Spare 125 V dc supply
SW5	Yes	J1D	Spare 125 V dc supply
SW6	Yes	J7X	<X> (or R8) Power, 125 V dc supply
SW7	Yes	J7Y	<Y> (or S8) Power, 125 V dc supply
SW8	Yes	J7Z	<Z> (or T8) Power, 125 V dc supply

Jumpers

Jumpers are located on TB1, and TB2. Resistors are located on TB3 to reduce the 125 V dc to 1.82 V dc for monitoring the bus.

Ground Reference Jumper

Jumper BJS is supplied for isolation of ground reference on systems with an external ground reference. The ground reference bridge across the 125 V dc power has two resistances, one on each side, and BJS connects the center to ground.

Note When more than one PDM is supplied from a common 125 V dc source, remove all the BJS connections except one.

PDM variables including the ac and dc sources, P125 and N125 voltages, and the status of fuses 31, 32, and 33, are monitored by the VCMi in <R> rack. Refer to the VCMi toolbox configuration in *GEI-100551, VCMi Bus Master Controller*.

Alarms

Fault	Fault Description	Possible Cause
43	125 Volt Bus = [] Volts is Outside of Limits. The 125 Volt bus voltage is out of the specified operating limits.	A source voltage or cabling problem; disable 125 V monitoring if not applicable.
44	125 Volt Bus Ground = [] Volts is Outside of Limits. The 125 Volt bus voltage ground is out of the specified operating limits.	Leakage or a fault to ground causing an unbalance on the 125 V bus; disable 125 V monitoring if not applicable.

PPDA Power Distribution System Feedback

Functional Description

The Power Distribution System Feedback (PPDA) pack accepts inputs from up to six different power distribution boards. It conditions the board feedback signals and provides a dual redundant Ethernet interface to the controllers. PPDA feedback is structured to be plug and play uses electronic IDs to determine the power distribution boards wired into it. This information is then used to populate the IONet output providing correct feedback from connected boards.

Compatibility

The PPDA I/O pack is hosted by the JPDS or JPDM 28 V dc Control Power boards on the Mark* VIe Modular Power Distribution (PDM) system. It is compatible with the feedback signals created by JPDB, JPDE, and JPDE.

Installation

The PPDA I/O pack mounts on either a JPDS or JPDM 28 V dc control power terminal board.

➤ To install the PPDA pack

- 1 Securely mount the desired terminal board.
- 2 Directly plug one PPDA I/O pack for simplex or three PPDA I/O packs for TMR into the terminal board connectors.
- 3 Mechanically secure the packs using the threaded studs adjacent to the Ethernet ports. The studs slide into a mounting bracket specific to the terminal board type. The bracket location should be adjusted such that there is no right-angle force applied to the DC-62 pin connector between the pack and the terminal board. The adjustment should only be required once in the life of the product.
- 4 Plug in one or two Ethernet cables depending on the system configuration. The pack will operate over either port. If dual connections are used, the standard practice is to connect ENET1 to the network associated with the R controller.
- 5 Apply power to the pack by plugging in the connector on the side of the pack. It is not necessary to insert this connector with the power removed from the cable as the I/O pack has inherent soft-start capability that controls current inrush on power application.
- 6 Configure the I/O pack as necessary.
- 7 Connect ribbon cables from connector J2 on JPDS or JPDM to daisy chain other core boards feeding information to PPDA.

Note Additional PDM feedback signals may be brought into the PPDA I/O pack through the P2 connector on the host board. The P1 connector is never used on a board that hosts the PPDA I/O pack, PPDA must always be at the end of the feedback cable daisy chain.

Diagnostics

The PPDA performs the following self-diagnostic tests:

- A power-up self-test including checks of RAM, flash memory, Ethernet ports, and most of the processor board hardware
- Continuous monitoring of the internal power supplies for correct operation
- A check of the electronic ID information from the terminal board, acquisition card, and processor card confirming the hardware set matches, followed by a check confirming the application code loaded from flash memory is correct for the hardware set
- The analog input hardware includes precision reference voltages in each scan. Measured values are compared against expected values and are used to confirm health of the A/D converter circuits.
- Details of the individual diagnostics are available from the ToolboxST* application. The diagnostic signals are individually latched, and then reset with the RESET_DIA signal if they go healthy.

Configuration

Variable	Description	Direction	Type
L3DIAG_PPDA_R	I/O Diagnostic Indication	Input	BOOL
L3DIAG_PPDA_S	I/O Diagnostic Indication	Input	BOOL
L3DIAG_PPDA_T	I/O Diagnostic Indication	Input	BOOL
LINK_OK_PPDA_R	I/O Link Okay Indication	Input	BOOL
LINK_OK_PPDA_S	I/O Link Okay Indication	Input	BOOL
LINK_OK_PPDA_T	I/O Link Okay Indication	Input	BOOL
ATTN_PPDA_R	I/O Attention Indication	Input	BOOL
ATTN_PPDA_S	I/O Attention Indication	Input	BOOL
ATTN_PPDA_T	I/O Attention Indication	Input	BOOL
PS18V_PPDA_R	I/O 18 V Power Supply Indication	Input	BOOL
PS18V_PPDA_S	I/O 18 V Power Supply Indication	Input	BOOL
PS18V_PPDA_T	I/O 18 V Power Supply Indication	Input	BOOL
PS28V_PPDA_R	I/O 28 V Power Supply Indication	Input	BOOL
PS28V_PPDA_S	I/O 28 V Power Supply Indication	Input	BOOL
PS28V_PPDA_T	I/O 28 V Power Supply Indication	Input	BOOL
IOPackTmpr_R	I/O pack Temperature (deg F)	AnalogInput	REAL
IOPackTmpr_S	I/O pack Temperature (deg F)	AnalogInput	REAL
IOPackTmpr_T	I/O pack Temperature (deg F)	AnalogInput	REAL
Pbus_R_LED	Pbus R is in Regulation	Input	BOOL
Pbus_S_LED	Pbus S is in Regulation	Input	BOOL
Pbus_T_LED	Pbus T is in Regulation	Input	BOOL
Src_R_LED	All R Pbus Sources OK	Input	BOOL
Src_S_LED	All S Pbus Sources OK	Input	BOOL
Src_T_LED	All T Pbus Sources OK	Input	BOOL
Aux_LED	Aux 28 outputs OK	Input	BOOL
Batt_125V_LED	125 V battery volts OK	Input	BOOL
Batt_125G_LED	125 V battery floating	Input	BOOL
JPDD_125D_LED	125 V JPDD feeds OK	Input	BOOL
Pbus_125P_LED	125 V Pbus feeds OK	Input	BOOL

Variable	Description	Direction	Type
Batt_24V_LED	24 V battery volts OK	Input	BOOL
Batt_24G_LED	24 V battery floating	Input	BOOL
JPDD_24D_LED	24 V JPDD feeds OK	Input	BOOL
Pbus_24P_LED	24 V Pbus feeds OK	Input	BOOL
AC_Input1_LED	Ac input 1 OK	Input	BOOL
AC_Input2_LED	Ac input 2 OK	Input	BOOL
AC_JPDA_LED	Ac JPDA feeds OK	Input	BOOL
AC_Pbus_LED	Ac Pbus feeds OK	Input	BOOL
JPDR_LED	JPDR Src Select OK	Input	BOOL
Accelerometer_X	Vibration input, X-coordinate	AnalogInput	REAL
Accelerometer_Y	Vibration input, Y-coordinate	AnalogInput	REAL
App_1_LED	Application driven	Output	BOOL
App_2_LED	Application driven	Output	BOOL
App_3_LED	Application driven	Output	BOOL
Fault_LED	Fault Led - Application driven)	Output	BOOL

Parameter	Description	Selections
InFiltEnb1	Enable inputs filtering for terminal board #1	Disable, Enable
InFiltEnb2	Enable inputs filtering for terminal board #2	Disable, Enable
InFiltEnb3		Disable, Enable
InFiltEnb4		Disable, Enable
InFiltEnb5		Disable, Enable
InFiltEnb6		Disable, Enable

DS2020DACAG2 ac-dc Power Conversion

Functional Description

The DS2020DACAG2 is a drop in replacement for the DS2020DACAG1. It is backward compatible in systems that used the previous version and it should be used as a replacement part for the previous model. The DACA converts 115/230 V ac input power into 125 V dc output power, and the output power rating is approximately 1000 W.

A DACA is used when the primary power source for a control system is 125 V dc with or without a battery. In addition to power conversion, DACA provides additional local energy storage to extend the ride-through time whenever the Mark VIe Control has a complete loss of control power.

The DS2020DACAG2 model has a higher power rating than the previous module. Also, this new model can be paralleled for greater output current, whereas paralleling was not recommended for the previous model. The DS2020DACAG2 is recommended for all new panel designs.

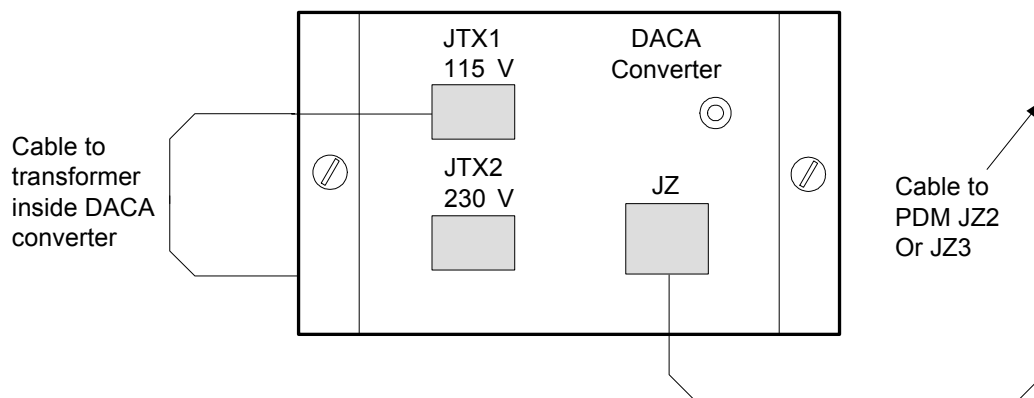
Installation

The DACA module has four mounting holes in its base. Ac power input and dc output is through a single 12-position connector JZ that is wired into connector JZ2 or JZ3 of the PDM. Selection of 115 V ac or 230 V ac input is made by plugging the DACA internal cable into connector JTX1 for 115 V or JTX2 for 230 V.



Ensure the proper voltage is selected before power is applied to the equipment.

Caution



DACA Module Wiring

DACA Filter Capacitor Wear Out

The electrolytic capacitors in the DACA module wear out over time due to the ambient temperature of the environment where they are used. The following table shows the calculated life expectancy and recommended replacement schedule for the DACA modules.

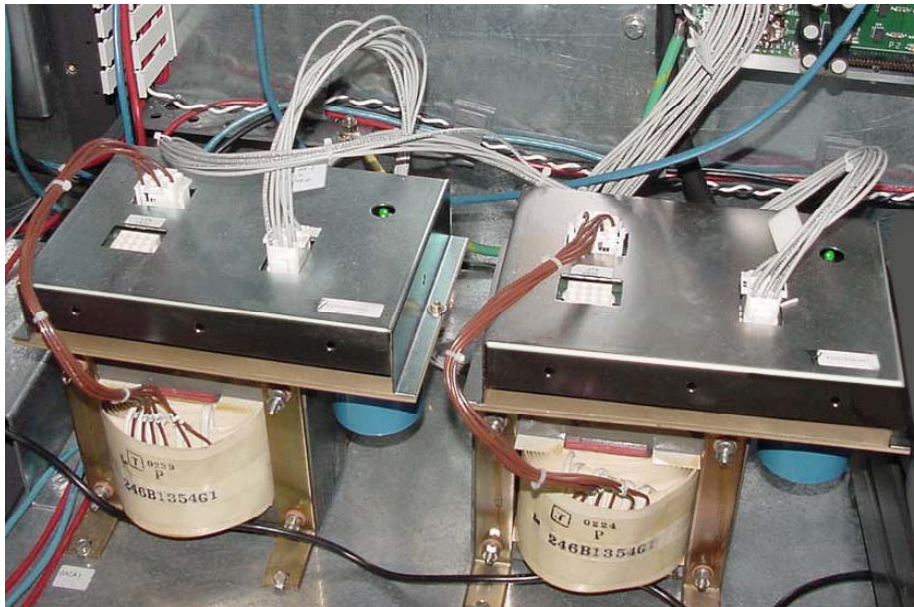
DACA Replacement Schedule

Calculated Life Expectancy of DACA Capacitor	Recommended Replacement Schedule*
At 20°C (68 °F) ambient	100 years
At 45°C (113 °F) ambient	20 years
At 65°C (149 °F) ambient	5 years

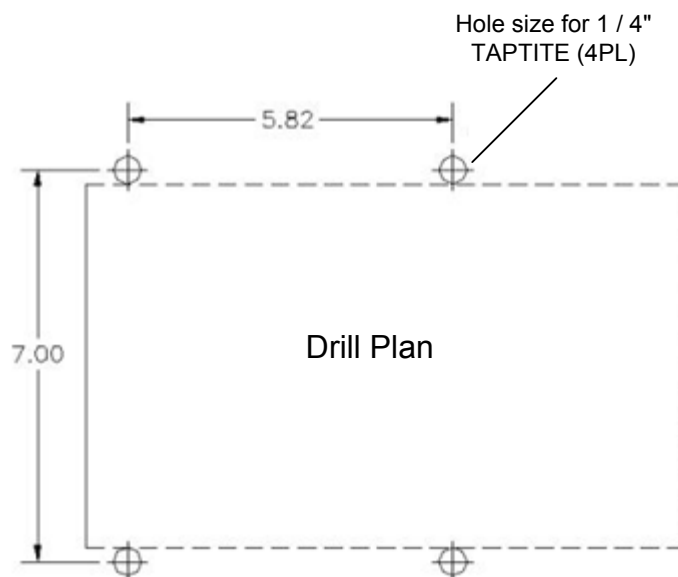
*Due to wear out of Electrolytic Capacitor

➤ To replace a DACA power conversion module

- 1** Remove power from the DACA module. Allow 1 minute for the output voltage to discharge.
- 2** Remove the power input/output cable (JZ) on the right side of the module top.
- 3** Remove the four bolts securing the DACA module to the floor of the cabinet.
- 4** Remove the DACA module.
- 5** Make note of which receptacle the capacitor power plug is in. This is on the left side of the module top. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
- 6** Ensure the capacitor power plug is in the same position as the one removed. JTX1 is for 115 V ac and JTX2 is for 230 V ac.
- 7** Place the new DACA module in the same position as the one removed.
- 8** Secure the DACA module to the cabinet floor with the four bolts removed from the previous module.
- 9** Install the power input/output plug (JZ) on the right side of the module top.
- 10** Restore power to the DACA module.



DACA Power Conversion Modules



Note: Keep out area is 8.65 in. x 13.9 in.

DACA Mounting Pattern

Operation

DACA receives ac power through the cable harness that is plugged into connector JZ. DACA uses a full wave bridge rectifier and an output filter capacitor. If needed, the user must provide an input filter to attenuate harmonic currents injected into the incoming line.

Single DACA Module, Maximum Output Current is 9.5 A dc

Input to DACA V ac RMS	Input Current at Max Load	Output Voltage Load = 1 A dc	Output Voltage Load = 9.5 A dc
115 V ac	11 A	119 V dc	107 V dc
230 V ac	6 A		

The DACAG2 can be paralleled for greater output current. In parallel operation, current sharing between the two DACAs is critical. Uneven current sharing can cause one of the DACAs to operate beyond its output current rating.

*Two DACA Modules with Outputs Paralleled, Maximum Output Current is 16.5 A dc**

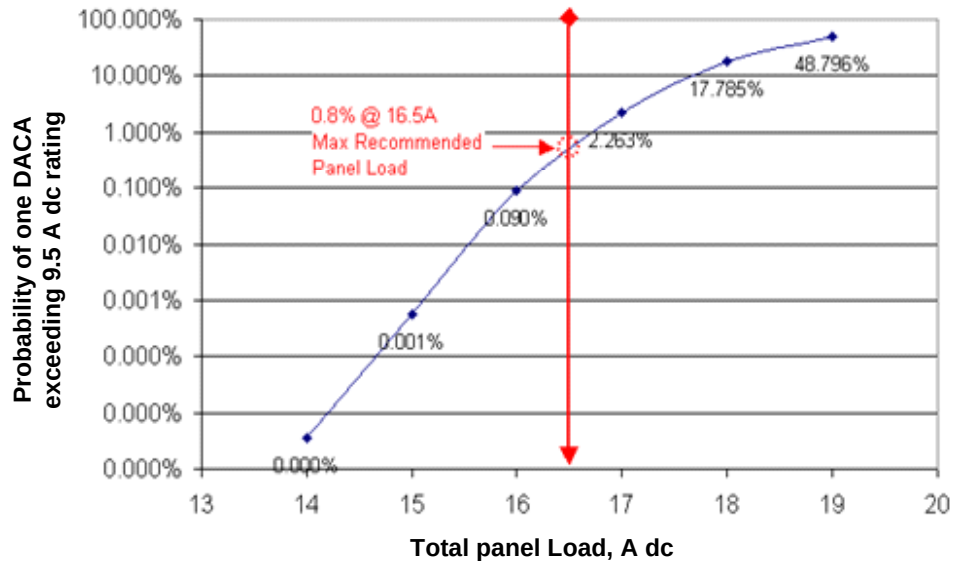
Input to DACA V ac RMS	Input Current at Max Load	Output Voltage Load = 1 A dc	Output Voltage Load = 15 A dc
115 V ac	20 A	120 V dc	110 V dc
230 V ac	11 A		

* The two paralleled DACAs must be connected to one ac voltage source for even output current sharing.

For proper implementation of parallel DACAs, the following must be observed:

- The DACAs must be connected to the same ac source to ensure equal input voltages to the DACAs.
- The maximum output current per DACA is derated for parallel operation. This derating accounts for variance in DACA open circuit voltages and variance in DACA output impedances. The following curve should be used. The maximum recommended total panel current is 16.5 A dc.

**Probability of overloading one DACA when two
DACAs are paralled; Plotted at various panel loads**



Specifications

Item	Specification			
Input Voltage	105-132 V ac or 210-265 V ac, 47 to 63 Hz			
Output Voltage	90 to 145 V dc with a load of 1 to 9.5 A Over the full range of input voltage			
Output Current Rating	9.5 A dc, -30 to 45°C (-22 to 113 °F) Linearly derate to 7.5 A dc at 60°C (140 °F)			
Output Ripple Voltage	4 V p-p			
Discharge Rate	Nominal input of 115 or 230 V ac, no load, discharge to less than 50 V dc within 1 minute of removal of input power.			
Hold Up (time for output to discharge to 70 V dc with constant power load)	V in (V ac)	105	115	132
	Initial Load (A dc)	9.5	9.5	9.5
	Pout (W)	882	974	1131
	Hold Up Time (ms)	19.5	29.5	48.8
Temperature	-30 to 60°C (-22 to +140 °F) free convection			
Humidity	5 to 95%, non-condensing			
	UL 508C Safety Standard Industrial Control Equipment			
	CSA 22.2 No. 14 Industrial Control Equipment			
	EN 61010 Section 14.7.2 – Overload Tests			
	EN 61010 Section 14.7.1 – Short Circuit Test			
	EN 61000-4-2 Electrostatic Discharge Susceptibility			
	EN 61000-4-3 Radiated RF Immunity			
	EN 61000-4-4 Electrical Fast Transient Susceptibility			
	EN 61000 –4-5 Surge Immunity			
	EN61000-4-6 Conducted RF Immunity			
	EN 50082-2:1994 Generic Immunity Industrial Environment			
	ENV 55011:1991 - ISM equipment emissions			
	IEC 529 Intrusion Protection Codes/NEMA 1/IP 20			

Diagnostics

No diagnostic features are provided on this module.

Configuration

Input voltage selection is made on DACA by plugging the captive cable harness into connector JTX1 for 115 V ac nominal input or connector JTX2 for 230 V ac nominal input.

Notes

Replacement/Warranty

Pack/Board Replacement

Handling Precautions



Caution

To prevent component damage caused by static electricity, treat all boards with static sensitive handling techniques. Wear a wrist grounding strap when handling boards or components, but only after boards or components have been removed from potentially energized equipment and are at a normally grounded workstation.



Warning

This equipment contains a potential hazard of electric shock, burn, or death. Ensure that all Lockout/Tag Out procedures are followed prior to replacing terminal boards. Only personnel who are adequately trained and thoroughly familiar with the equipment and the instructions should install, operate, or maintain this equipment.

Printed wiring boards may contain static-sensitive components. Therefore, GE ships all replacement boards in anti-static bags.

Use the following guidelines when handling boards:

- Store boards in anti-static bags or boxes.
- Use a grounding strap when handling boards or board components (per previous Caution criteria).

Replacement Procedures

System troubleshooting should be at the circuit board level. The failed pack/board should be removed and replaced with a spare.

Note The failed pack/board should be returned to GE for repair. Do not attempt to repair it on site.



Warning

To prevent electric shock, turn off power to the turbine control, then test to verify that no power exists in the board before touching it or any connected circuits.



Caution

To prevent equipment damage, do not remove, insert, or adjust board connections while power is applied to the equipment.

Replacing V-type Boards

➤ To replace the board

- 1** Power down the rack and remove the failed board.
- 2** Replace the board with a spare board of the same type, and move the Ethernet ID plug from the old VPRO board to the replacement.
- 3** Power up the rack.
- 4** From the toolbox Outline View, under item Mark VI I/O, locate the failed protection rack. From the shortcut menu, click Download. The board firmware and configuration downloads.
- 5** Cycle power to the rack to establish communication with the controller.

Replacing T-type Boards

➤ To replace the board

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Check the voltage on each terminal and ensure no voltage is present.
- 3** Unplug the I/O cable (J-Plugs).
- 4** If applicable, unplug JF1, JF2 and JG1.
- 5** If applicable, remove TB3 power cables.
- 6** Loosen the two screws on the wiring terminal blocks and remove the blocks, leaving the field wiring attached.
- 7** Remove the terminal board and replace it with a spare board, check that all jumpers are set correctly (the same as in the old board).
- 8** Screw the terminal blocks back in place and plug in the J-plugs and connect cable to TB3 as before

Replacing D-type Boards

➤ To replace the board

- 1** Lockout and/or tag out the field equipment and isolate the power source.
- 2** Unplug the I/O cable (J-plugs).
- 3** Disconnect all field wire and thermocouples along with shield wire.
- 4** Remove the terminal board and install the new board.
- 5** Reconnect all field wire and thermocouples as before.
- 6** Plug the I/O cable (J-plug) back.

Replacing J-type Boards

➤ To replace the board

- 1** Lockout and/or tag out the field equipment and isolate the power source.
- 2** Check the voltage on each terminal to ensure no voltage is present.
- 3** Verify the label and unplug all connectors.
- 4** Loosen the two screws on each of the terminal blocks and remove the top portion leaving all field wiring in place. If necessary, tie the block to the side out of the way.
- 5** Remove the mounting screws and the terminal board.
- 6** Install a new terminal board. Check that all jumpers, if applicable, are in the same position as the ones on the old board.
- 7** Tighten it securely to the cabinet.
- 8** Replace the top portion of the terminal blocks and secure it with the screws on each end. Ensure all field wiring is secure.
- 9** Plug in all wiring connectors.

Replacing S-type Boards

➤ To replace the board

- 1** Lockout and/or tagout the field equipment and isolate the power source.
- 2** Check the voltage on each terminal to ensure there is no voltage present.
- 3** Unplug the I/O cable (J-plugs)
- 4** If applicable, unplug JF1, JF2, and JG1.
- 5** If applicable, remove the TB3 power cables.
- 6** A S-type terminal board uses a Euro-style box terminal block. Gently pry the segment of the terminal block, containing the field wiring, away from the part attached to the terminal board, leaving the wiring in place. If necessary, tie the block to the side out of the way.
- 7** Remove the mounting screws and terminal board.
- 8** Install a new terminal board. Check to ensure all jumpers, if applicable, are in the same position as the ones on the old board.
- 9** Tighten it securely to the cabinet.
- 10** Slide the segments containing field wiring into the terminal block. Ensure the numbers on the segment with the field wires match the numbers on the terminal block. Press together firmly. Ensure all field wiring is secure.

Renewal/Warranty

How to Order a Board

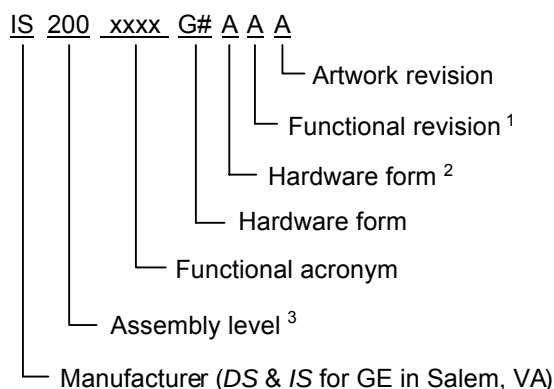
When ordering a replacement board for a GE product, you need to know:

- How to accurately identify the part
- If the part is under warranty
- How to place the order

Board Identification

A printed wiring board is identified by an alphanumeric **part (catalog) number** located near its edge. The following figure explains the structure of the part number.

The board's functional acronym, shown below, is normally based on the **board description**, or name.



¹Backward compatible

²Not backward compatible

³200 = a base-level board

215 = a higher level assembly or added components

220 = pack specific assembly

230 = a higher level module

Board Part Number Conventions

Placing the Order

Renewals/spares (or those not under warranty) should be ordered by contacting the nearest GE Sales or Service Office, or an authorized GE Sales Representative. Be sure to include:

- Complete part number and description
- Serial number
- Material List (ML) number

Note All digits are important when ordering or replacing any board. The factory may substitute later versions of replacement boards based on availability and design enhancements. However, GE Energy ensures backward compatibility of replacement boards.

Glossary of Terms

Glossary of Terms

application code

Software that controls the machines or processes, specific to the application.

ARCNET

Attached Resource Computer Network. A LAN communications protocol developed by Datapoint Corporation. The physical (coax and chip) and datalink (token ring and board interface) layer of a 2.5 MHz communication network which serves as the basis for DLAN+. See DLAN+.

attributes

Information, such as location, visibility, and type of data that sets something apart from others. In signals, an attribute can be a field within a record.

Balance of Plant (BOP)

Plant equipment other than the turbine that needs to be controlled.

baud

A unit of data transmission. Baud rate is the number of bits per second transmitted.

Bently Nevada

A manufacturer of shaft vibration monitoring equipment.

BIOS

Basic input/output system. Performs the controller boot-up, which includes hardware self-tests and the file system loader. The BIOS is stored in EEPROM and is not loaded from the toolbox.

bit

Binary Digit. The smallest unit of memory used to store only one piece of information with two states, such as One/Zero or On/Off. Data requiring more than two states, such as numerical values 000 to 999, requires multiple bits (see Word).

block

Instruction blocks contain basic control functions, which are connected together during configuration to form the required machine or process control. Blocks can perform math computations, sequencing, or continuous control. The ToolboxST application receives a description of the blocks from the block libraries.

board

Printed wiring board.

Boolean

Digital statement that expresses a condition that is either True or False. In the toolbox, it is a data type for logical signals.

Bus

An electrical path for transmitting and receiving data.

byte

A group of binary digits (bits); a measure of data flow when bytes per second.

CIMPLICITY

Operator interface software configurable for a wide variety of control applications.

COI

Computer Operator Interface that consists of a set of product and application specific operator displays running on a small panel computer hosting Embedded Windows NT.

COM port

Serial controller communication ports (two). COM1 is reserved for diagnostic information and the Serial Loader. COM2 is used for I/O communication

configure

To select specific options, either by setting the location of hardware jumpers or loading software parameters into memory.

CRC

Cyclic Redundancy Check, used to detect errors in Ethernet and other transmissions.

CT

Current Transformer, used to measure current in an ac power cable.

data server

A PC which gathers control data from input networks and makes the data available to PCs on output networks.

DCS (Distributed Control System)

Control system, usually applied to control of boilers and other process equipment.

DDPT

IS200DDPT Dynamic Pressure Transducer Terminal Board that is used in conjunction with the IS200VAMA VME Acoustic Monitoring Board that is used to monitor acoustic or pressure waves in the turbine combustion chamber.

dead band

A range of values in which the incoming signal can be altered without changing the output response.

device

A configurable component of a process control system.

DIN-rail

European standard mounting rail for electronic modules.

DLAN+

GE Energy LAN protocol, using an ARCNET controller chip with modified ARCNET drivers. A communications link between exciters, drives, and controllers, featuring a maximum of 255 drops with transmissions at 2.5 MBPS.

DRAM

Dynamic Random Access Memory, used in microprocessor-based equipment.

EGD

Ethernet Global Data is a control network and protocol for the controller. Devices share data through EGD exchanges (pages).

EMI

Electro-magnetic interference; this can affect an electronic control system

Ethernet

LAN with a 10/100 M baud collision avoidance/collision detection system used to link one or more computers together. Basis for TCP/IP and I/O services layers that conform to the IEEE 802.3 standard, developed by Xerox, Digital, and Intel.

EVA

Early valve actuation, to protect against loss of synchronization.

event

A property of Status_S signals that causes a task to execute when the value of the signal changes.

EX2000 (Exciter)

GE generator exciter control; regulates the generator field current to control the generator output voltage.

EX2100 (Exciter)

Latest version of GE generator exciter control; regulates the generator field current to control the generator output voltage.

fanned input

An input to the terminal board which is connected to all three TMR I/O boards.

fault code

A message from the controller to the HMI indicating a controller warning or failure.

firmware

The set of executable software that is stored in memory chips that hold their content without electrical power, such as EEPROM.

flash

A non-volatile programmable memory device.

forcing

Setting a live signal to a particular value, regardless of the value blockware or I/O is writing to that signal.

frame rate

Basic scheduling period of the controller encompassing one complete input-compute-output cycle for the controller. It is the system dependent scan rate.

function

The highest level of the blockware hierarchy, and the entity that corresponds to a single .tre file.

gateway

A device that connects two dissimilar LAN or connects a LAN to a wide-area network (WAN), pc, or a mainframe. A gateway can perform protocol and bandwidth conversion.

Graphic Window

A subsystem of the ToolboxST application for viewing and setting the value of live signals.

health

A term that defines whether a signal is functioning as expected.

heartbeat

A signal emitted at regular intervals by software to demonstrate that it is still active.

hexadecimal (hex)

Base 16 numbering system using the digits 0-9 and letters A-F to represent the decimal numbers 0-15. Two hex digits represent 1 byte.

HMI

Human Machine Interface, usually a PC running CIMPLICITY software.

HRSG

Heat Recovery Steam Generator using exhaust from a gas turbine.

ICS

Integrated Control System. ICS combines various power plant controls into a single system.

IEEE

Institute of Electrical and Electronic Engineers. A United States-based society that develops standards.

initialize

To set values (addresses, counters, registers, and such) to a beginning value prior to the rest of processing.

I/O Device

Input/output hardware device that allow the flow of data into and out

I/O

Input/output interfaces that allow the flow of data into and out of a device

I/O drivers

Interface the controller with input/output devices, such as sensors, solenoid valves, and drives, using a choice of communication networks.

I/O mapping

Method for moving I/O points from one network type to another without needing an interposing application task.

IONet

The Mark VI I/O Ethernet communication network (controlled by the VCMIs)

insert

Adding an item either below or next to another item in a configuration, as it is viewed in the hierarchy of the Outline View of the ToolboxST application.

instance

Update an item with a new definition.

item

A line of the hierarchy of the Outline view of the ToolboxST application, which can be inserted, configured, and edited (such as Function or System Data)

IP Address

The address assigned to a device on an Ethernet communication network.

LCI Static Starter

This runs the generator as a motor to bring a gas turbine up to starting speed.

logical

A statement of a true sense, such as a Boolean

macro

A group of instruction blocks (and other macros) used to perform part of an application program. Macros can be saved and reused.

Mark VIe Turbine controller

A controller hosted in one or more VME racks that perform turbine-specific speed control, logic, and sequencing.

median

The middle value of three values; the median selector picks the value most likely to be closest to correct.

Modbus

A serial communication protocol developed by Modicon for use between PLCs and other computers.

module

A collection of tasks that have a defined scheduling period in the controller.

MTBFO

Mean Time Between Forced Outage, a measure of overall system reliability.

NEMA

National Electrical Manufacturers Association; a U.S. standards organization.

non-volatile

The memory specially designed to store information even when the power is off.

online

Online mode provides full CPU communications, allowing data to be both read and written. It is the state of the ToolboxST application when it is communicating with the system for which it holds the configuration. Also, a download mode where the device is not stopped and then restarted.

pcode

A binary set of records created by the ToolboxST application, which contain the controller application configuration code for a device. Pcode is stored in RAM and flash memory.

period

The time between execution scans for a module or task - also a property of a module that is the base period of all of the tasks in the module

pin

Block, macro, or module parameter that creates a signal used to make interconnections.

Plant Data Highway (PDH)

Ethernet communication network between the HMI Servers and the HMI Viewers and workstations

PLC

Programmable Logic Controller. Designed for discrete (logic) control of machinery. It also computes math (analog) function and performs regulatory control.

PLU

Power load unbalance, detects a load rejection condition which can cause overspeed.

Power Distribution Module (PDM)

The PDM distributes 125 V dc and 115 V ac to the VME racks and I/O terminal boards.

PROFIBUS

An open fieldbus communication standard defined in international standard EN 50 170 and is supported in simplex Mark VIe systems.

Proximator

Bently Nevada's proximity probes used for sensing shaft vibration.

PT

Potential Transformer, used for measuring voltage in a power cable.

QNX

A real time operating system used in the controller.

real time

Immediate response, referring to process control and embedded control systems that must respond instantly to changing conditions.

reboot

To restart the controller or the ToolboxST application.

RFI

Radio Frequency Interference is high frequency electromagnetic energy which can affect the system.

register page

A form of shared memory that is updated over a network - register pages can be created and instanced in the controller and posted to the SDB

resources

Also known as groups. Resources are systems (devices, machines, or work stations where work is performed) or areas where several tasks are carried out. Resource configuration plays an important role in the CIMPLICITY system by routing alarms to specific users and filtering the data users receive.

RPSM

IS2020RPSM Redundant Power Supply Module for VME racks that mounts on the side of the control rack instead of the power supply. The two power supplies that feed the RPSM are mounted remotely.

RTD

Resistance Temperature Device used for measuring temperature.

runtime

See product code.

runtime errors

Controller problems indicated on the front panel by coded flashing LEDS, and also in the Log View of the ToolboxST application.

sampling rate

The rate at which process signal samples are obtained, measured in samples/second.

Serial Loader

Connects the controller to the toolbox PC using the RS-232C COM ports. The Serial Loader initializes the controller flash file system and sets its TCP/IP address to allow it to communicate with the ToolboxST application over Ethernet.

Server

A pc which gathers data over Ethernet from plant devices, and makes the data available to PC-based operator interfaces known as viewers.

SIFT

Software Implemented Fault Tolerance, a technique for voting the three incoming I/O data sets to find and inhibit errors. Note that Mark VIe also uses output hardware voting.

signal

The basic unit for variable information in the controller.

Simplex

Operation that requires only one set of control and I/O, and generally uses only one channel. The entire Mark VIe control system can operate in simplex mode, or individual VME boards in an otherwise TMR system can operate in implex mode.

stall detection

Detection of stall condition in a gas turbine compressor.

SOE

Sequence of Events, a high-speed record of contact closures taken during a plant upset to allow detailed analysis of the event.

Static Starter

See LCI.

symbols

Created by the ToolboxST application and stored in the controller, the symbol table contains signal names and descriptions for diagnostic messages.

task

A group of blocks and macros scheduled for execution by the user.

TBAI

Analog input terminal board, interfaces with VAIC.

TBAO

Analog output terminal board, interfaces with VAOC.

TBCC

Thermocouple input terminal board, interfaces with VTCC.

TBCI

Contact input terminal board, interfaces with VCCC or VCRC.

TCP/IP

Communications protocols developed to inter-network dissimilar systems. It is a de facto UNIX standard, but is supported on almost all systems. TCP controls data transfer and IP provides the routing for functions, such as file transfer and e-mail.

TGEN

Generator terminal board, interfaces with VGEN.

TMR

Triple Modular Redundancy. An operation that uses three identical sets of control and I/O (channels R, S, and T) and votes the results.

ToolboxST

A Windows-based software package used to configure the Mark VIe controllers, also exciters and drives.

TPRO

Turbine protection terminal board, interfaces with VPRO.

TPYR

Pyrometer terminal board for blade temperature measurement, interfaces with VPYR.

TREG

Turbine emergency trip terminal board, interfaces with VPRO.

trend

A time-based plot to show the history of values, similar to a recorder, available in the Historian and the ToolboxST application.

TRL Y

Relay output terminal board, interfaces with VCCC or VCRC.

TRPG

Primary trip terminal board, interfaces with VTUR.

TRTD

RTD input terminal board, interfaces with VRTD.

TSVO

Servo terminal board, interfaces with VSVO.

TTUR

Turbine terminal board, interfaces with VTUR.

TVIB

Vibration terminal board, interfaces with VVIB.

UCVB

A version of the Mark VIe controller.

Unit Data Highway (UDH)

Connects the Mark VIe controllers, LCI, EX2000, PLCs, and other GE provided equipment to the HMI Servers.

validate

Makes certain that the ToolboxST application items or devices do not contain errors, and verifies that the configuration is ready to be built into pcode.

VAMA

IS200VAMA VME Acoustic Monitoring Board that is used in conjunction with the IS200DDPT Dynamic Pressure Transducer Terminal Board to monitor acoustic or pressure waves in the turbine combustion chamber.

VCMI

The Mark VIe VME communication board which links the I/O with the controllers.

VME board

All the Mark VIe boards are hosted in Versa Module Eurocard (VME) racks.

VPRO

Mark VIe Turbine Protection Module, arranged in a self contained TMR subsystem.

Windows NT

Advanced 32-bit operating system from Microsoft for 386-based PCs and above.

word

A unit of information composed of characters, bits, or bytes, that is treated as an entity and can be stored in one location. Also, a measurement of memory length, usually 4, 8, or 16-bits long.



GE Energy
1501 Roanoke Blvd.
Salem, VA 24153-6492 USA

1 540 387 7000
www.geenergy.com